Characterizing Electromigration Effects in a 16nm FinFET Process Using a Circuit Based Test Vehicle

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***Abstract*—**This work showcases measured data corresponding to direct-current (DC) stress induced Electromigration (EM) phenomenon, characterized using on-chip circuits for interconnect test structures fabricated in a 16nm FinFET process. An array-based test vehicle featuring parallel stress and 4-wire Kelvin sensing capabilities is presented, employing wires with distinct feature sizes and metal stacks as the Devices-Under-Test (DUTs). Accelerated stress testing is achieved using on-chip using metal heaters positioned directly above the DUTs, which provides precise local temperature regulation in conjunction with fast cycling between stress and measurement temperatures. Test chip data captures several EM effects ranging from abrupt and/or progressive failures depending on DUT geometry, temporary healing effects, circuit-interconnect interplay, and process variation impacting EM lifetime.

I. Introduction

Although FinFET technologies present a vastly superior alternative from the perspective of power, performance, and area as compared to their planar equivalents, the increased current densities in conjunction with localized thermal effects (self-heating) [1] have resulted in renewed electromigration (EM) concerns for both power and signal interconnections alike [2]. Traditionally, EM effects were characterized by monitoring the resistance of individual wires under stress. Since EM lifetime is a stronger function of temperature than voltage or current, for accelerated testing, the stress temperature must be raised to above 300°C using an extensive test setup. Furthermore, for accurate lifetime prediction, EM data must be collected from a large number of wires which is time consuming due to the limited number of wires that can be stressed together in existing setups.

To overcome the aforementioned testing challenges of EM, this work presents the first circuit based EM characterization test vehicle in a FinFET technology, using on-chip circuits to stress interconnects with different geometries. A fully automated test flow stresses multiple DUTs parallelly using an on-chip heater while also periodically keeping track of their resistances. The presented test vehicle offers a practical on-chip EM characterization approach, enabling efficient data collection from a large population of DUTs and providing deeper insights into underlying effects.

II. Proposed EM Characterization Macro

Fig. 1 presents an overview of the test-vehicle design and chip implementation specifics. The overall architecture follows an array-based scheme, with the unit tile-able block (Fig. 1(c)) housing the DUTs together with the active (stress, measurement and mode-control) circuits comprising the left and the right arrays. The heating area is centrally positioned, with the on-chip heaters employing wide Metal-6 (M6) tracks implemented in a snake-like fashion and uniformly covering the entire area underneath to ensure similar heat distribution throughout. The local die temperature was measured using the on-chip heater structures through 4-terminal Kelvin sensing. The DUTs are routed underneath the heating area using wide feeder tracks to minimize IR drop (Fig. 2) and are folded to maximize the area utilization. The active circuits on either side are placed far away from the central heating area to avoid leakage issues during measurement as well as to prevent damage to the core circuits during stress. The DUT resistance measurement circuitry comprises 4-wire sensing switches per test structure, implemented using I/O based transmission gates as switches, (owing to leakage concerns) which share common output pads on either side: I-High (I_H), I-Low (I_L), V-High (V_H), V-Low (V_L) for the left array, and I'_H, I'_L,V'_H,V'_L for the right array. A one-hot encoded scan sequence is used for selecting the DUTs serially during the measurement window. The stress circuit comprises wide tri-state drivers, enabled using control signals from the scan-chain, with the inputs at either end driven to '1/0' and '0/1', respectively (Fig. 2) to result in a constant unidirectional current flow across the DUT during stress mode. A total of 15 DUT groups, each consisting of 10 wires on either side (total 300 DUTs) are tiled to cover the entire area underneath the heaters. Local stress generation and control provides the flexibility to stress one or several DUT groups simultaneously. The scan chain is implemented using D flip flops employing staggered two-phase clocking to prevent hold time issues during operation at elevated temperatures.

Fig. 2 illustrates the interconnect test structures with different geometries implemented in this work. Each of the test structures is composed of wide metal feeder lines connected using multiple vias which ensures redundancy at the driver end and a single via at the DUT end. This combination then implements an upstream / downstream for the case of M2 Feeder – M3 DUT (M2-M3) and M4 Feeder – M5 DUT (M4-M5), and a downstream / upstream for M4 Feeder – M3 DUT (M4-M3). The M3 as well as M5 DUTs are implemented using the minimum width allowed by the process. The via width for M3 lines is the same as the DUT width whereas for M5 lines the contact is fully enclosed. Wire lengths of 50µm, 100µm and 200µm were implemented for each of the DUT types.

III. TEST SETUP AND EXPERIMENT METHODOLOGY

Fig. 3 shows the measurement setup used for the DC stress experiments. The test chip is interfaced using a socket-based PCB (inset), placed inside a temperature chamber cooled to 20°C (discussed shortly). An FPGA based control is used for sequencing the scan-chain. Kelvin sensing for the heaters and the DUT is carried out using Source-Measure Units (SMU).

Fig. 4 shows the detailed test sequence. In this work, the on-chip metal heaters themselves are used to establish and monitor a desired stress temperature using the Temperature Coefficient of Resistance (TCR) method. Therefore, the first step in the experiment flow begins with the TCR extraction for the individual heaters. Fig. 5(a) presents the individual heater resistance distributions recorded from 11 test chips at 0°C showing a mean heater resistance of 44.71Ω and a standard deviation of 1.78Ω. Fig. 5(b) shows the extracted TCR measured by ramping up the chamber temperature from 0°C to 100°C in steps of 20°C as well as the extrapolation using the linear model to desired stress temperature of 325°C. The measurements demonstrate excellent linearity, however slight variations in the fresh heater resistance at 0°C (p2 parameter) as well as the TCR coefficient p1 result in dissimilar resistance values for the same target stress temperature, emphasizing the importance of precise per-heater TCR characterization. Furthermore, leakage in the DUT 4-wire switches at high stress temperatures corrupts the resistance measurement, therefore the temperature needs to be brought down during measurement. We chose a measurement temperature of 100°C as no leakage effects were detected in the sensing switches at this temperature.

With the stress and measurement targets extrapolated, the individual heater voltages are ramped up in varying steps to reach within 0.5% of the targeted resistance values. A proportional-integral-derivative (PID) loop implemented in software monitors and regulates each on-chip heater temperature separately. A tight temperature control is especially needed for recording DUT resistances to suppress measurement artifacts, and the loop ensures that all individual heaters stay close to their target temperature prior to each sampling. The heater voltage polarity is also reversed every 5 seconds, to prevent EM induced heater failures [3]. Once the resistance values are measured, the heaters are ramped up to stress temperature (325°C) for 20 minutes with the cycle continuously looped. Fig. 6(a) presents the measured heater resistance values as well as the extrapolated stress temperatures during the repetitive measure-stress cycles.

Fig. 6(b) shows the average heater currents over a stress cycle measured from multiple dies at ambient temperatures of -20°C and +20°C, with the applied voltages being between 6.9V and 8.3V. A lower ambient temperature, although useful from the perspective of cooling the active circuits, imposes higher power requirements on the heaters to generate the same stress temperature leading to shorter heater lifetimes. From Fig. 6(b), it can be noted that heater B sandwiched between heaters A and C, draws the lowest current of the three, attributed to the additional heat generated from both sides. Figs. 5(b) and 5(c) show changes in heater resistance over time and the measured pre/post stress TCR. The heater resistance degrades over time which can be attributed to the sharp temperature cycling in this work, causing the heater to draw larger currents with longer stress time.

IV. DISCUSSION OF MEASURED RESULTS

Fig. 7 presents the sampled resistance traces and the corresponding lognormal failure distributions, collected from a total of 70 wires corresponding to shorter 50µm flavor for each of the distinct wire types. The stress voltage of the driver circuit was 1.5V and the stress temperature was 325°C. Abrupt (3-10X) jumps in resistance were observed in most cases for each of the narrow M2-M3, M3-M4 wires featuring via enclosure on only one side, with some cases exhibiting jumps as high as 16-25X, to rare GΩ order shifts. These failures can be attributed to 'slit void' formations directly underneath the via as shown in [4]. Compared to our previous 32nm results in [3] where resistance jumps were typically more than 100X, the resistance change was smaller in this process. Some wires showed unique trace patterns such as the one highlighted in Fig. 7 (upper left) where the resistance peaks first followed by intervals of partial recovery and even full healing [3, 5], eventually followed by abrupt shifts. In contrast, the wider M4-M5 wires featuring a full contact enclosure exhibited both abrupt failures as well as progressive monotonic shifts in the DUT resistance over time. Progressive failures resulting in monotonic shifts have been reported previously in literature for both downstream and upstream stressed wires [4 ,6], however, the wider width of M4 feeder line in our implementation would point to either the M4-M5 via or the M5 metal line itself as being the plausible failure location, likely making the failure an upstream one.

Lognormal failure distributions (failure criteria defined as 10% resistance shift) in Fig. 8 show similar average time-to-failure for the three flavor types (50µm). This interesting phenomenon can attributed to the constant voltage stress condition used in this work, resulting in higher stress current density in the wider wire competing against faster transistor degradation in the driver circuit due to pronounced hot-carrier effects. In addition, the current density requirements needed to induce EM vary between the test-structures due to the structure and implementation differences such as the metal stack and wire widths. It should be noted that process variations also impact the distribution [7], with the wider M5 DUTs exhibiting tight failure bounds, possibly due to the lower spread in the fresh wire resistance values as shown in Fig. 9. Fig. 10 presents the stress current degradation over time, collected from three test chips, which can be explained by both EM induced failures as well as current degradation over time for the stress circuits. Fig. 11 presents results from the longer 100µm and 200µm wires, for which relatively fewer failures were observed at 325°C, a consequence of reduced stress current density owing to the 2-4X higher DUT resistance.

REFERENCES

[1] D. Jang, E. Bury, R. Ritzenthaler et. al., IEDM, pp. 11.6.1-11.6.4., 2015
[2] Y. Sun, C. Zhan, J. Guo, et al., IRPS, pp. 3D.2.1-3D.2.6, 2015
[3] C. Zhou, X. Wang, R. Fung, et al., VLSI Technology, pp. T42-T43, 2015
[4] S. Lee and A. S. Oates, IRPS, pp. 107-114, 2006
[5] A. W. Hunt, S. P. Riege, and J. A. Prybyla, Applied Physics Letters, vol. 70, no. 19, pp. 2541–2543, 1997
[6] A. S. Oates and M. H. Lin, TDMR, vol. 9, no. 2, pp. 244-254, June 2009
[7] A. H. Fischer, A. von Glasow, S. Penka et. al., IITC, pp. 253-255, 2003

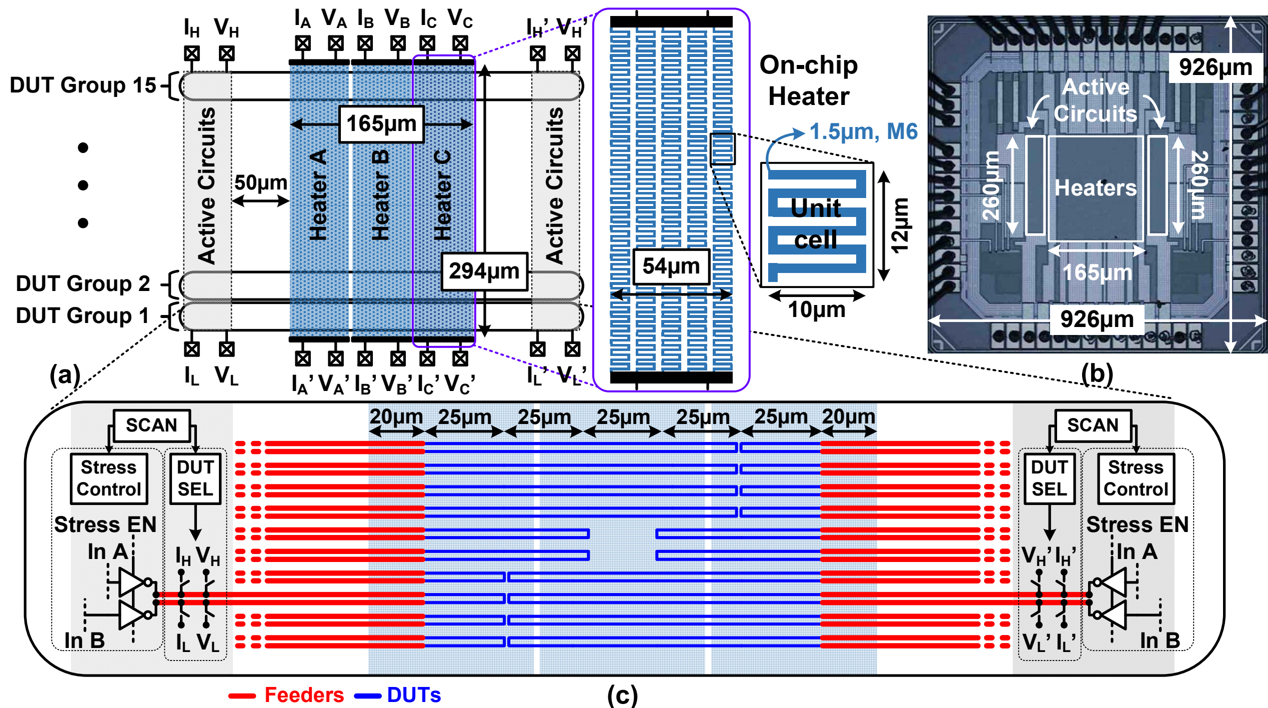
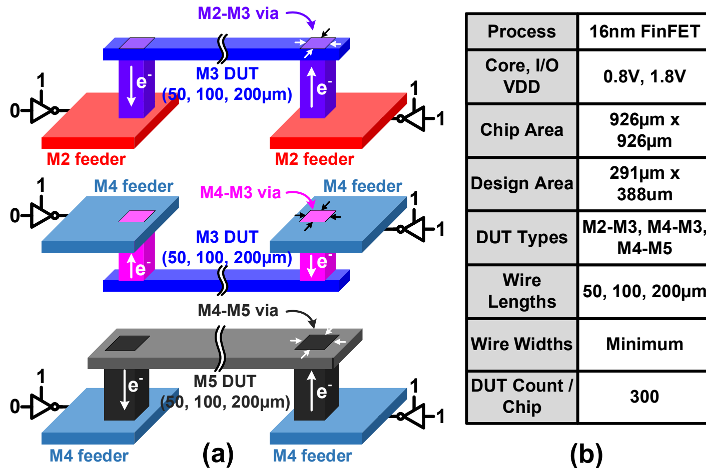


Fig. 1. (a) Overview of the 16nm EM test-vehicle and on-chip heater specifics, (b) Die-micrograph and (c) Unit Tile-able DUT group details



Process	16nm FinFET
Core, I/O VDD	0.8V, 1.8V
Chip Area	926µm x 926µm
Design Area	291µm x 388um
DUT Types	M2-M3, M4-M3, M4-M5
Wire Lengths	50, 100, 200µm
Wire Widths	Minimum
DUT Count / Chip	300

Fig. 2. Interconnect structure, stress details and implementation summary

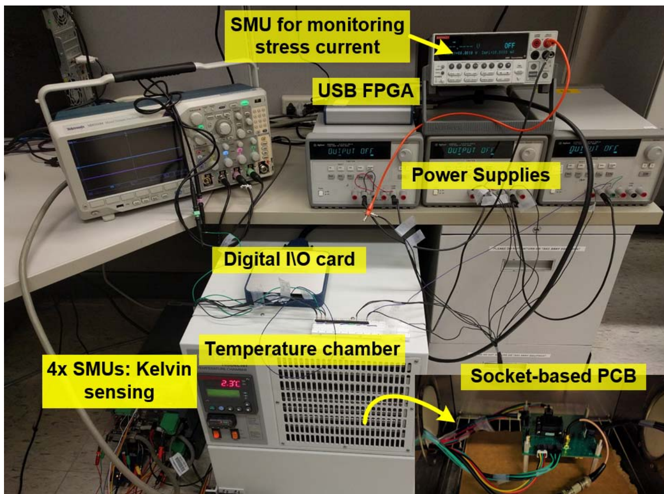


Fig. 3. Measurement setup

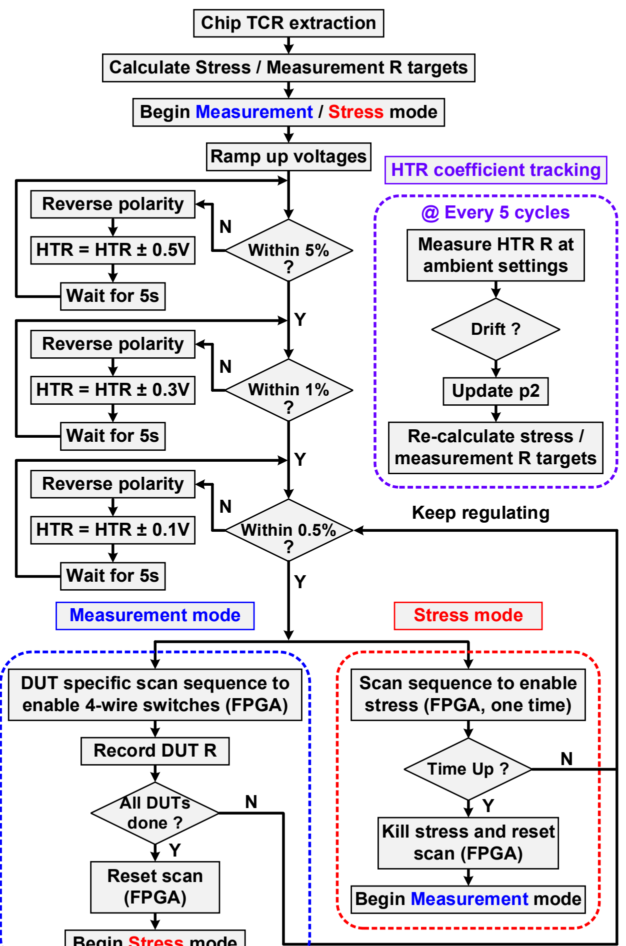


Fig. 4. Automated test flow for TCR extraction, on-chip temperature regulation, stress control, and data collection.

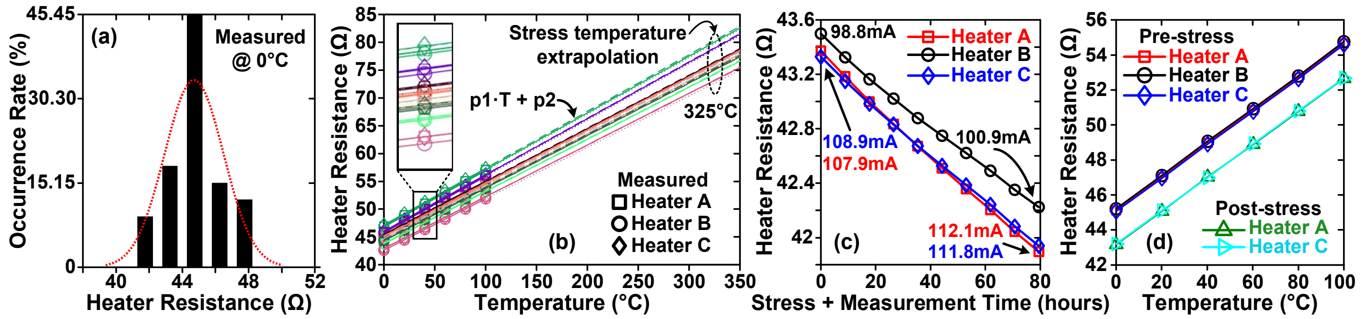


Fig. 5 (a) Time 0 heater resistances (b) Measured TCR (c) Degradation in heater resistance over time and (d) Pre / post measurement TCR

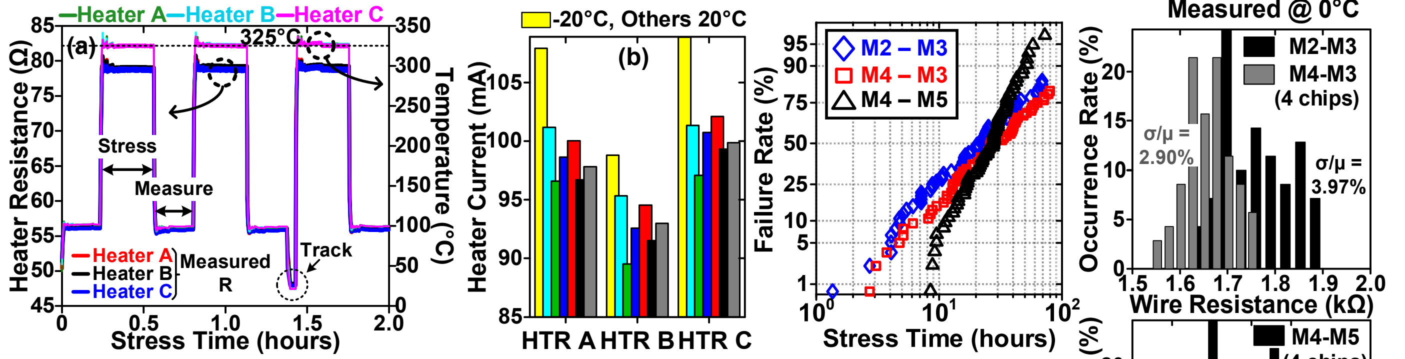


Fig. 6 (a) Temperature cycling (b) Heater current at 325°C from multiple dies

Fig. 8 Overall lognormal curves

Fig. 9 Fresh DUT distributions

Fig. 7 Resistance traces (left) and corresponding lognormal failure distributions (right) for 50µm DUTs

Fig. 10 I_{STRESS} degradation

Fig. 11 EM in longer wires