Session 17 - Modeling, Reliability and Safety

A Counter based ADC Non-linearity Measurement Circuit and Its Application to Reliability Testing

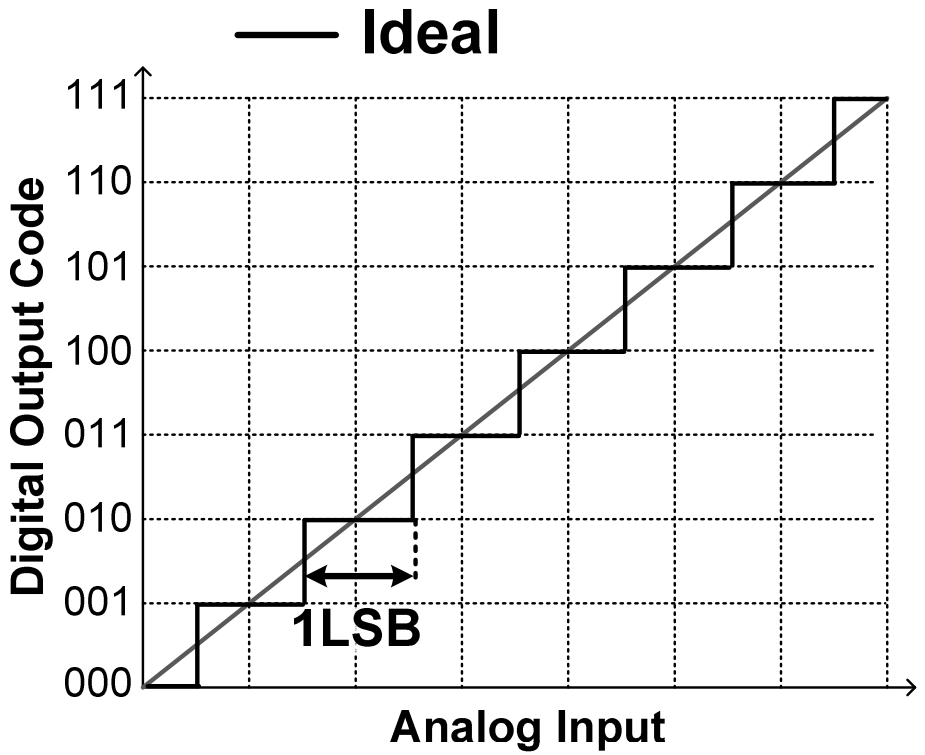
Gyusung Park, Minsu Kim, Nakul Pande,
Po-wei Chiu, Chris H. Kim

University of Minnesota, Minneapolis, USA

Outline

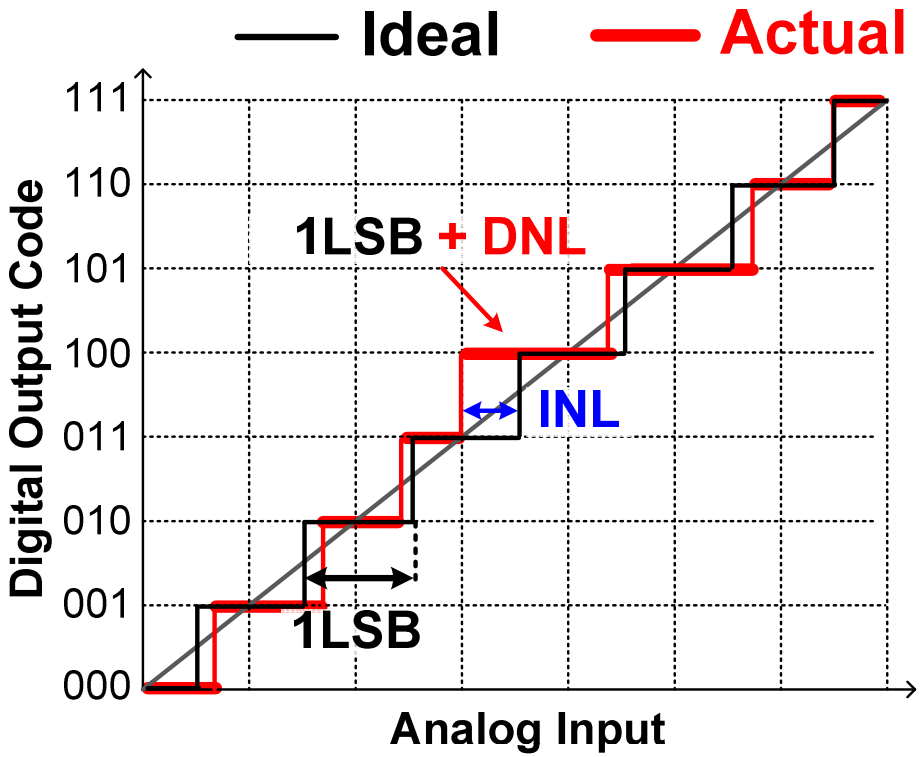
- Background
- Proposed ADC Non-linearity Measurement Circuit
- 65nm Test Chip Results
- Application to ADC Reliability Studies
- Conclusion

Analog-to-Digital Converter (ADC) Non-linearity



- Differential Non-Linearity (DNL) : Deviation from ideal width (1LSB)
- Integral Non-Linearity (INL) : Maximum deviation from ideal slope

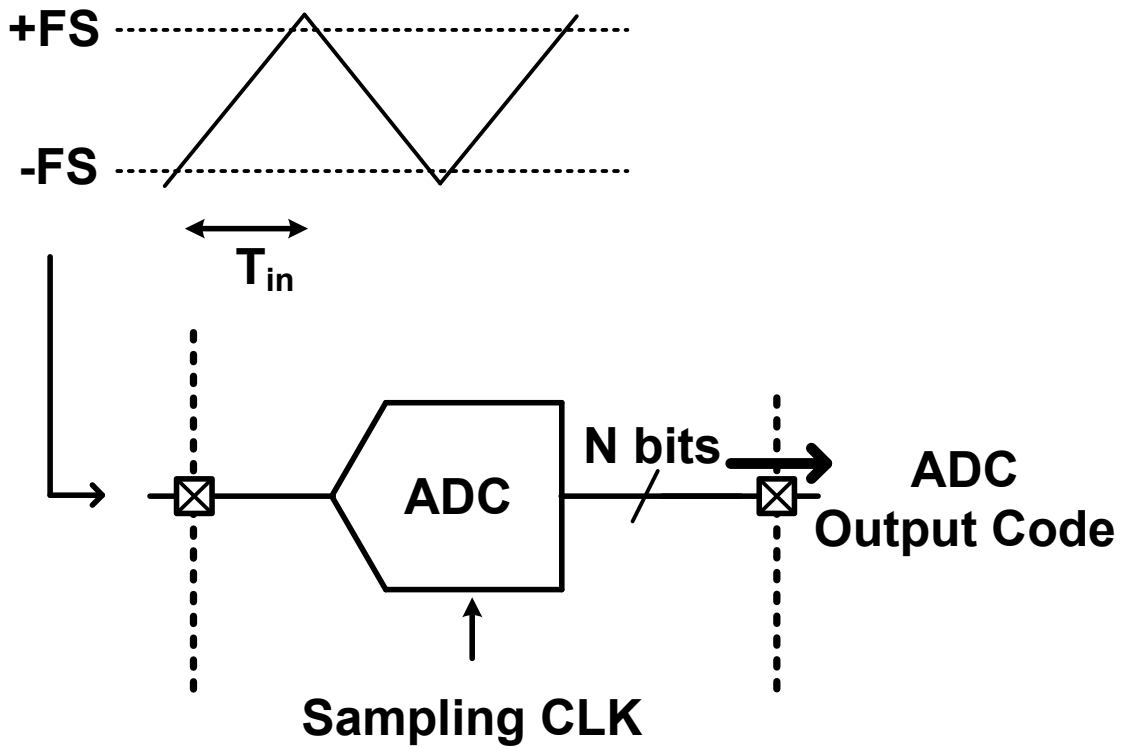
Analog-to-Digital Converter (ADC) Non-linearity



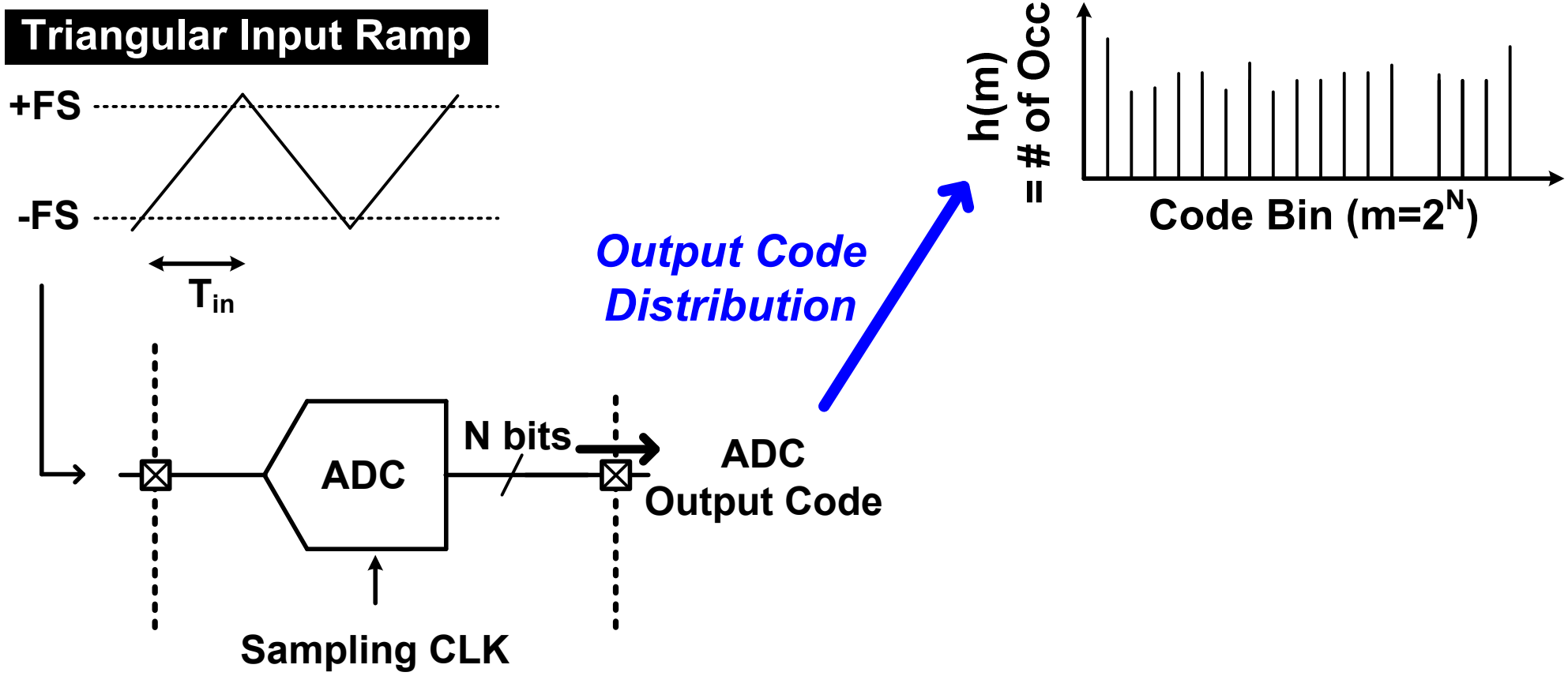
- Differential Non-Linearity (DNL) : Deviation from ideal width (1LSB)
- Integral Non-Linearity (INL) : Maximum deviation from ideal slope

ADC Non-linearity Testing: Histogram Method

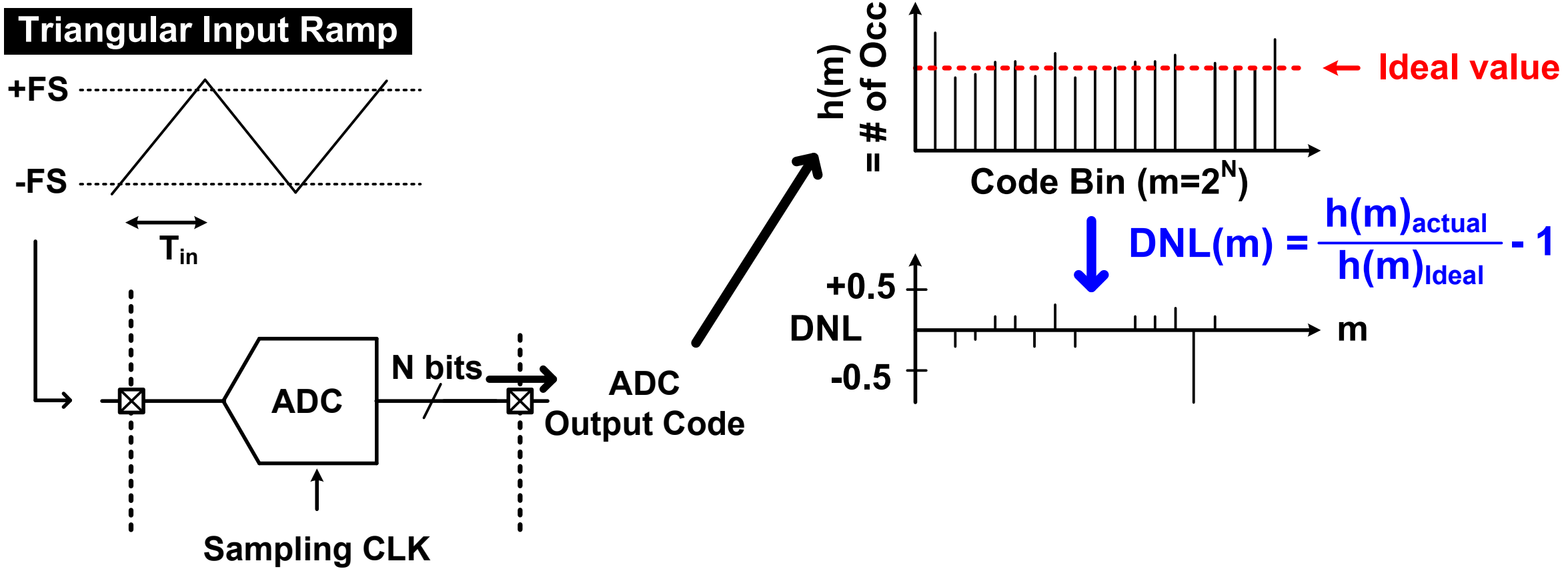
Triangular Input Ramp



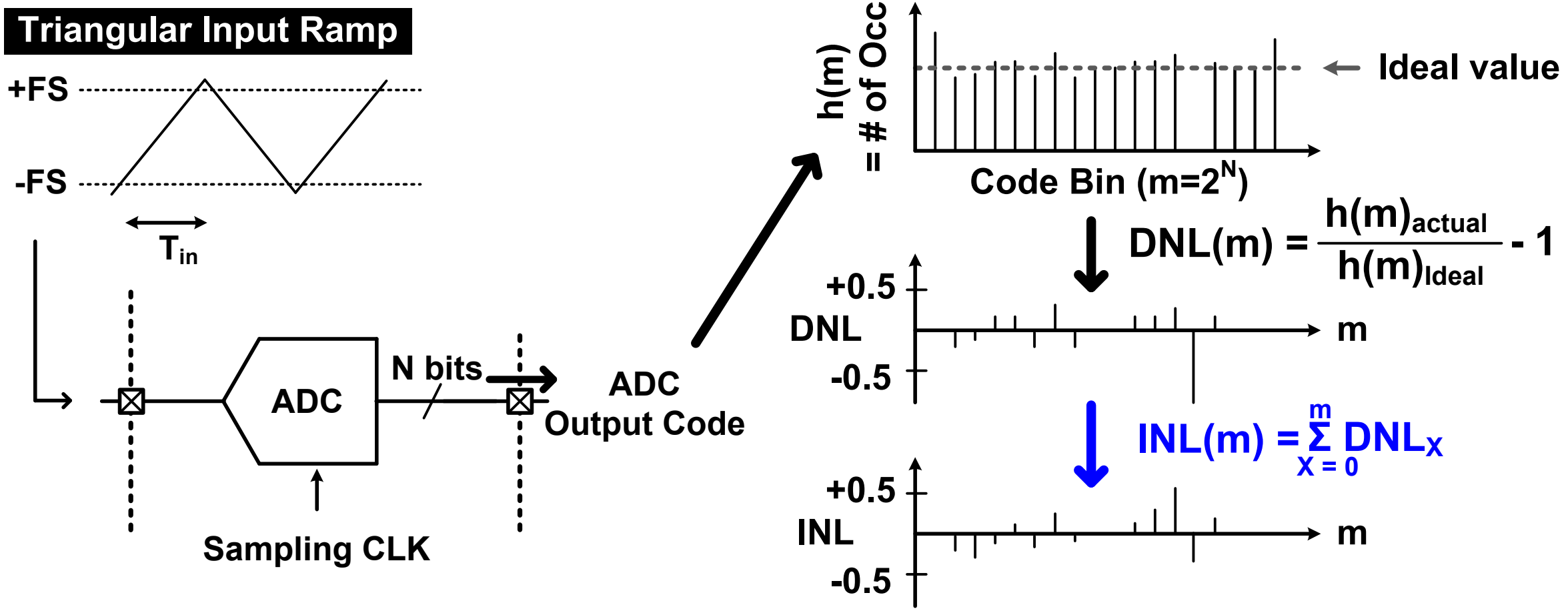
ADC Non-linearity Testing: Histogram Method



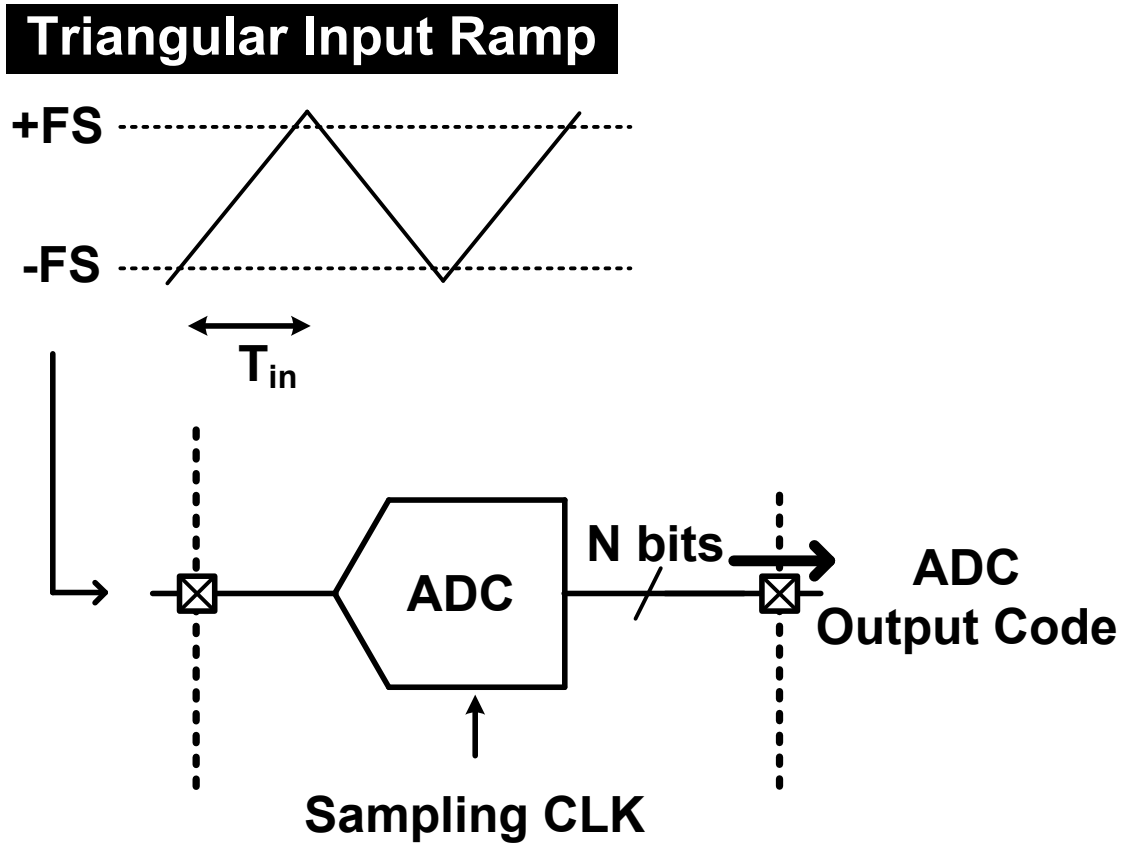
ADC Non-linearity Testing: Histogram Method



ADC Non-linearity Testing: Histogram Method



ADC Non-linearity Testing: Histogram Method



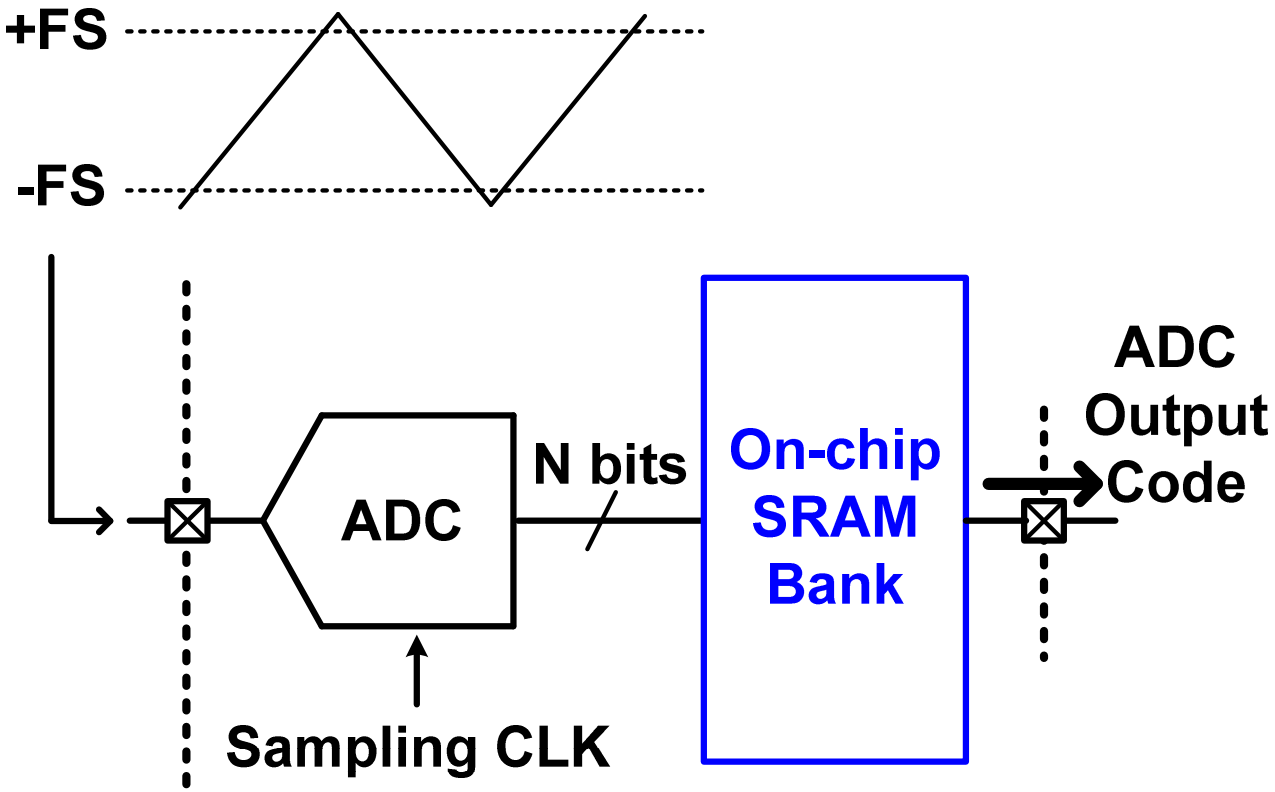
Pros.

- Simple setup
  : Does not require any on-chip measurement circuits

Cons.

- Susceptible to package and on-chip noise

Conventional On-chip Test Setup



L. Kull, et al., *ISSCC 2014*

Pros.

- Better noise immunity
  : Separate ADC operation from data transfer operation

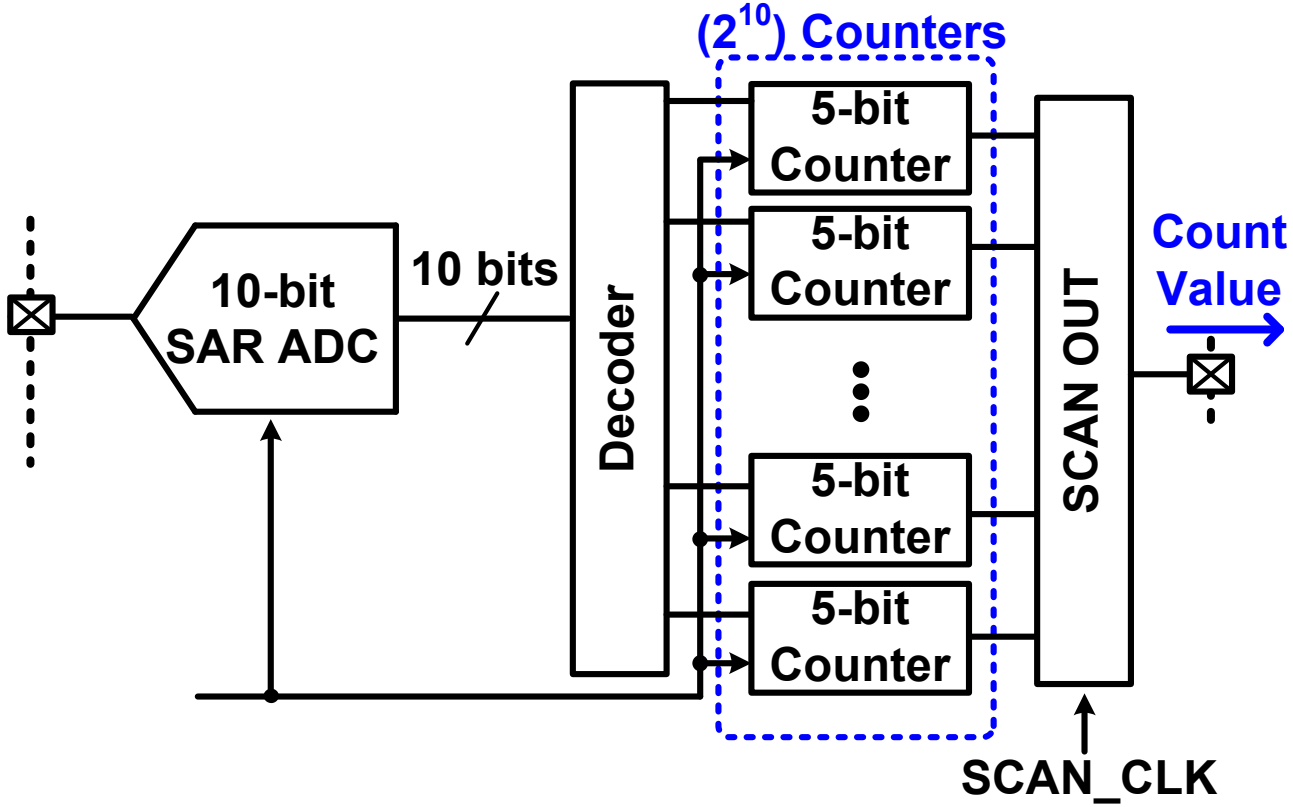
Cons.

- Requires large on-chip memory (~1megabits) and long data transfer time

Outline

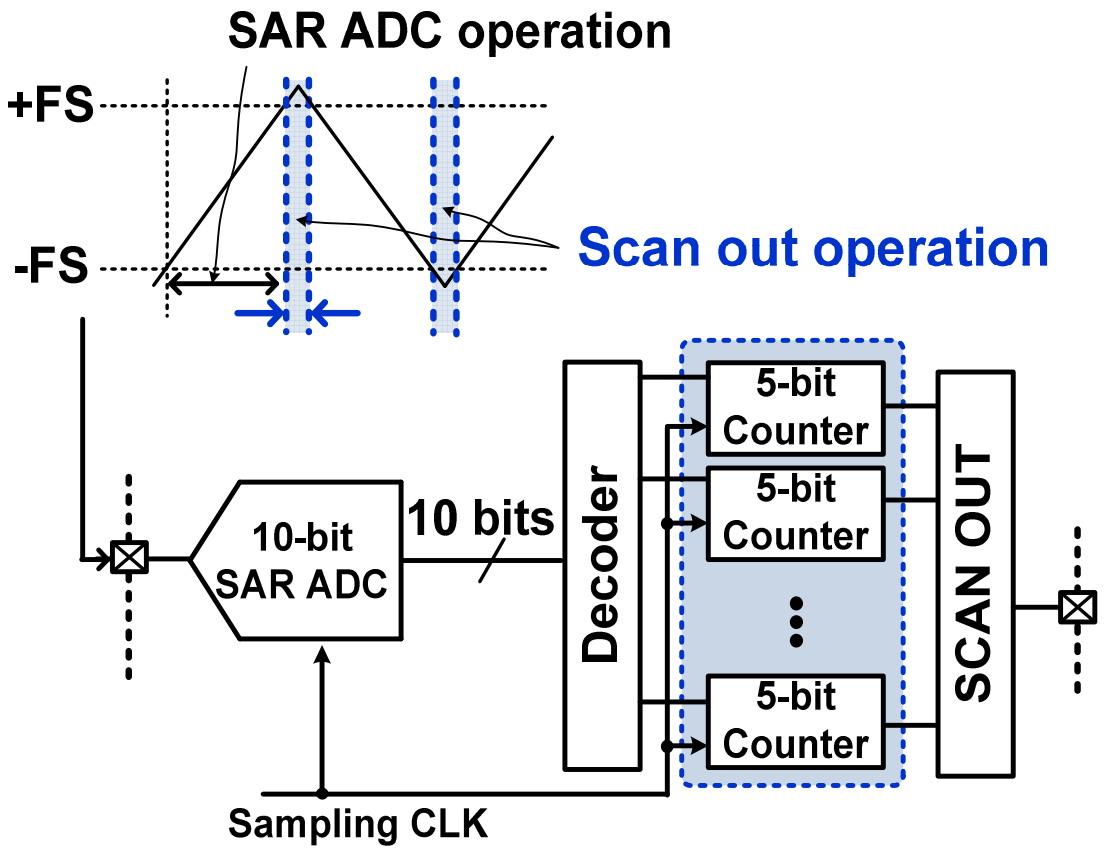
- Background
- **Proposed ADC Non-linearity Measurement Circuit**
- **65nm Test Chip Results**
- Application to ADC Reliability Studies
- Conclusion

Proposed In-situ DNL/INL Measurement Circuit (10b)



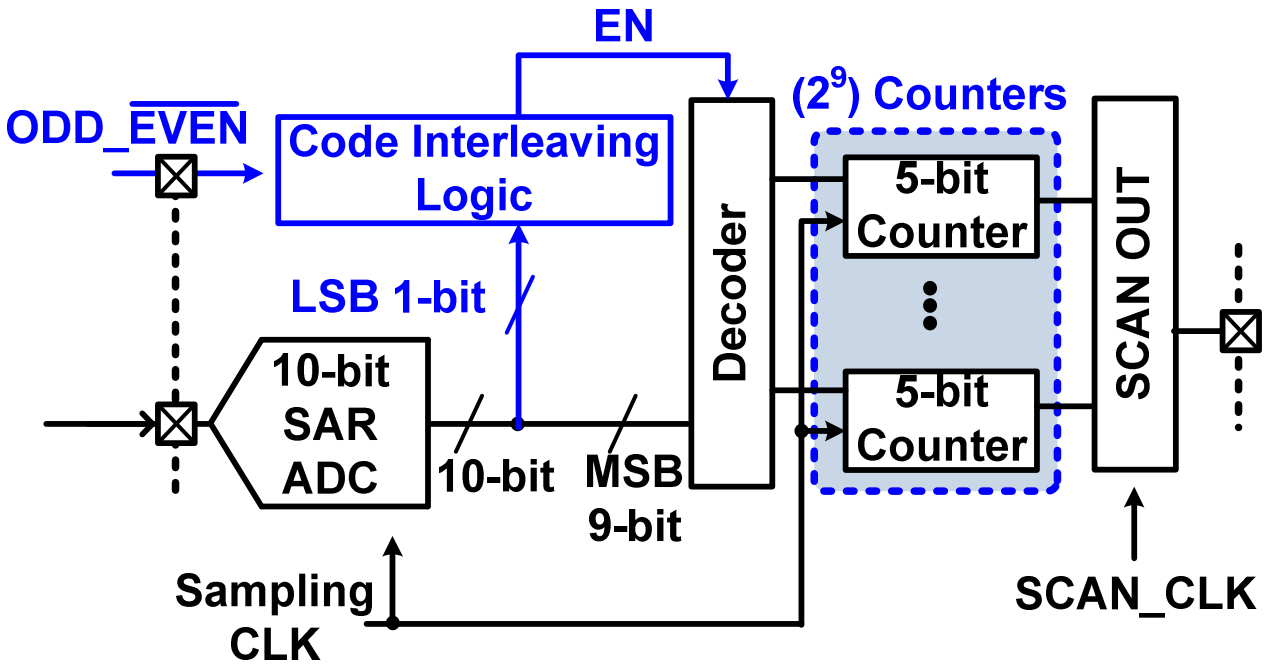
- Consists of a decoder block + array of 5b counters
- Counters corresponding to ADC codes increment their count value
- Count value instead of ADC output code → readout data volume↓

Proposed In-situ DNL/INL Measurement Circuit (10b)



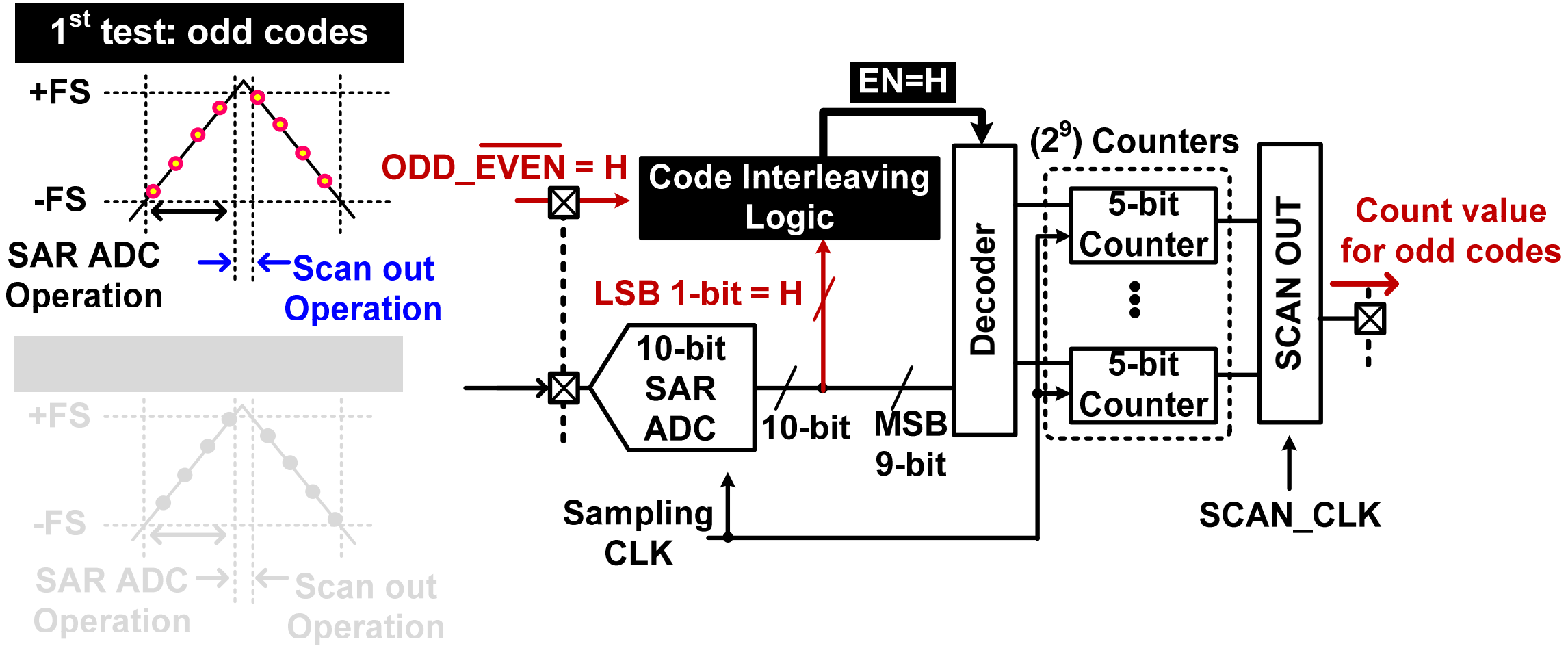
- Separate ADC operation from data transfer operation
- Readout data volume↓
  → small area overhead for storing data compared to SRAM array

Interleaved Design for Area Reduction

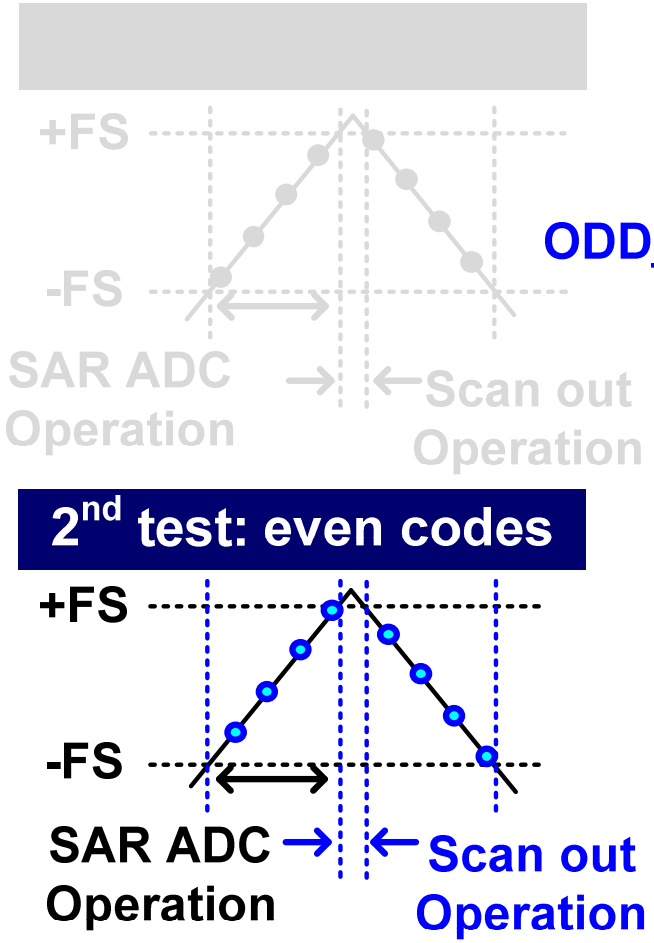


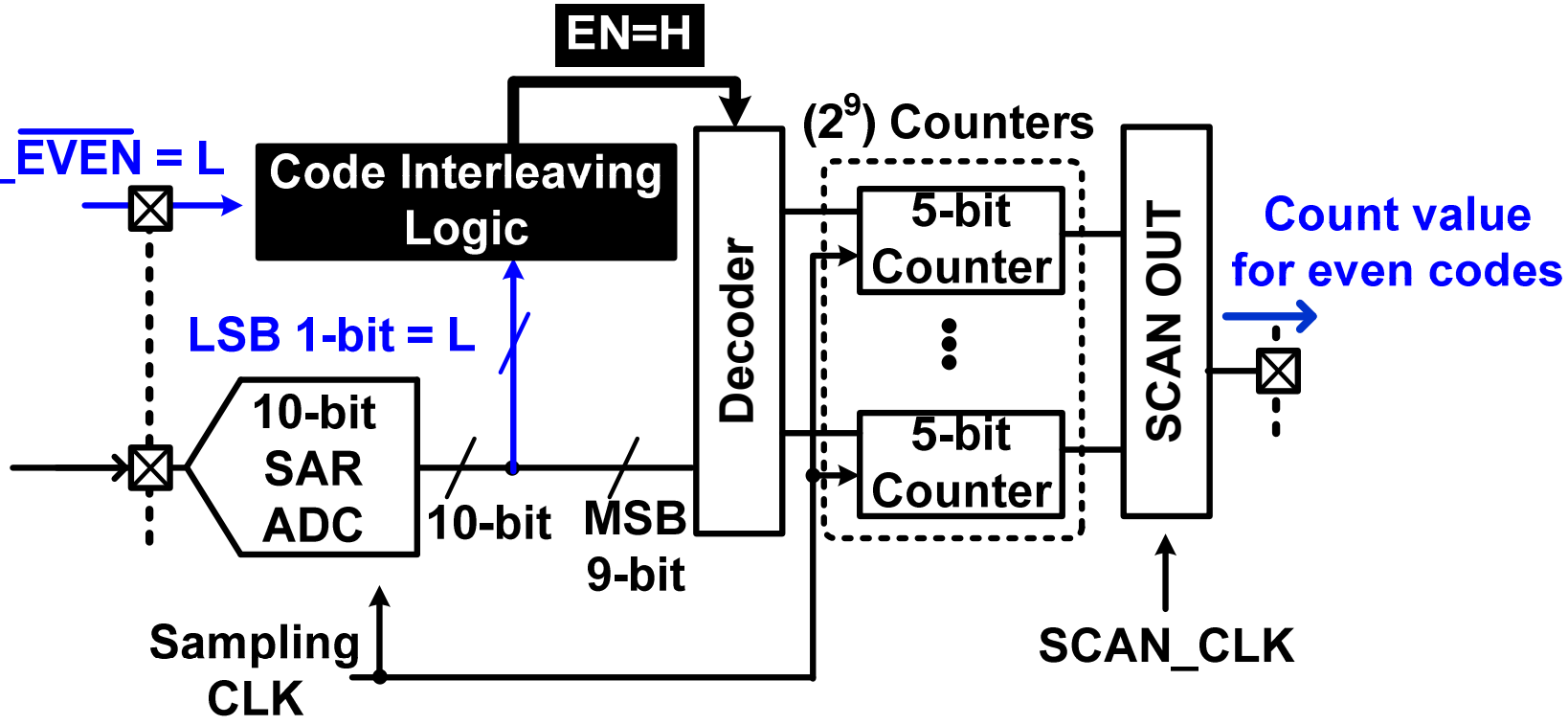
- 2-way interleaved design with only 50% counters
- Two separate tests for odd and even codes
- Stitch two test results for full DNL & INL histogram

Step 1: Odd Code Measurement

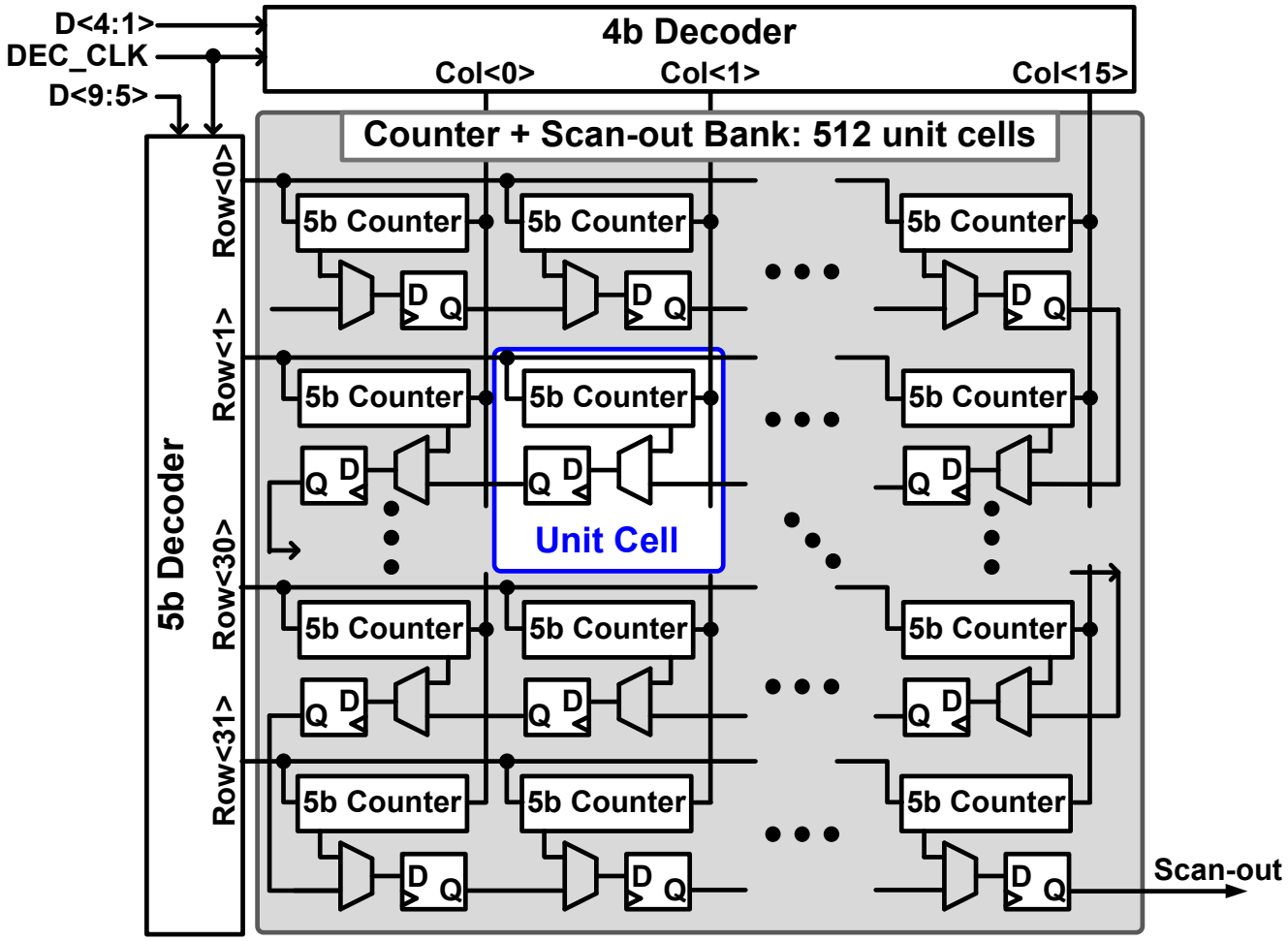


Step 2: Even Code Measurement





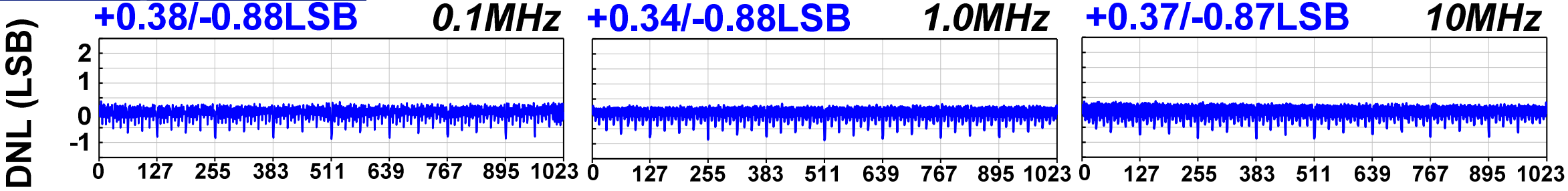
Implementation of DNL/INL Measurement Circuit



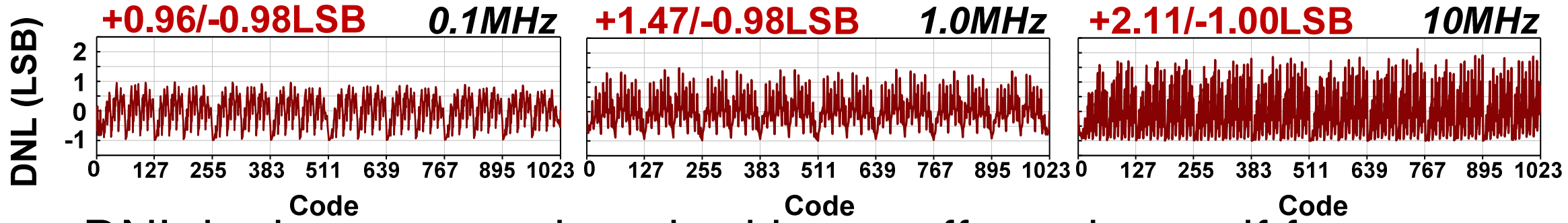
- Total 512 5-bit counters corresponding to ADC out D<9:1>
- Unit cell = 5b counter + scan-out circuits

Noise Immunity: Proposed vs. Off-chip Test

Proposed



Off-chip

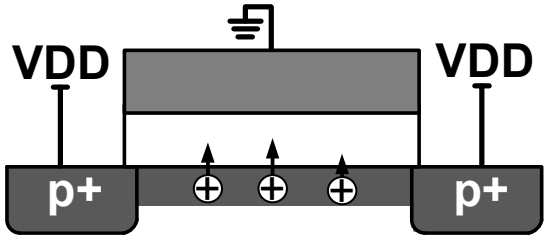


- DNL in the proposed method is not affected even if frequency increases
- Proposed method eliminates package and board noise issues

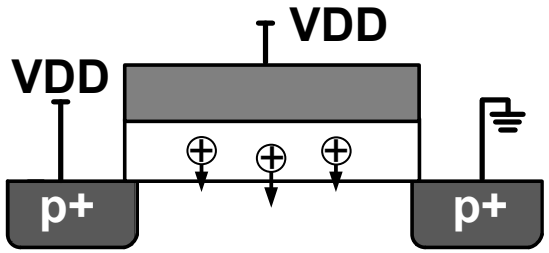
Outline

- Background
- Proposed ADC Non-linearity Measurement Circuit
- 65nm Test Chip Results
- **Application to ADC Reliability Studies**
- Conclusion

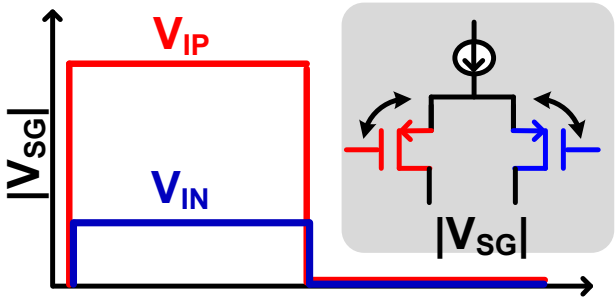
Short-term Vth Instability

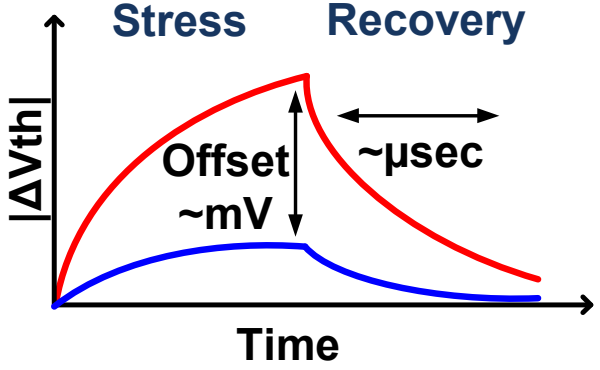


Stress (on-state)



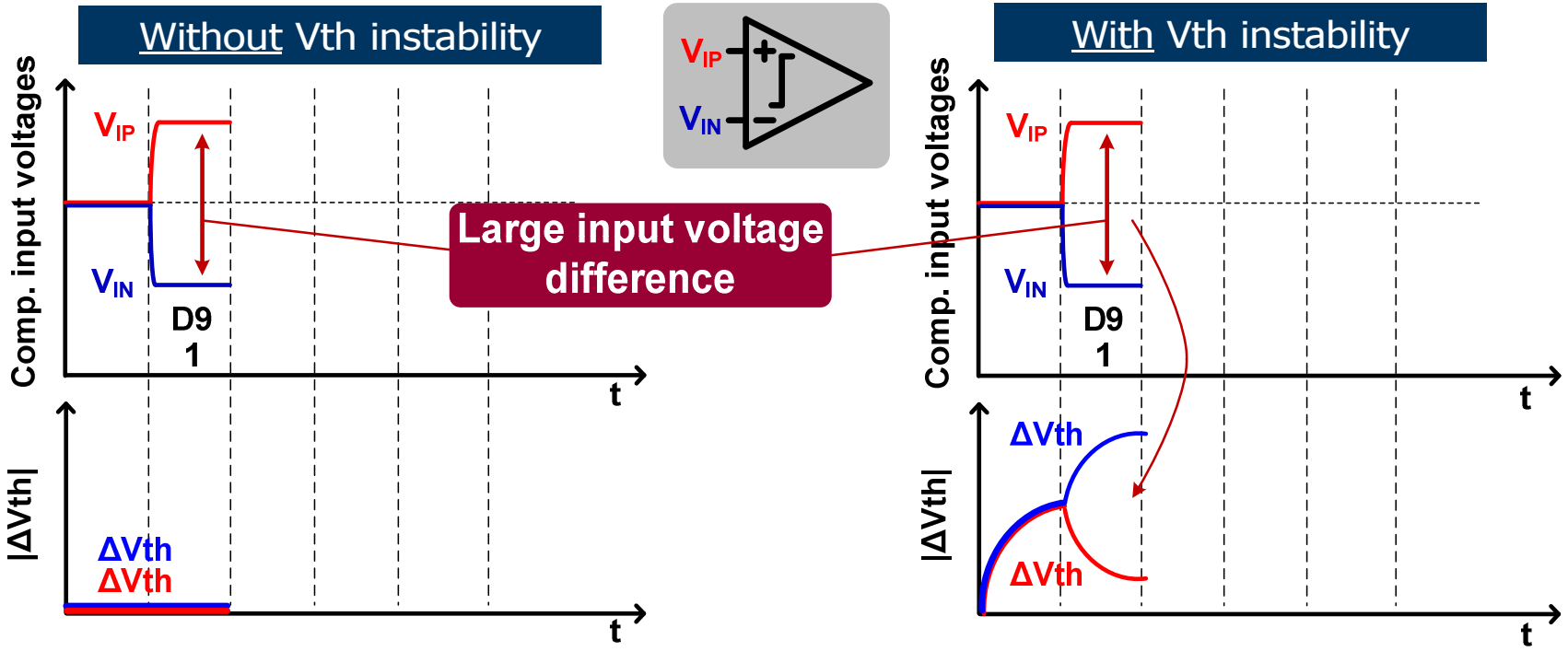
Recovery (off-state)





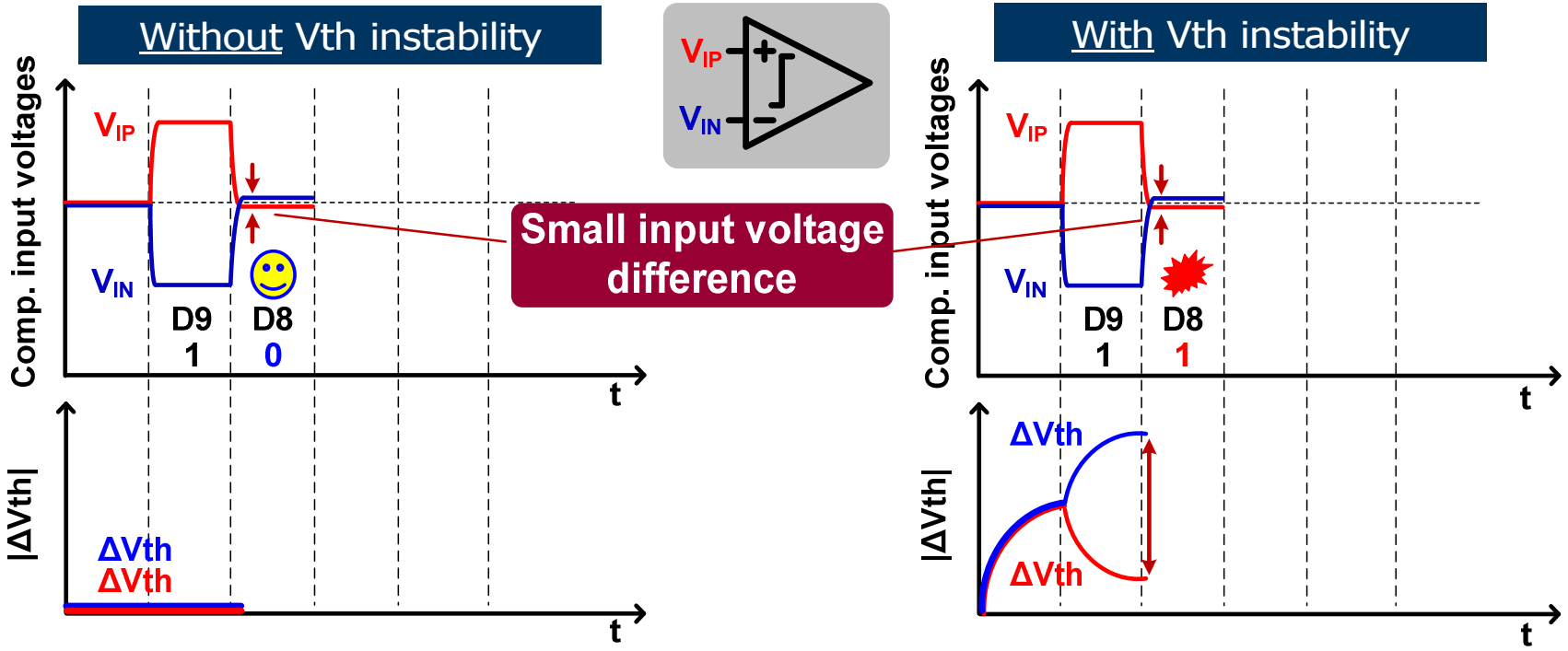
- Short-term Vth degradation and recovery occur due to Bias Temperature Instability (BTI)
- Time constant usually in the µs ~10's of µs order

Impact on SAR-ADC Operation



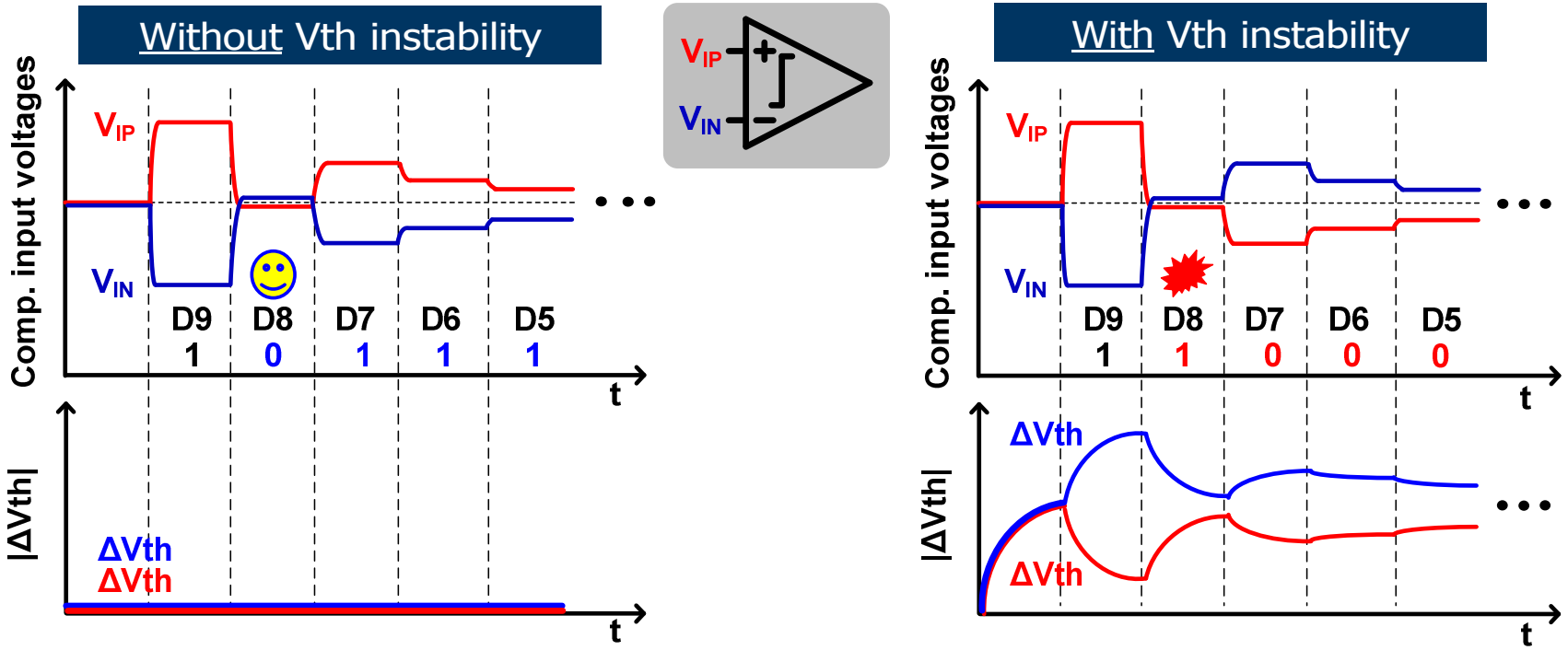
- Large input voltage difference → offset due to short-term Vth shifts

Impact on SAR-ADC Operation



- If input voltage difference < Vth shift difference in the next step → incorrect decision

Impact on SAR-ADC Operation



- Manifests as a 1LSB error in the output code
  - Correct code pattern "**0111**" vs Incorrect code pattern "**1000**"
- Affects high-resolution, low-speed SAR-ADCs

Output Codes Vulnerable to Short-term BTI

Digital out							Conv. step generating error
Decimal value	Binary D9	D8	D7	D6	D5	•••	
127	0	0	0	1	1	•••	D7
128	0	0	1	0	0	•••	
255	0	0	1	1	1	•••	D8
256	0	1	0	0	0	•••	
383	0	1	0	1	1	•••	D7
384	0	1	1	0	0	•••	
639	1	0	0	1	1	•••	D7
640	1	0	1	0	0	•••	
767	1	0	1	1	1	•••	D8
768	1	1	0	0	0	•••	
895	1	1	0	1	1	•••	D7
896	1	1	1	0	0	•••	

W. Choi, C. H. Kim, *CICC 2015*

- Prior arts identified vulnerable output codes
  - Error can occur from second conversion step
  - Odd codes ending with **0111**…
  - Even codes ending with **1000**…

Output Codes Vulnerable to Short-term BTI

Digital out							Conv. step generating error
Decimal value	Binary D9	D8	D7	D6	D5	•••	
127	0	0	0	1	1	•••	D7
128	0	0	1	0	0	•••	
255	0	0	1	1	1	•••	D8
256	0	1	0	0	0	•••	
383	0	1	0	1	1	•••	D7
384	0	1	1	0	0	•••	
639	1	0	0	1	1	•••	D7
640	1	0	1	0	0	•••	
767	1	0	1	1	1	•••	D8
768	1	1	0	0	0	•••	
895	1	1	0	1	1	•••	D7
896	1	1	1	0	0	•••	

- E.g. Error occurring in **D8** step
  - Large ΔV_{IN} @D9 + small ΔV_{IN} @D8
  - Odd codes ending with **0111**

Adjacent even codes ending with **1000**

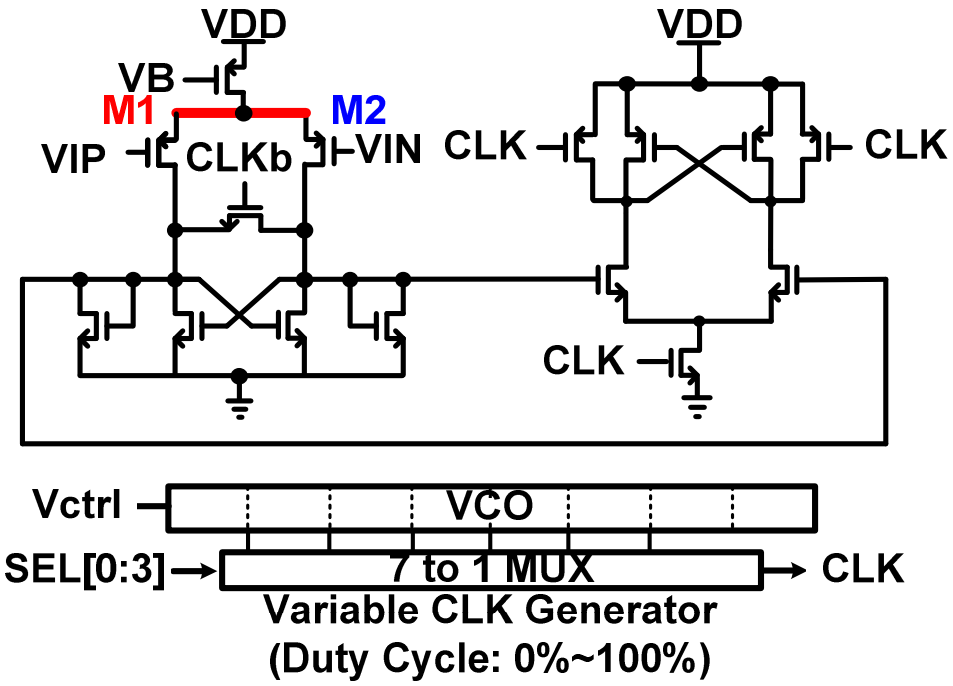
Output Codes Vulnerable to Short-term BTI

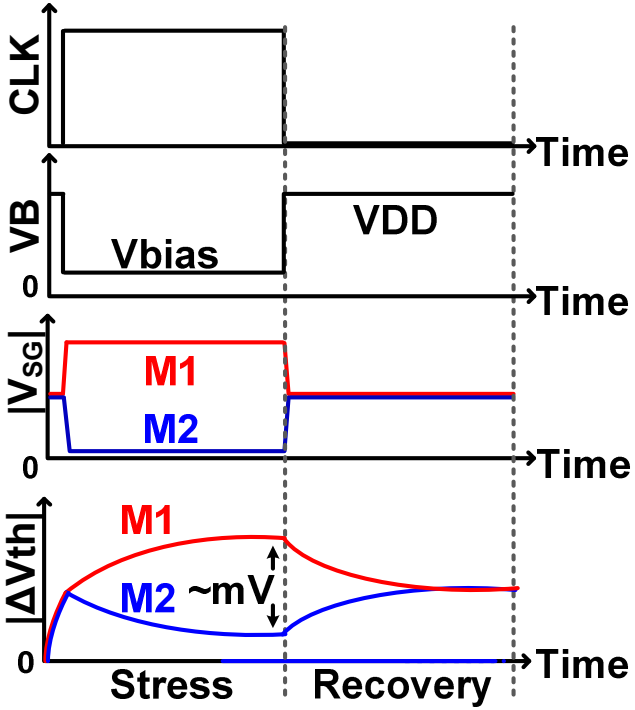
Digital out							Conv. step generating error
Decimal value	Binary D9	D8	D7	D6	D5	•••	
127	0	0	0	1	1	•••	D7
128	0	0	1	0	0	•••	
255	0	0	1	1	1	•••	D8
256	0	1	0	0	0	•••	
383	0	1	0	1	1	•••	D7
384	0	1	1	0	0	•••	
639	1	0	0	1	1	•••	D7
640	1	0	1	0	0	•••	
767	1	0	1	1	1	•••	D8
768	1	1	0	0	0	•••	
895	1	1	0	1	1	•••	D7
896	1	1	1	0	0	•••	

- E.g. Error occuring in **D7** step
  - Large ΔV_{IN} @D9, D8 + small ΔV_{IN} @D7
  - Odd codes ending with **0111**

  Adjacent even codes ending with **1000**

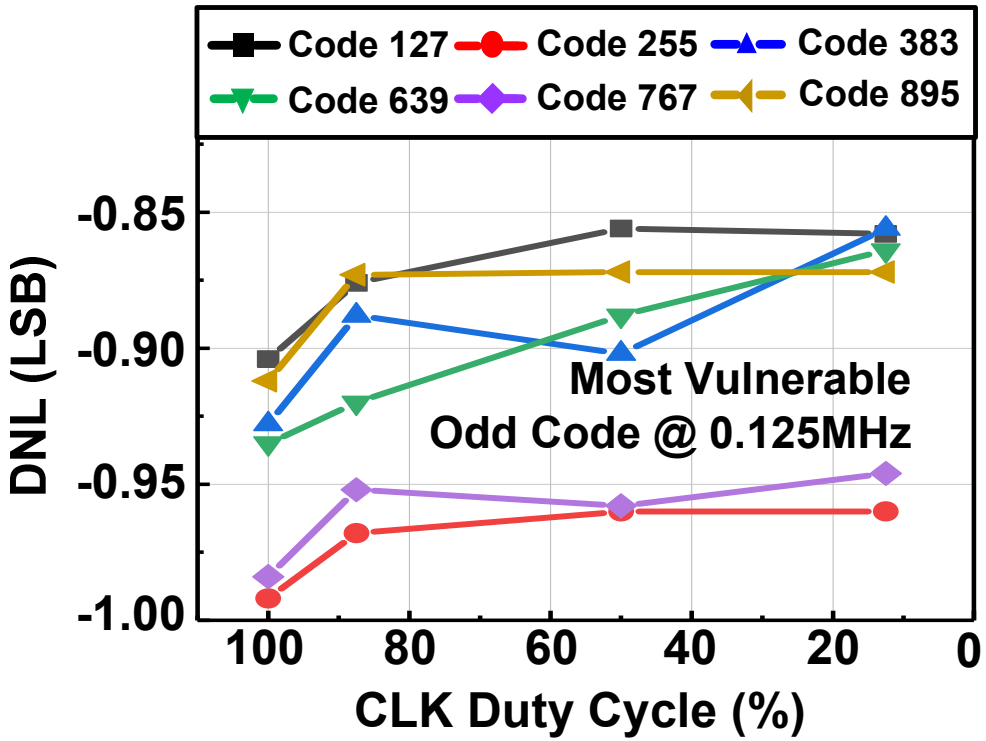
Stress Equalization, Variable Duty Cycle

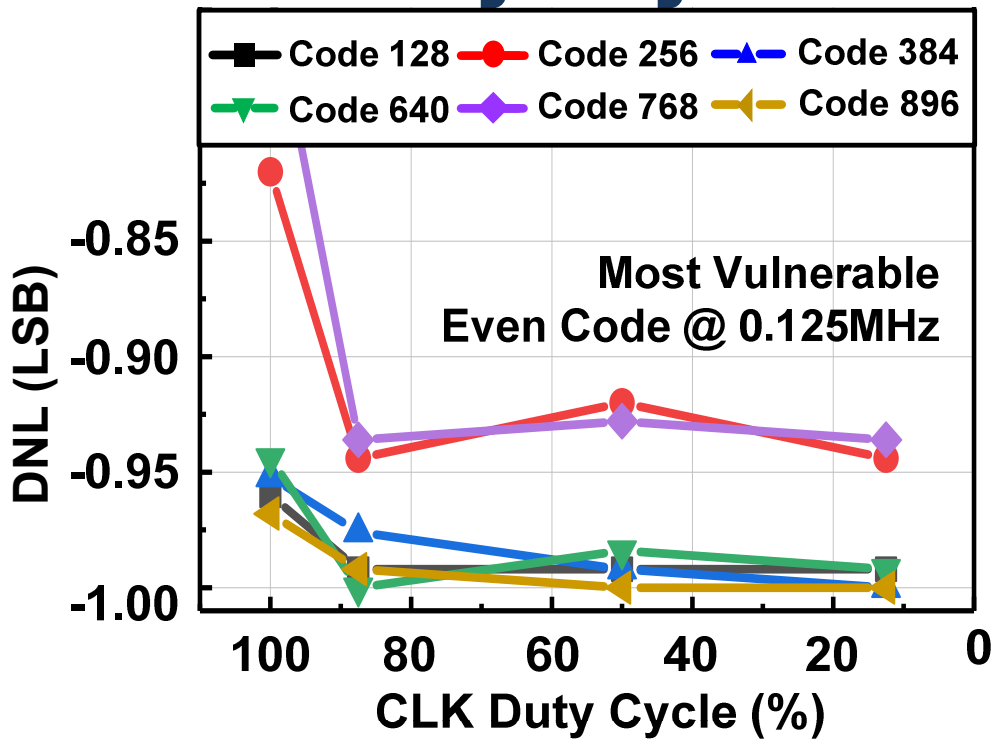




- Stress equalization using switched source node
- Ratio between stress and recovery times can be varied
  - Multi-phase VCO used to generate different duty cycles

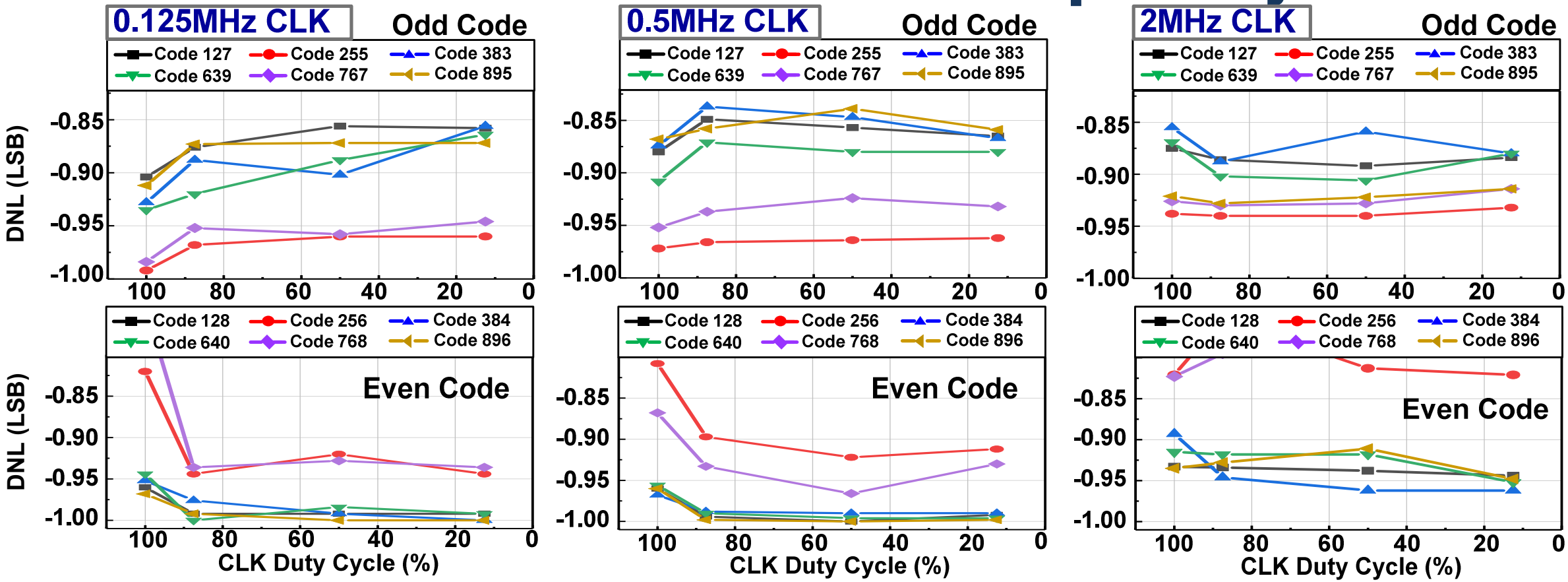
10b SAR-ADC DNL vs. Duty Cycle





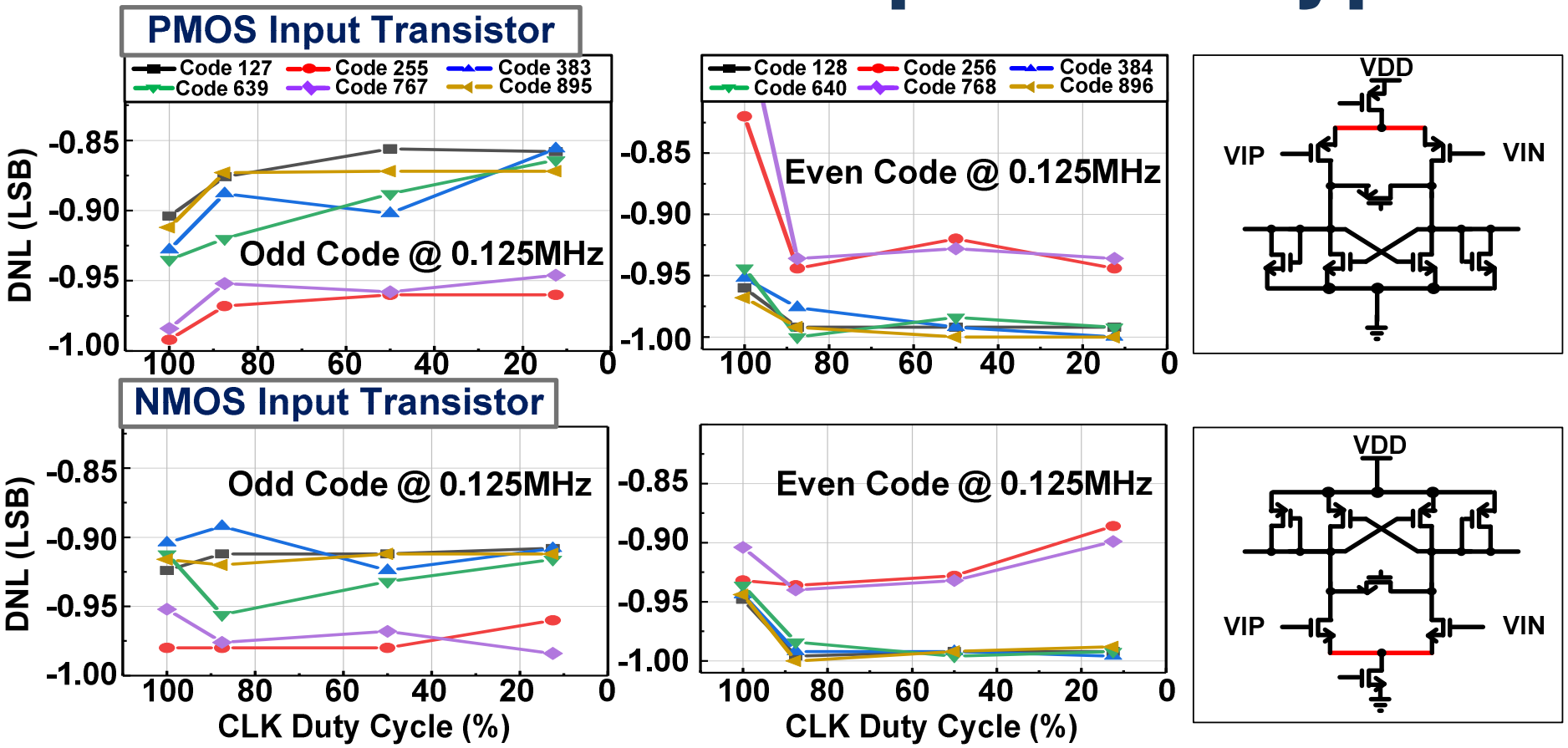
- Shorter duty cycle → shorter BTI stress & longer recovery time
  - DNL increases (or decreases) for odd (or even) vulnerable codes
  - Subtle shift because comparators use IO input devices

10b DNL vs. Clock Frequency



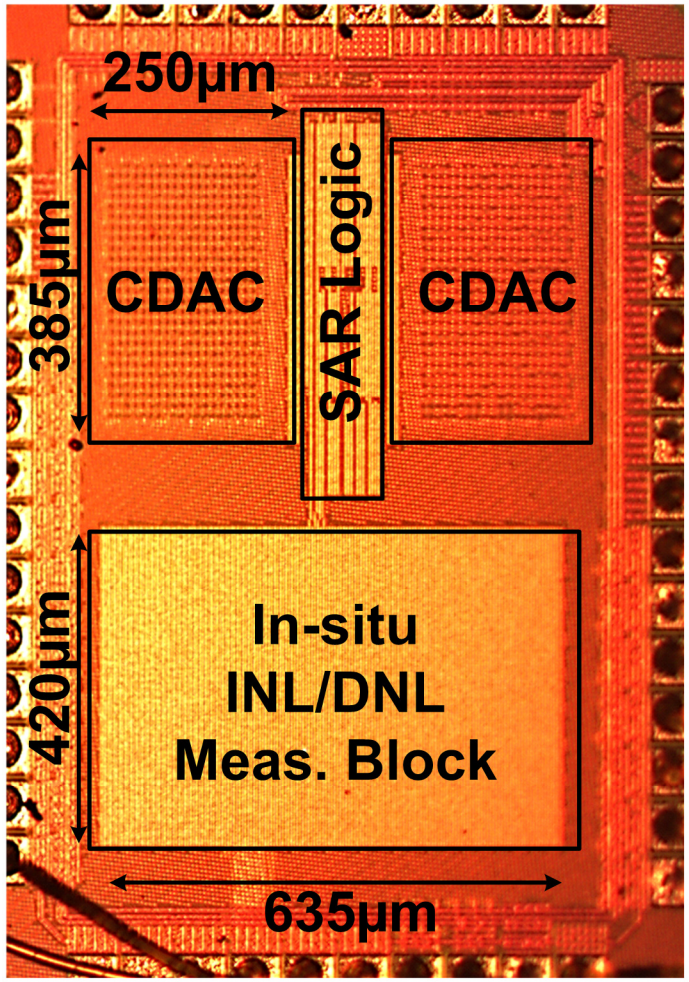
- Short term Vth instability effect less at higher frequencies due to reduced stress time

10b DNL vs. Comparator Type



- Short term Vth instability effect more pronounce for PMOS input comparator

Chip Summary & Die Photo



Process		65nm CMOS
Core / IO supply		1.0V / 2.5V
ADC resolution		10-bit
DNL (max)	vs Con. (w/o SRAM)	0.88 LSB (1.23 LSB improv.)
Read Out Data Volume	vs Con.	1/64 (for 32 samples/code)
Tr. count of on-chip measurement block		94K (Counters only)
DNL		+0.34 / -0.88 LSB @ 1MHz
INL		+1.67 / -1.41 LSB @ 1MHz
Total chip area		0.57mm^2

Conclusion

- Counter based measurement circuit is demonstrated for precise characterization of ADC DNL and INL
- Using the proposed method, short-term BTI is studied in a 10-bit SAR-ADC in 65nm CMOS
- Subtle DNL shifts can be accurately measured using the proposed method

Acknowledgement: Dr. Vijay Reddy and Dr. Srikanth Krishnan at Texas Instruments for their technical feedback. This work was supported in part by the Semiconductor Research Corporation(SRC) and the Texas Analog Center of Excellence (TxACE).