2018 VLSI TECHNOLOGY SYMPOSIUM HONOLULU

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Electromigration Effects in Power Grids Characterized Using an On-Chip Test Structure with Poly Heaters and Voltage Tapping Points

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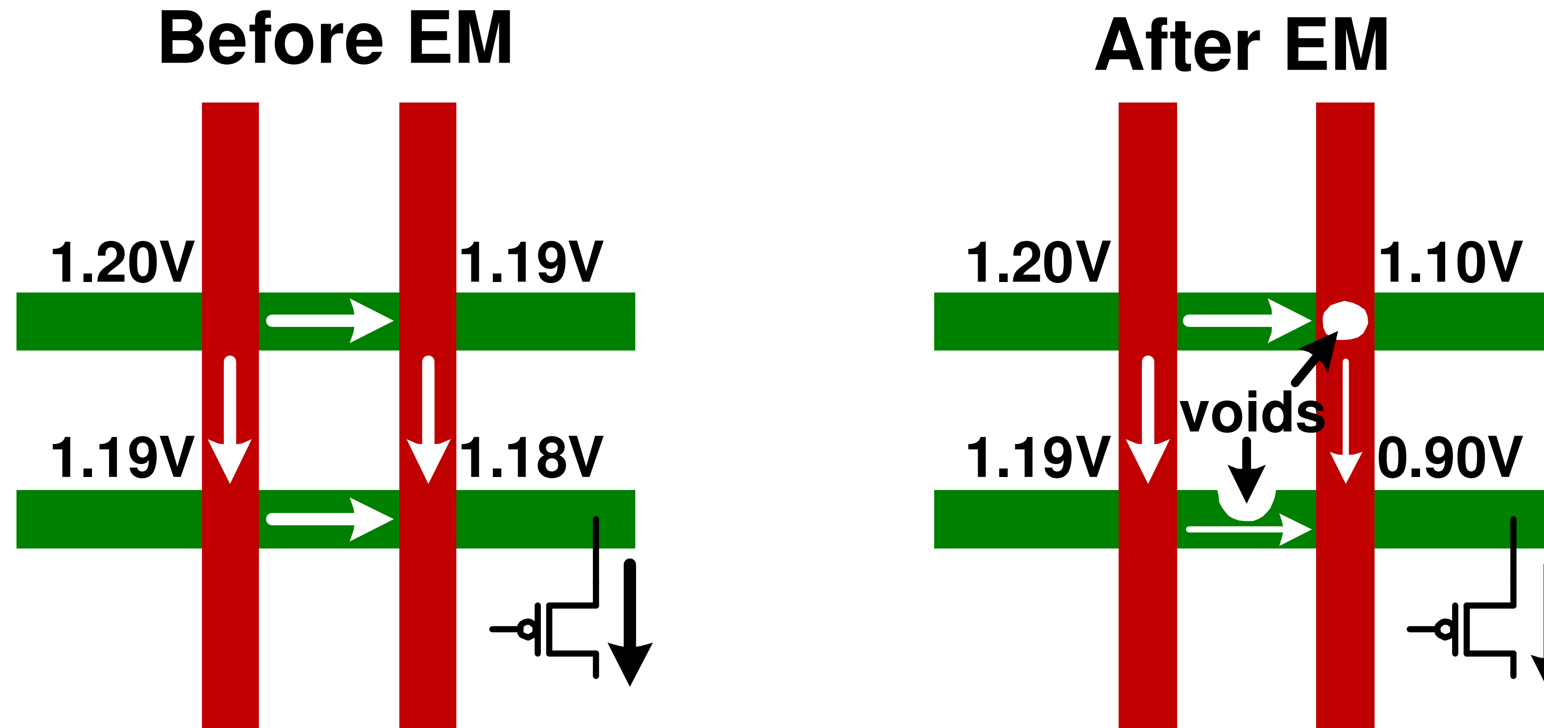
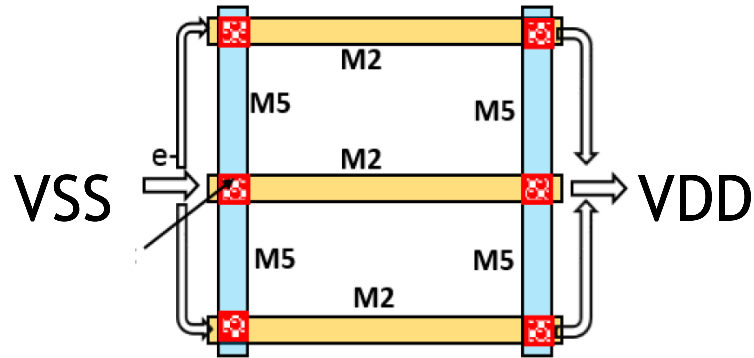
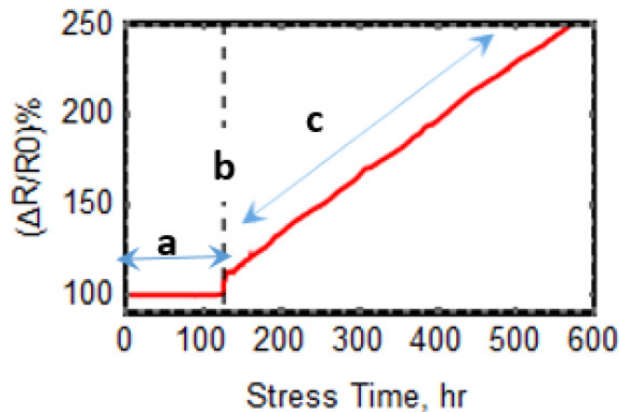
Electromigration (EM) in Power Grid



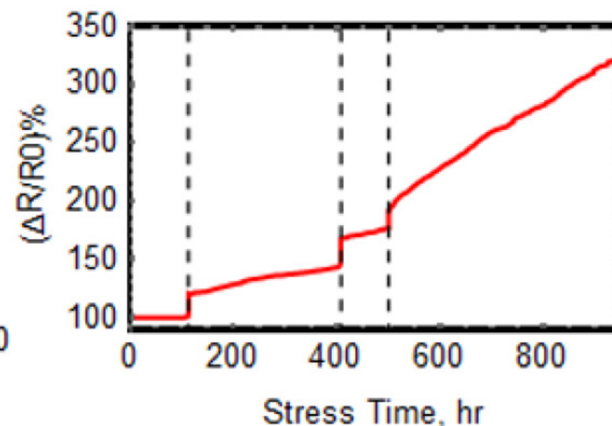
- IR drop increases due to EM in power grid
- Redundant current paths exist in power grid
- Failure time and location hard to track

Previous Work on Power Grid EM





a) Single link EM structure

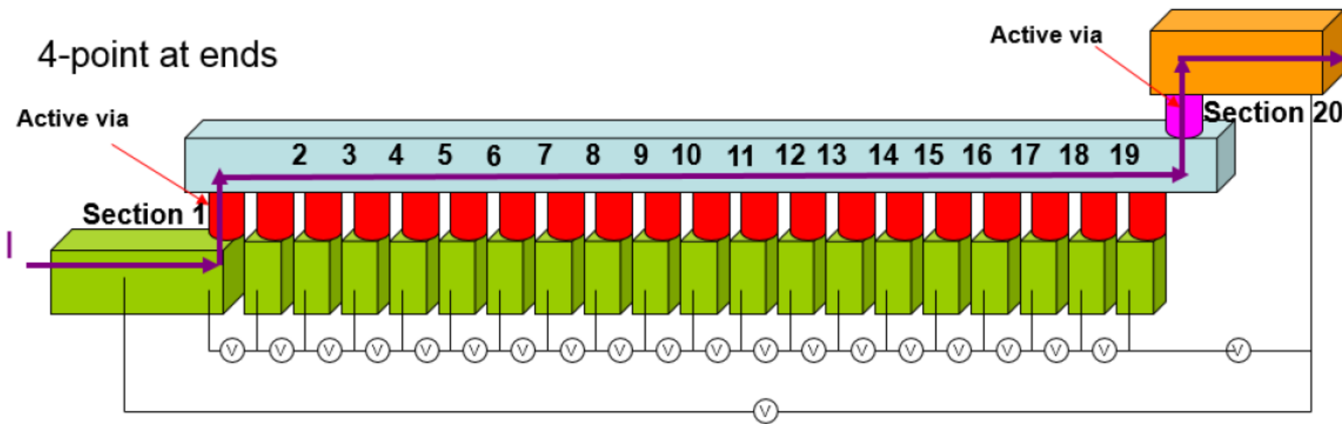


b) Power grid like EM structure (Type II)

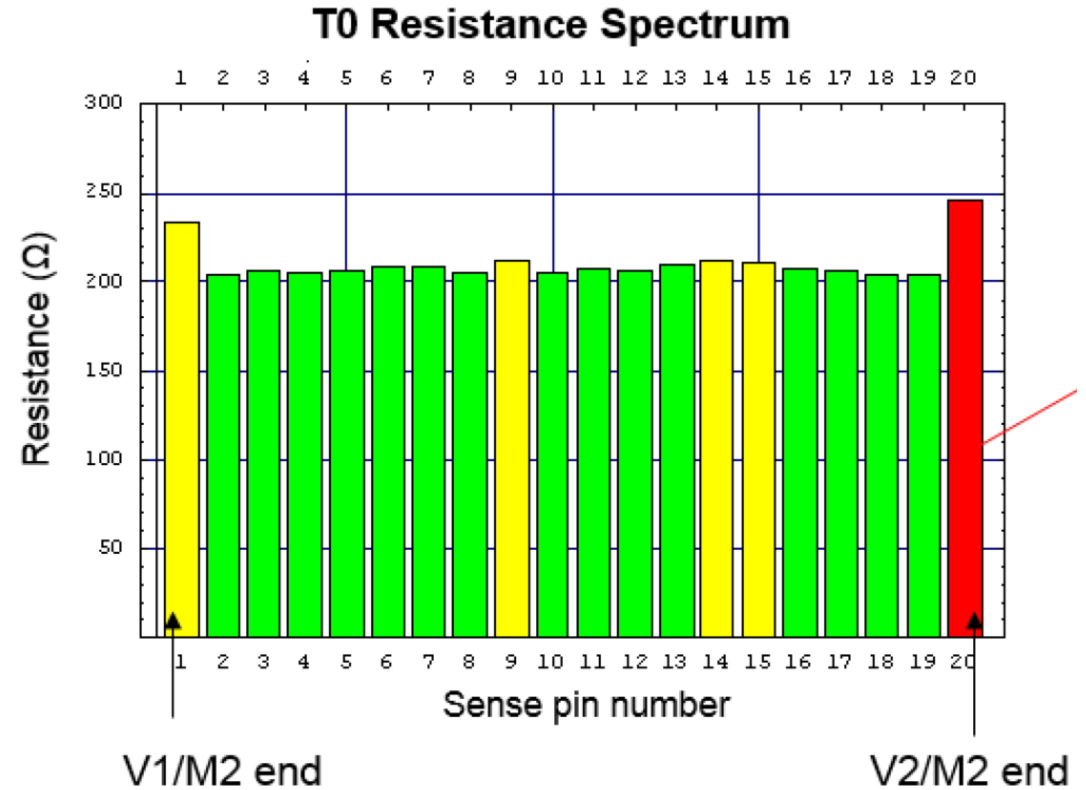
B. Li, IRPS 2018 (IBM)

- Total resistance of 3x2 test structure monitored
- Resistance shifts indicate EM failure events
- Limitation: Simplified structure, failure location can only be pinpointed using SEM, large test area due to pads

Previous Work on Voltage Tapping

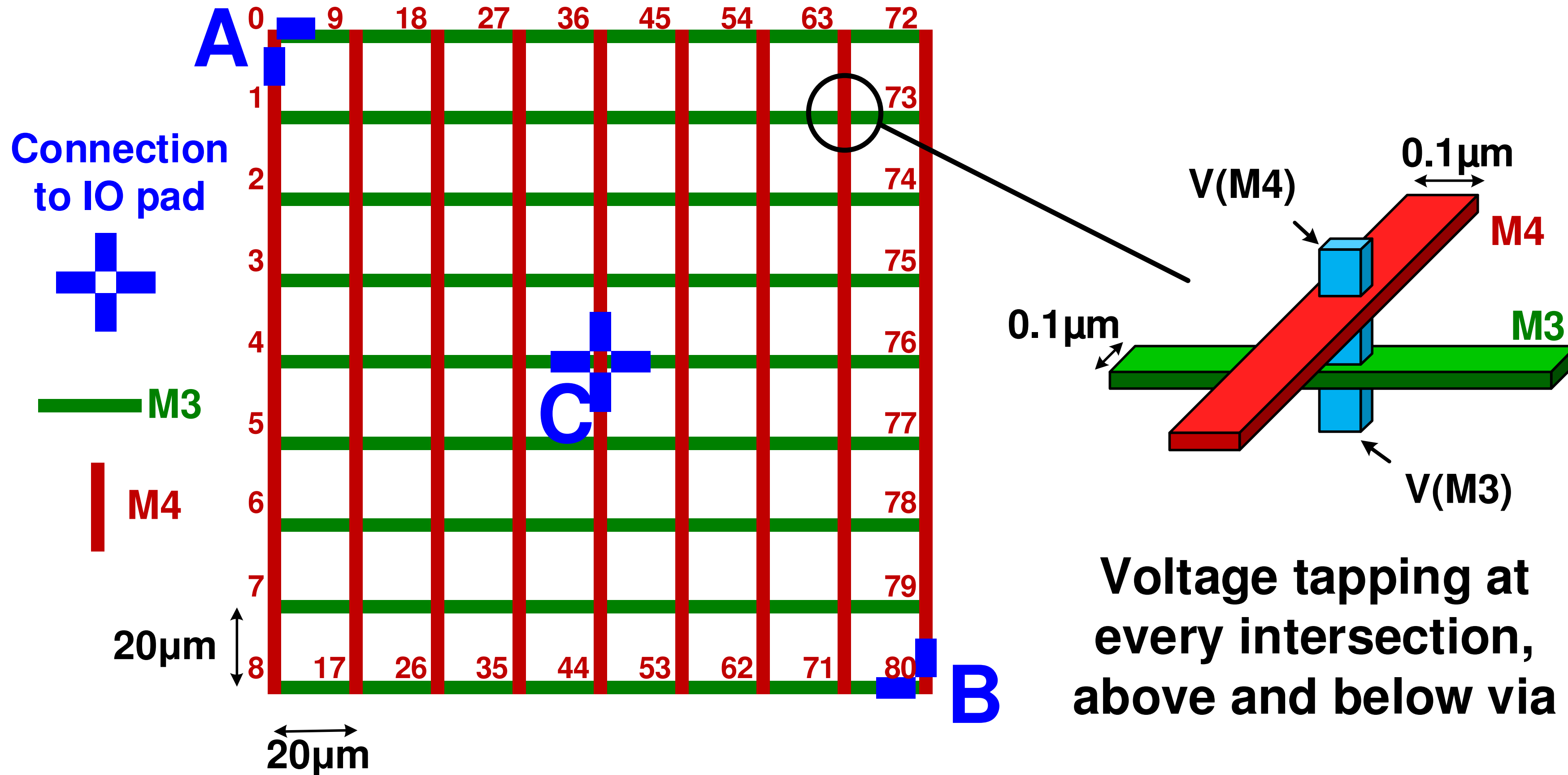


F. Chen, IRPS 2015 (IBM)



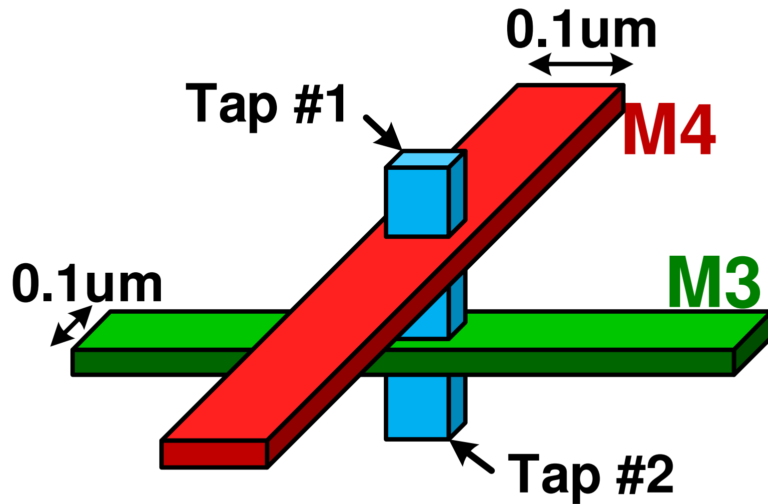
- Via taps enable resistance measurement for each wire segment
- Failure location can be pinpointed based on resistance shift

Proposed Power Grid EM Test Structure

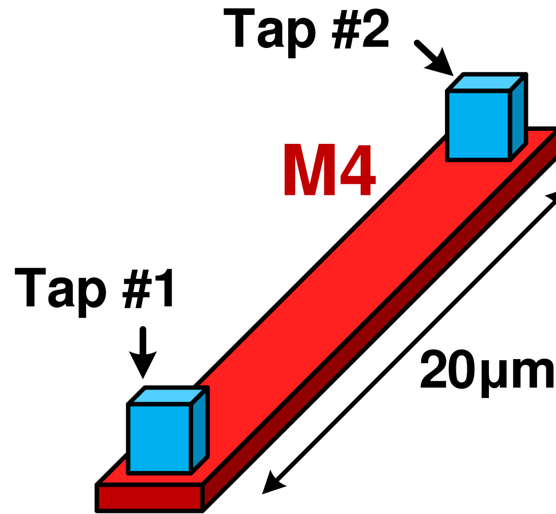


- 9x9 M4-M3 “pseudo” power grid with three voltage connection points (A,B,C)
- Voltage tapping through top and bottom vias

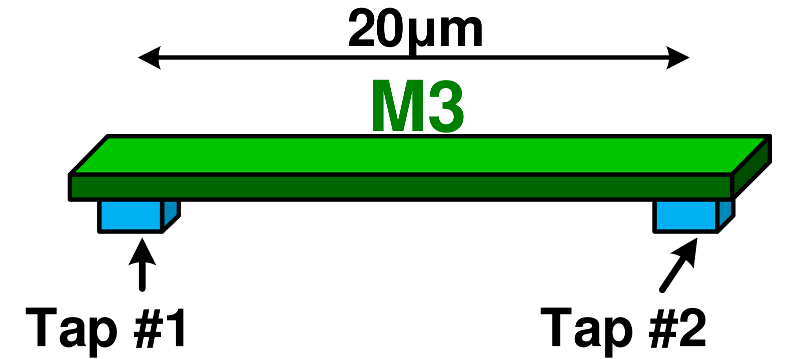
Voltage Drop Across Wire and Via



Via



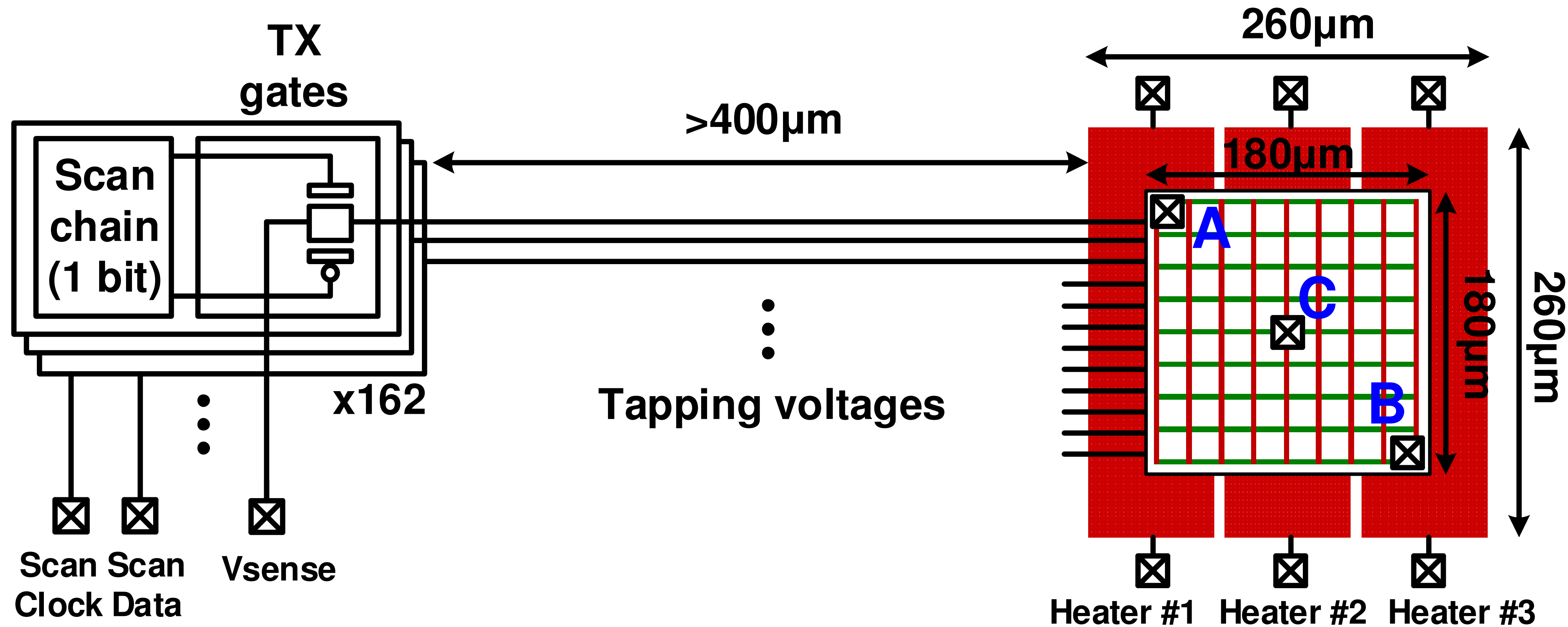
M4 segment



M3 segment

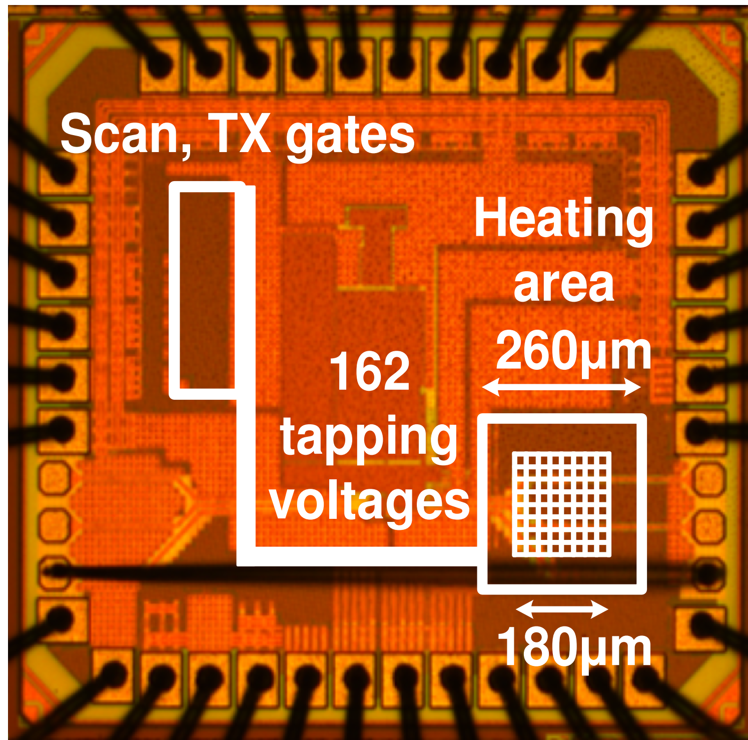
- Voltage drop across each via, vertical and horizontal wire segment measured by voltage tapping

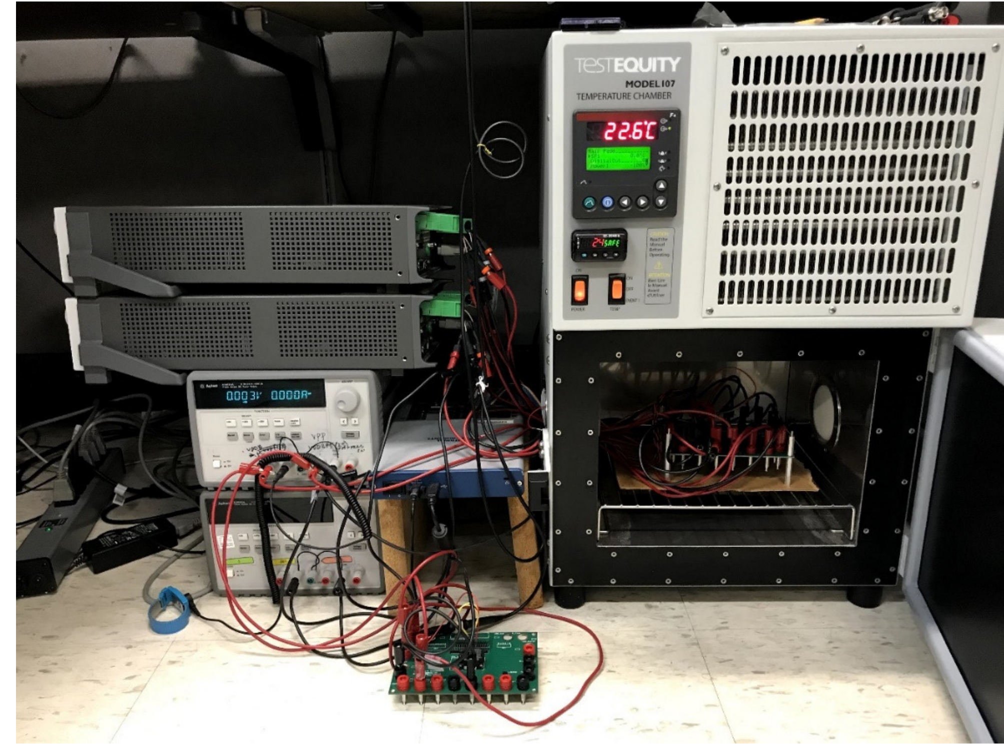
65nm EM Test Chip Overview



- IO device based transmission gates used for on-the-fly voltage tapping
- Circuits >400µm away from heaters to protect from high temp.

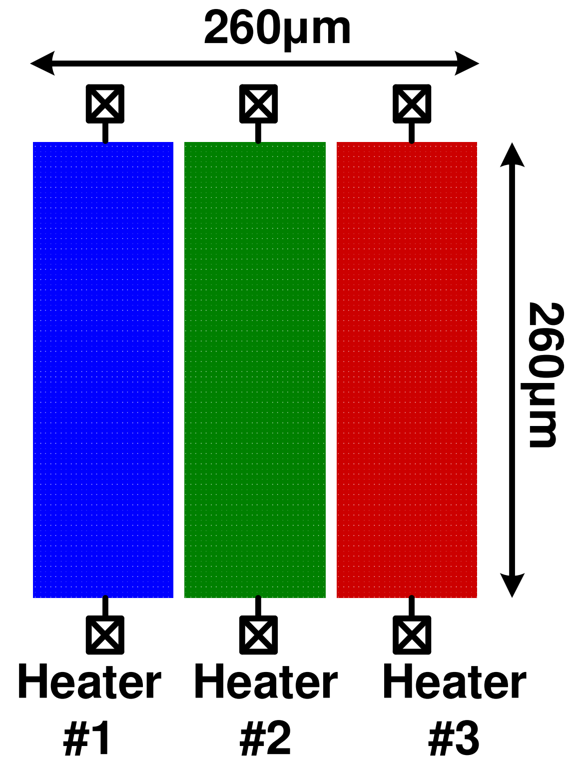
Die Photo and Test Setup

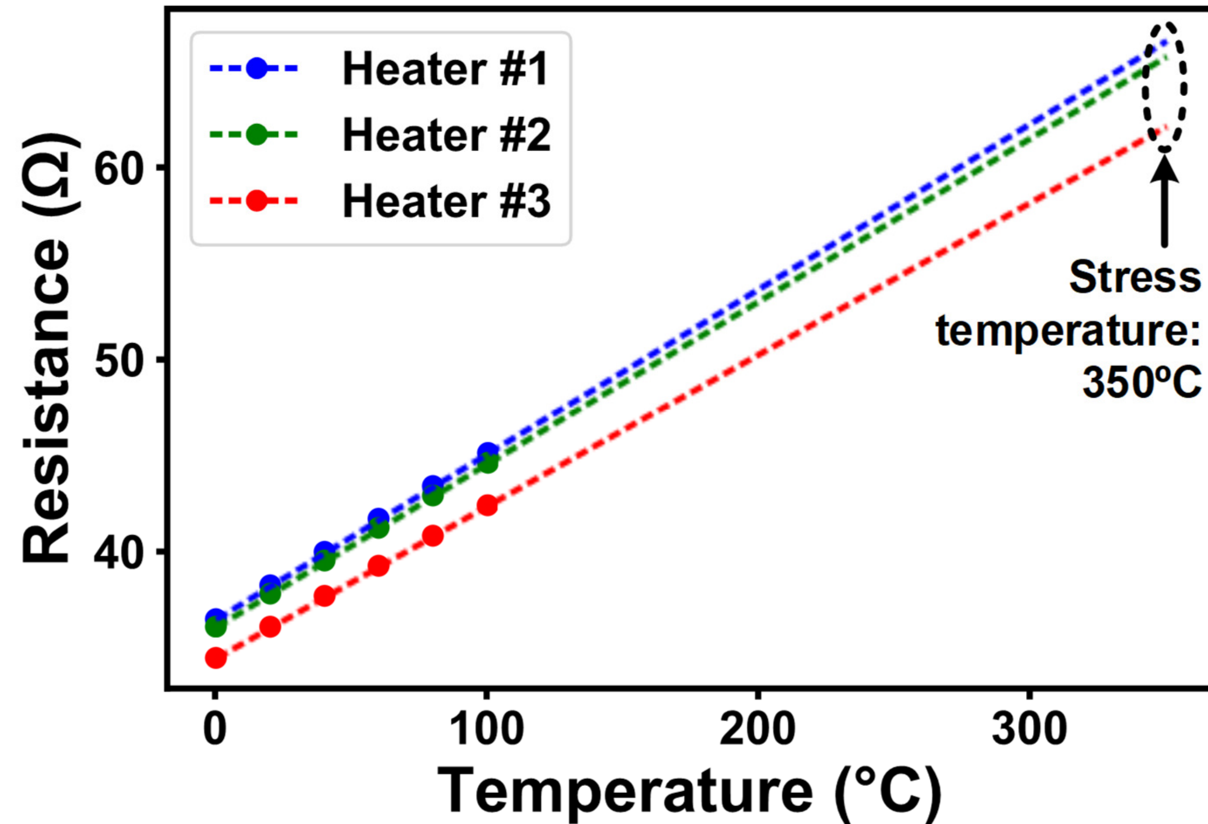




- Temperature chamber:
  - Measure heater TCR before EM test
  - Ambient temperature set to 0 °C to keep control circuits cool during test

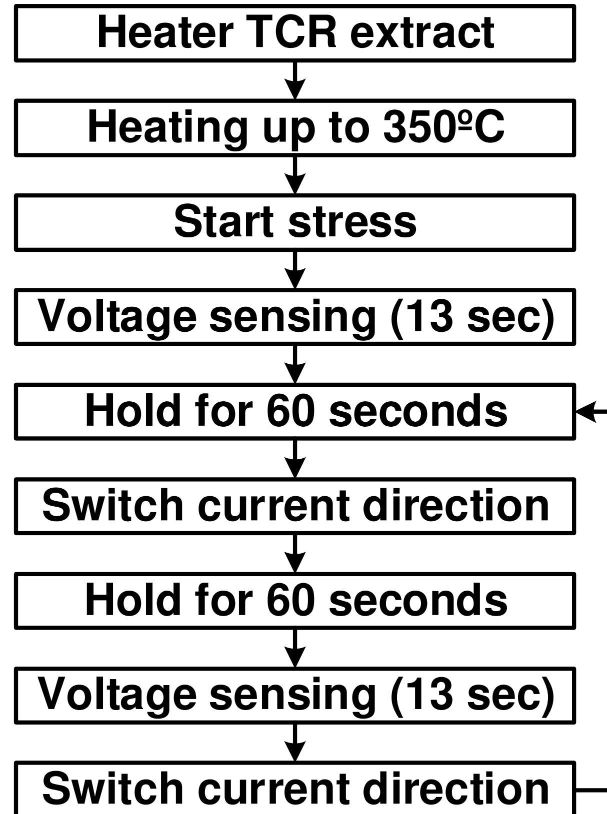
Temperature Coefficient of Resistance (TCR)

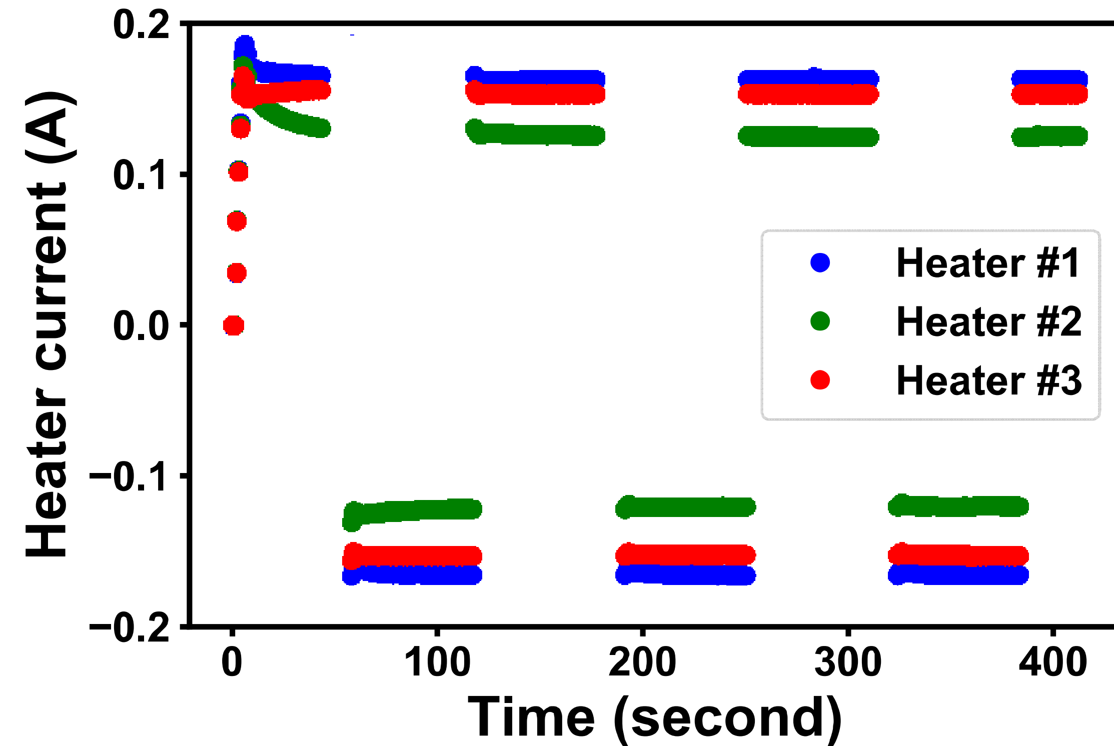




- Excellent linearity between temperature and heater resistances
- Trend lines extended to target stress temperature of 350ºC

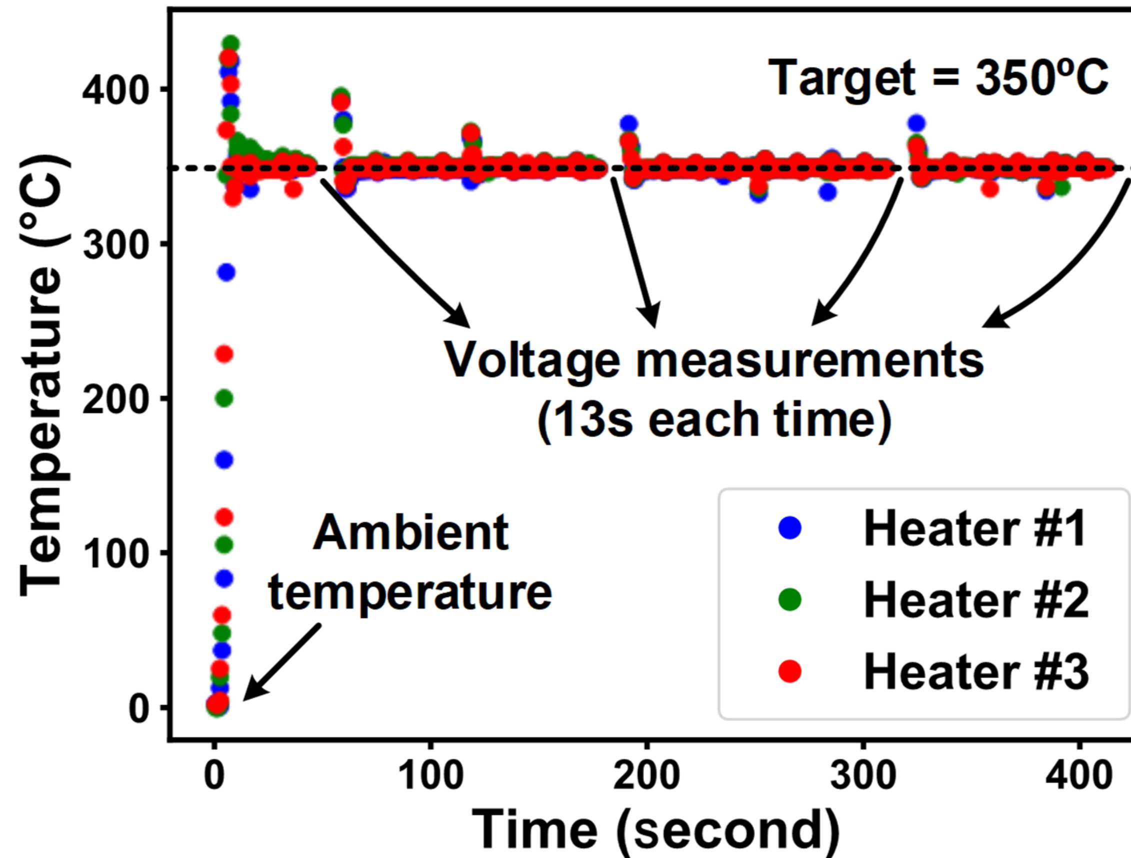
Heater Power Dynamic Control





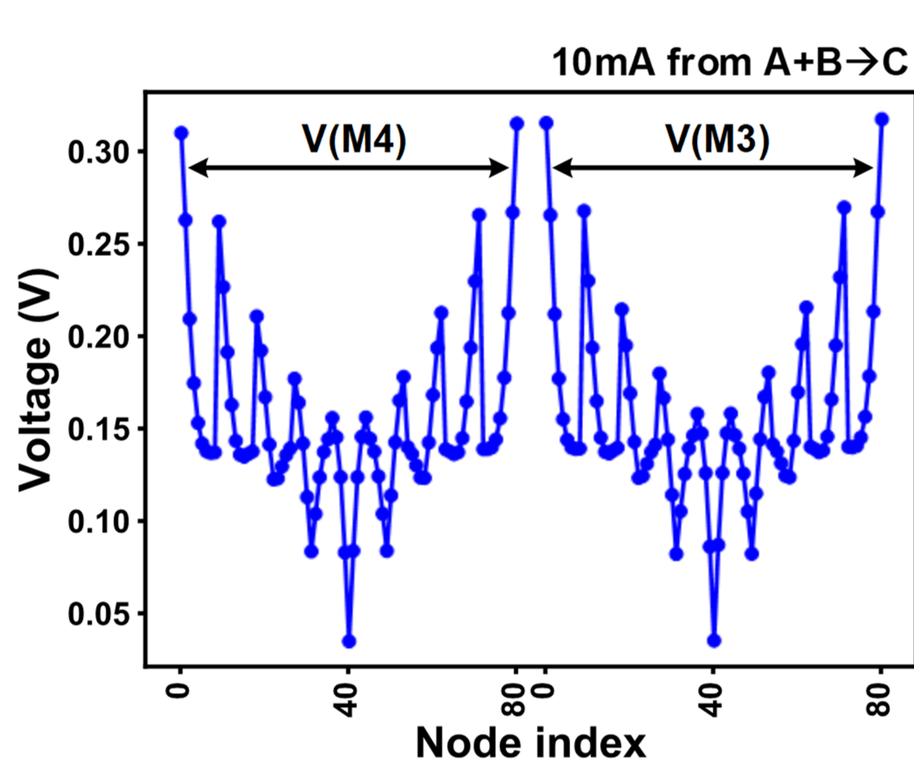
- Heater temperature maintained at 350ºC during measurements
- Heater current direction switched every minute to prevent EM in heaters

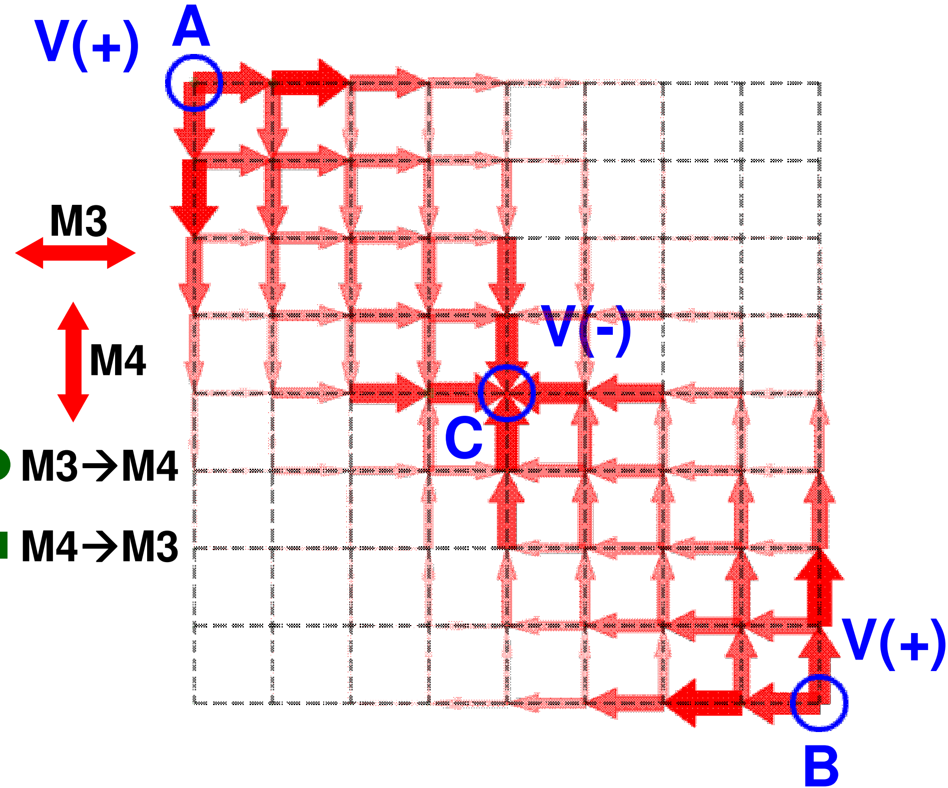
Heater Temperature Log



- Temperature reaches target in seconds compared to minutes in oven
- Control loop adjusts heater current every 0.83 seconds

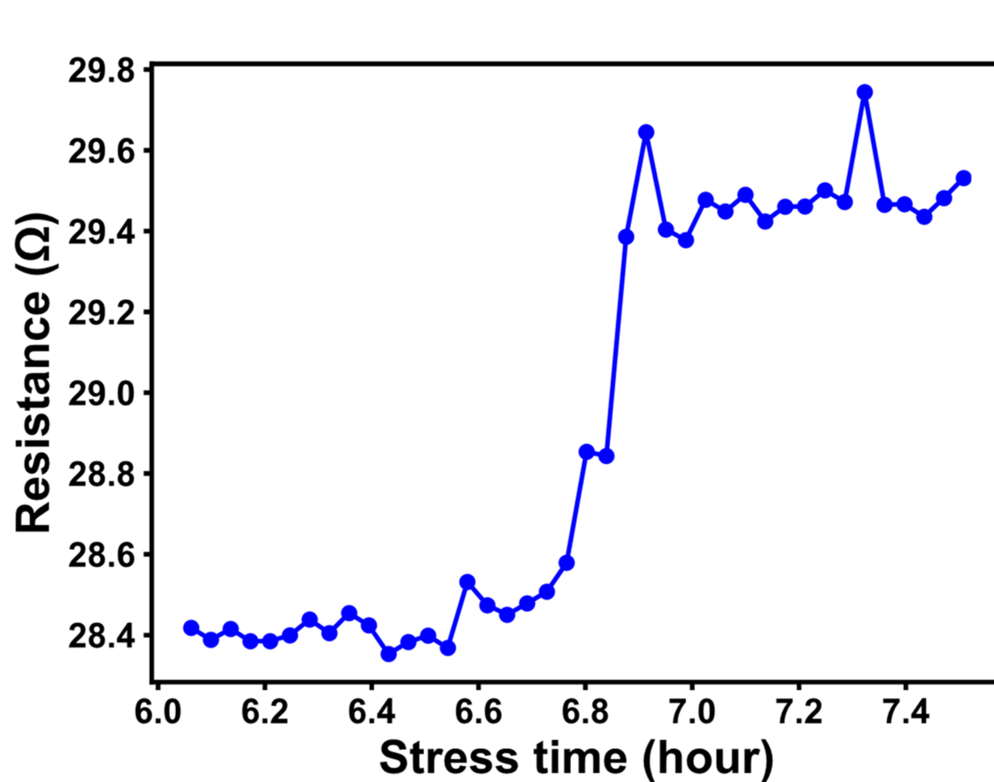
Initial Voltage Map Measurement

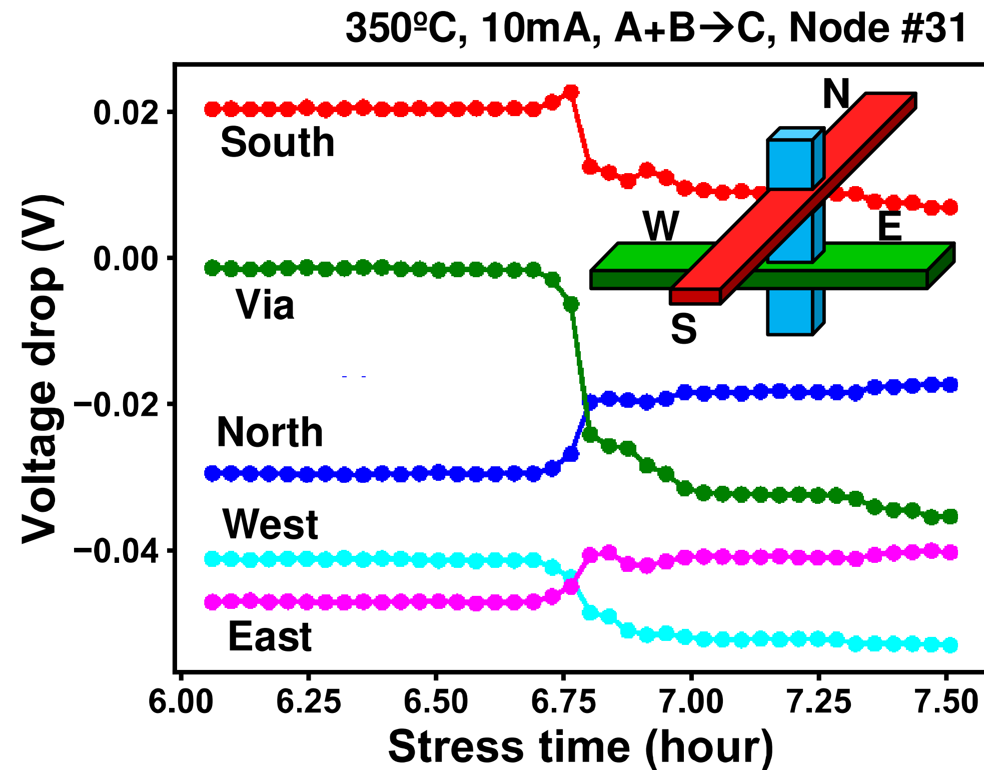


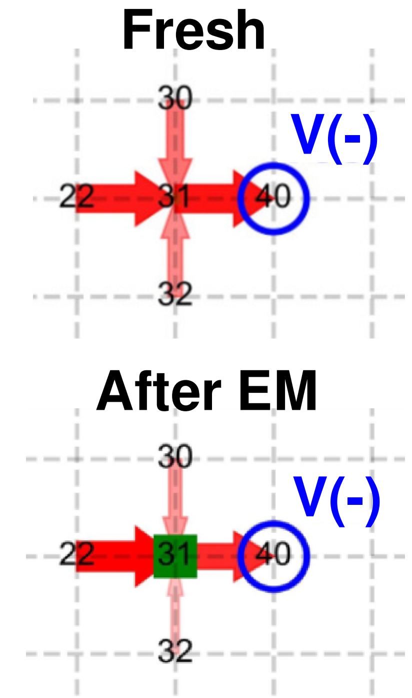


- 162 node voltage samples → voltage drop across entire power grid
- Largest current density near voltage connection points A, B, C

EM Failure Location Analysis

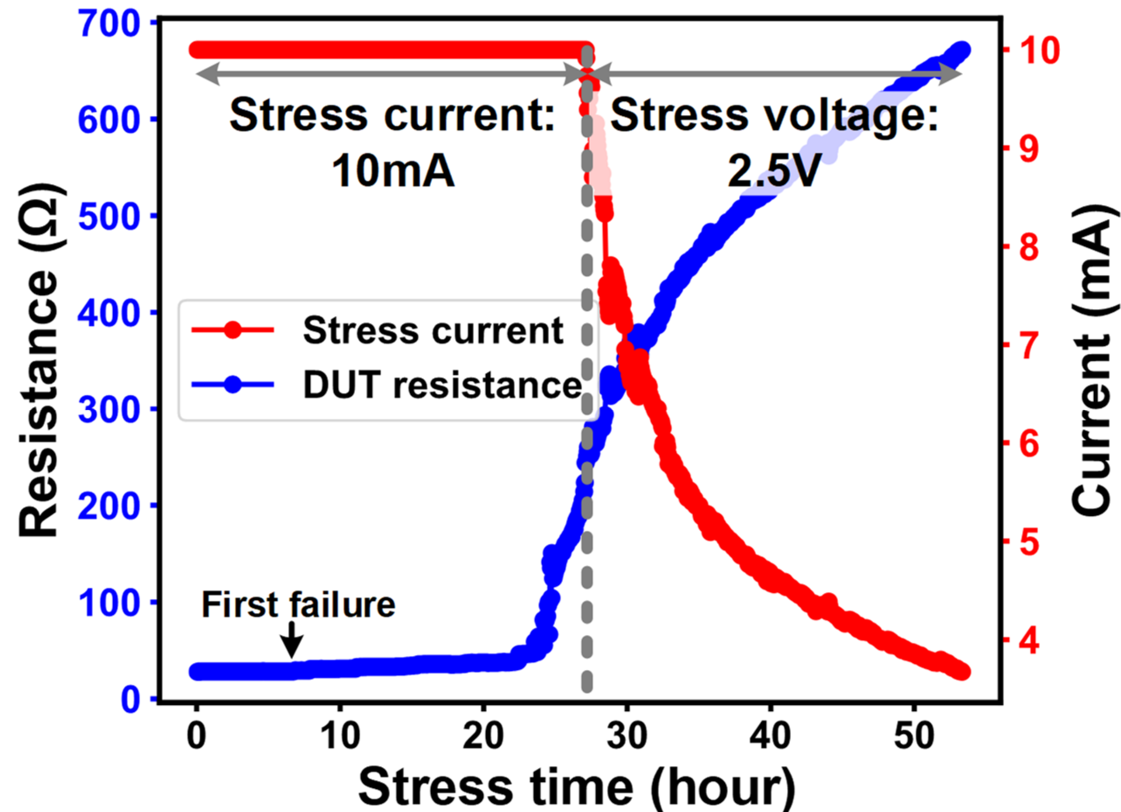


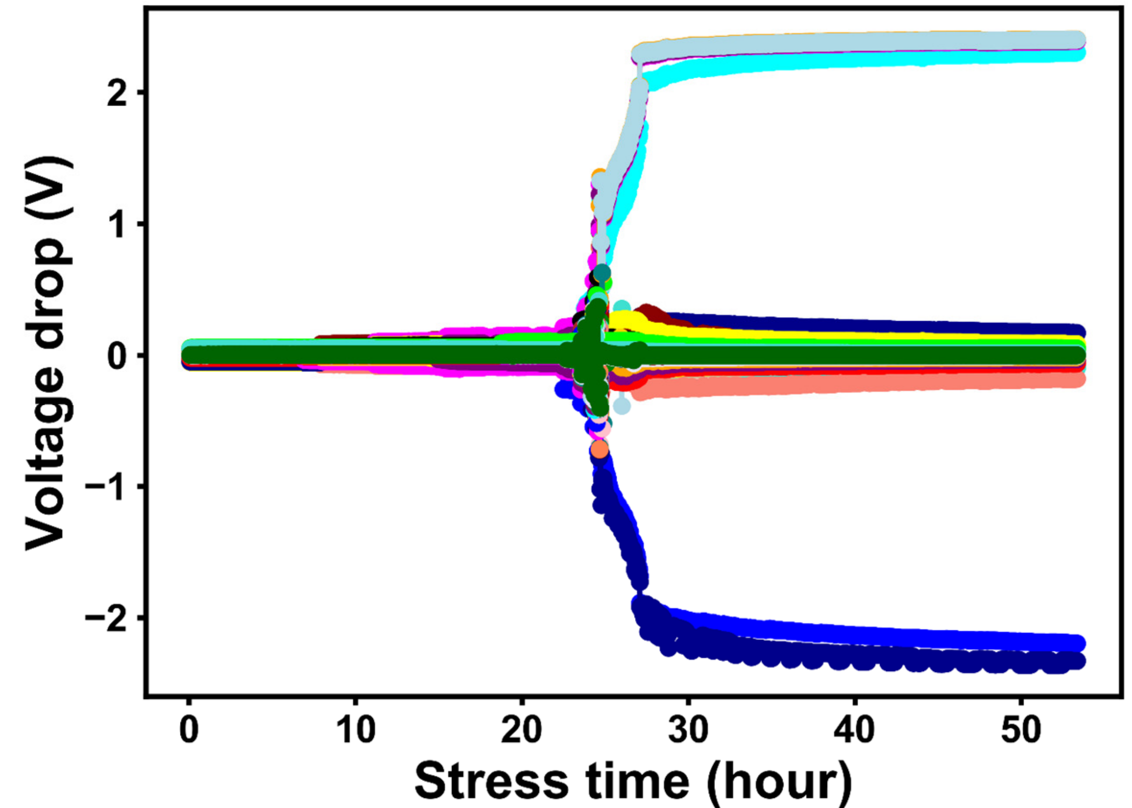




- Largest shift indicates failure location
- Resistance shift not instantaneous (i.e. gradually changes over minutes)

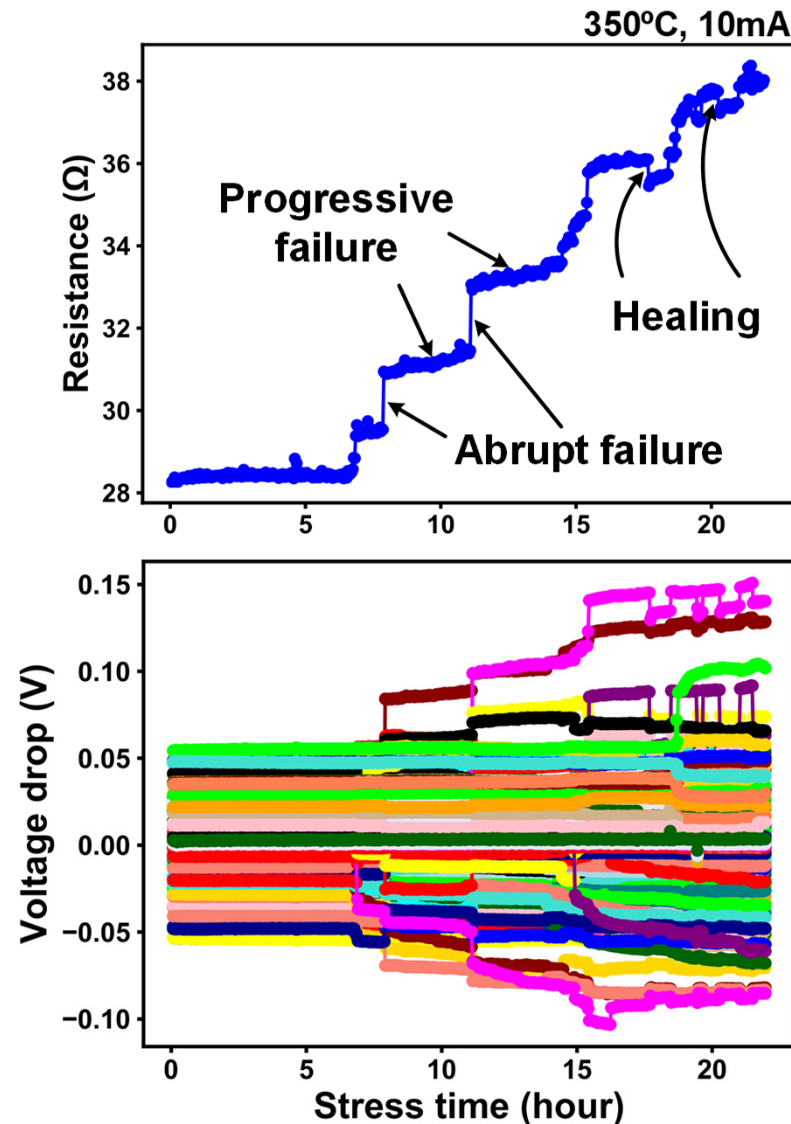
Total Power Grid Resistance and Voltage Drop Traces





- Stress mode: constant current mode → constant voltage mode

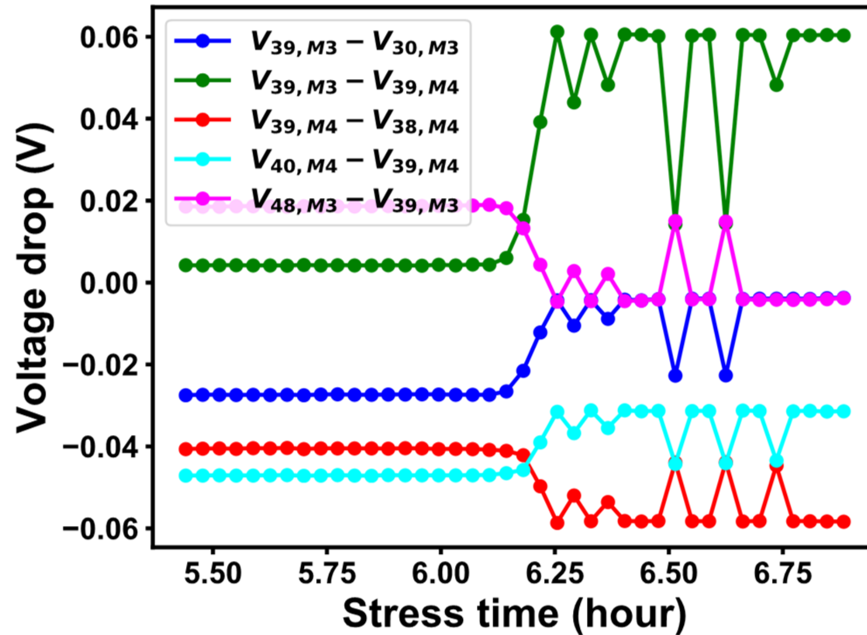
Failure and Healing Types



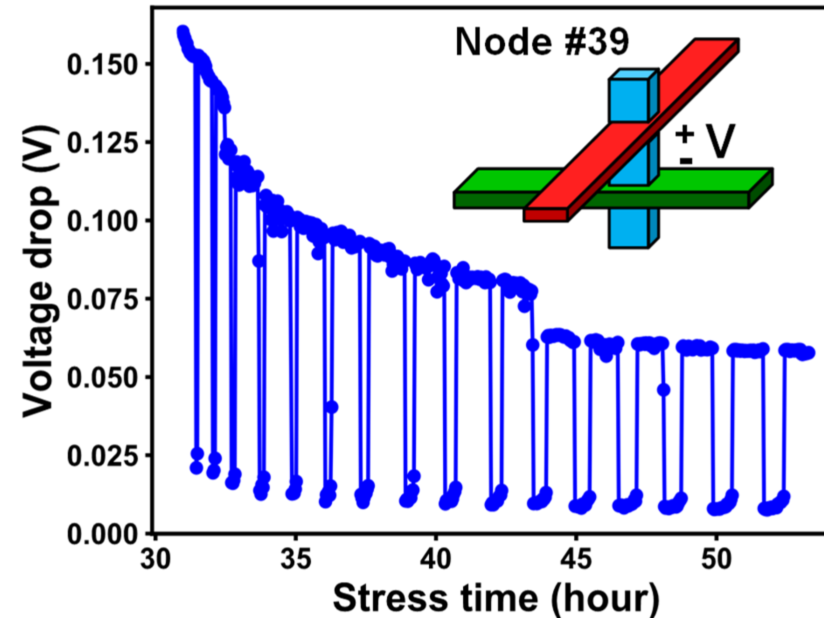
- Both abrupt and progressive failures observed
- Temporary healing also observed:
  - Electromigration
  - Mechanical stress
- Voltage drop traces provide better insight than resistance traces

EM Healing Observations

Chip #8

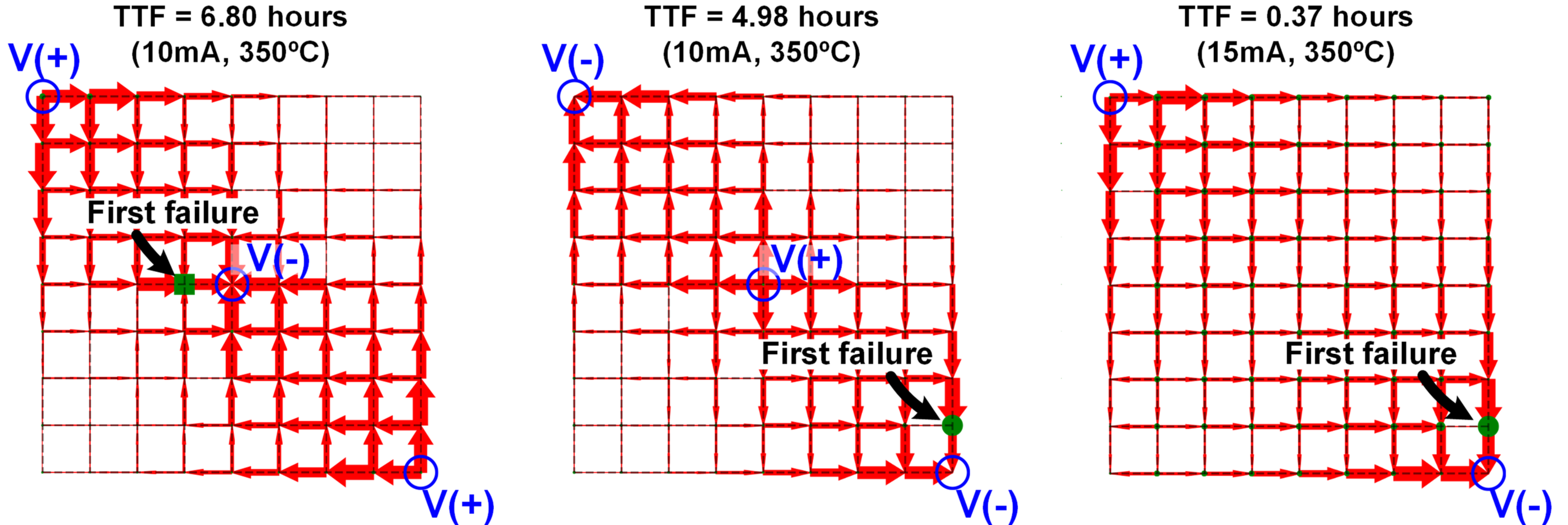


Chip #6



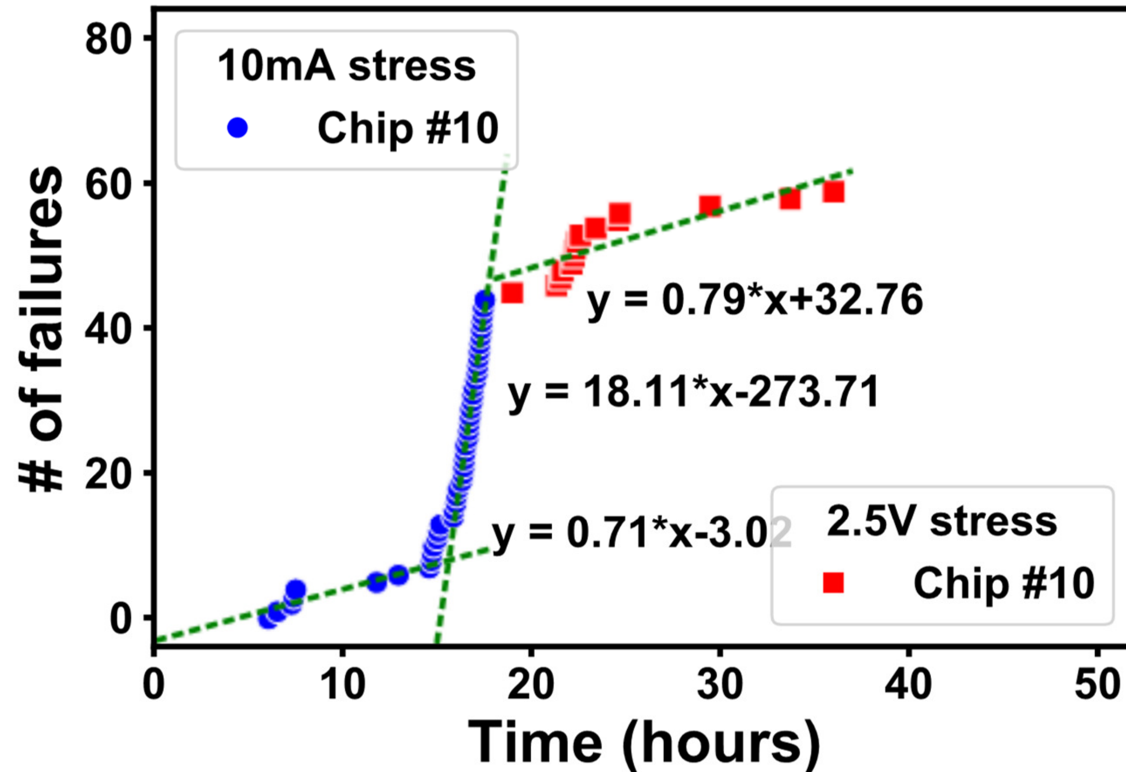
- Voltage fluctuation implies stress and healing cycles
- Healing can happen either early or late
- Redundant current paths believed to be the reason for healing

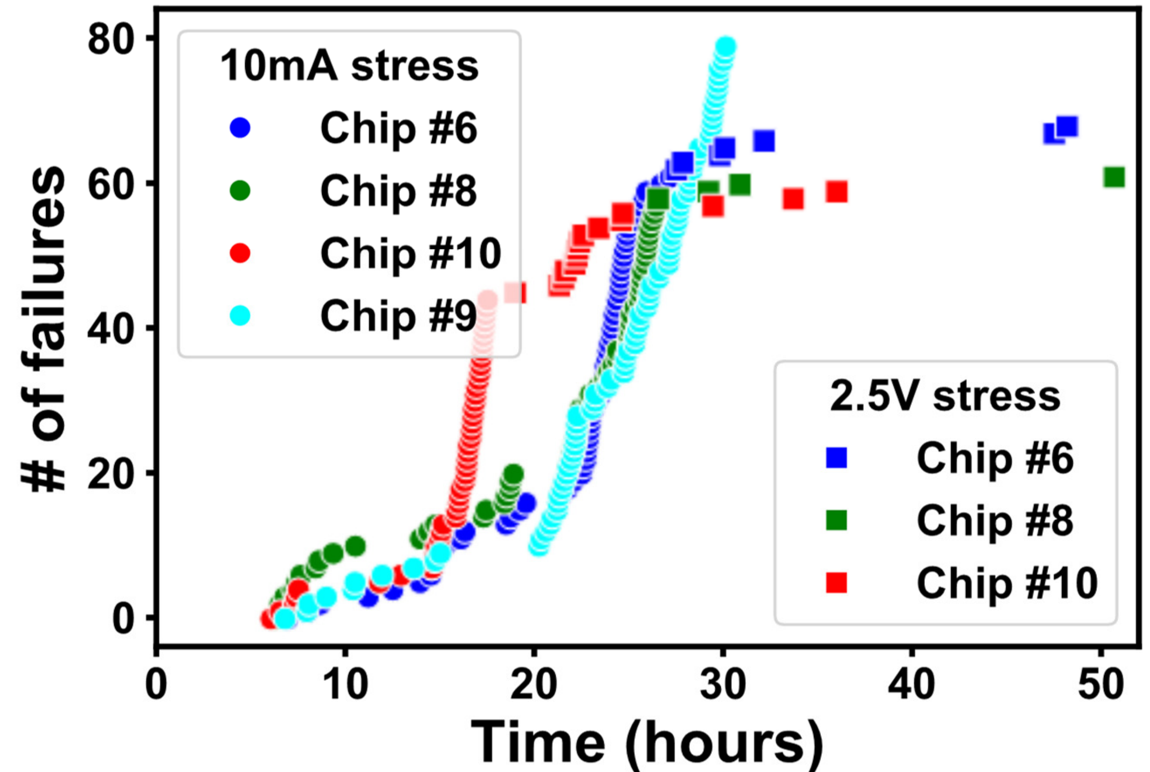
First EM Failure Location



- Three current stress modes applied on multiple chips
- First failure always near negative voltage terminal: EM tensile stress

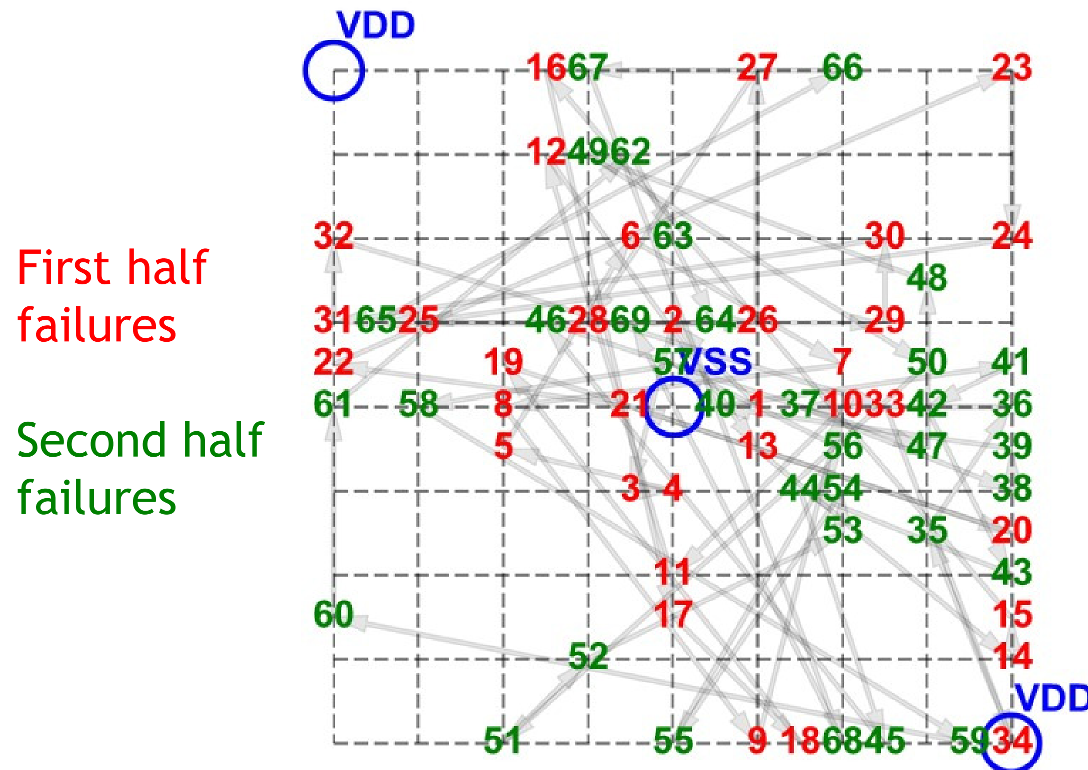
EM Failure Rates





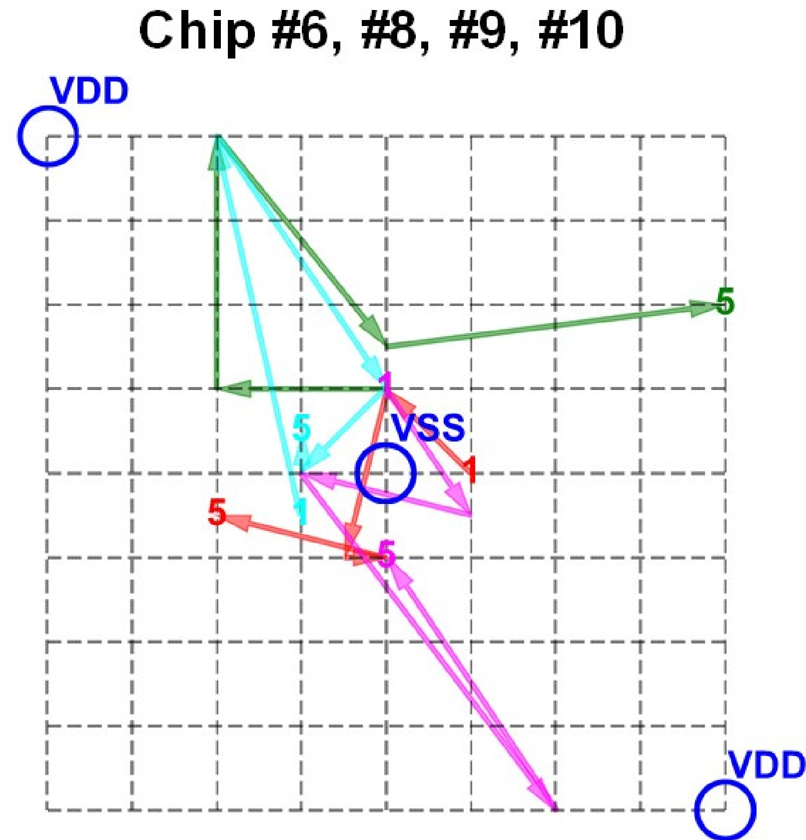
- Constant current phase: slow → fast (due to current density increase)
- Constant voltage phase: failure rate reduces due to less current

Failure Order



- Failures located across entire power grid
- Failure order unpredictable except for the early failures

Failure Order Variation Between Chips



*Only first 5 failure locations shown

- Early failures occur near the negative voltage terminal or edges
- No strong correlation of test data between chips

Summary

- Voltage tapping technique used to tracking real-time EM failures in "pseudo" power grid
- Insights:
  - Early failures occurs at negative voltage terminal or edges of grid
  - Failure rate increases after early failure due to higher current density
  - Healing was repeatedly observed during stress due to redundant current paths
  - Failure order is unpredictable except for early failures
- Suggestions for future EM test chip design:
  - Include both VDD and GND grids
  - More voltage connection points
  - Support different stress modes such as pulsed DC stress