A Fully Integrated Digital LDO With Built-In Adaptive Sampling and Active Voltage Positioning Using a Beat-Frequency Quantizer

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***Abstract*— This paper proposes a fully integrated digital low-dropout (DLDO) regulator using a beat-frequency (BF) quantizer implemented in a 65-nm low power (LP) CMOS technology. A time-based approach, replacing the conventional voltage quantizer by a pair of voltage-controlled oscillator and a time quantizer, makes the design highly digital. A D-flip-flop is utilized as a BF generator, which is used as the sampling clock for the DLDO. The variable sampling frequency in the BF DLDO can achieve fast response, LP consumption, and excellent stability at the same time. In addition to that, the DLDO has a built-in active voltage positioning (AVP) for lower peak-to-peak voltage deviation during load step. The load capacitor is only 40 pF, and the total core area of the DLDO is 0.0374 mm^2. A 50-mA step in load current produces a voltage droop of 108 mV, which is recovered in 1.24 μs. It can operate for a wide input voltage from 0.6 to 1.2 V while generating a 0.4–1.1-V output for a maximum load current of 100 mA. The peak current efficiency is 99.5% and the figure of merit (FOM) is 1.38 ps.**

***Index Terms*— Active voltage positioning (AVP), adaptive sampling, analog-to-digital converter (ADC), low dropout (LDO) regulator, time quantizer, voltage-controlled oscillator (VCO), voltage regulator, voltage-to-time converter.**

I. Introduction

TRADITIONAL analog low-dropout (ALDO) regulators can achieve a fast-transient response and good immunity to droop/overshoot, but their performance degrades at lower operating voltages [1], [2]. The error amplifier design in ALDO is challenging at a very low supply voltage. Also, its gain and bandwidth are sensitive to the process–voltage–temperature (PVT) variations which impact the stability margin and response time. As a result, the implementation of digital LDOs (DLDOs) [3]–[12] is widely explored due to their process scalability, compactness, PVT immunity, and easy programmability for design optimization. A DLDO replaces the analog amplifier by a voltage quantizer followed by a digital control block, as shown in Fig. 1. The voltage quantizer generates a digital code (N_{OUT}) proportional to the voltage error; i.e., $V_{REF} - V_{LDO\_OUT}$. The output stage consists of an array of PMOS transistors operating as switches driven by the digital control. Since the transistors operate in the triode region, the voltage headroom requirement is small.

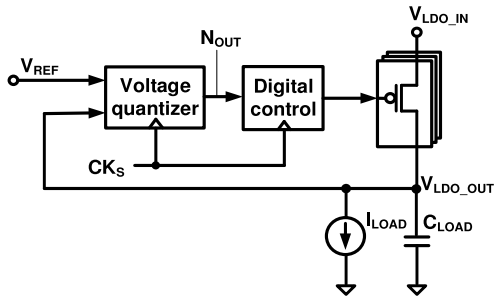

Fig. 1. Block diagram of a conventional voltage quantizer-based DLDO. The LDO output voltage is compared with the reference voltage by a 1-bit voltage quantizer.

The most common architecture for DLDO is using a voltage comparator as a 1-bit quantizer followed by a series of shift registers [3], [4], [9]–[11]. This enables a simpler design and lowers quiescent current (I_Q). However, such a bang–bang control requires many clock cycles to reach a steady state, as the loop is updated by a fixed step in every cycle. Using a higher clock frequency (f_s) for loop sampling is the only solution to improve the transient response, but this comes at a large cost in power consumption. In addition to that, increasing f_s moves the open-loop pole closer to the unit circle in the discrete or z-domain causing stability issues [4]. Therefore, the multi-bit voltage quantizer or analog-to-digital converter (ADC) is used in recent studies [5]–[7] for faster response by directly quantizing the output voltage error. Higher ADC resolution improves the response time, as it

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requires fewer clock cycles to resolve the error. However, the design complexity, the power consumption, and the area overhead associated with a high-resolution ADC at sub-1-V supply are the primary limiting factors. Moreover, the maximum value of f_s is dictated by the ADC resolution.

In order to address the tradeoff among response time, stability, and power consumption, different adaptive design techniques are incorporated. However, each of these techniques has its own drawback. For example, Nasir *et al.* [4] utilize multiple voltage-controlled oscillators (VCOs) operating simultaneously for sampling clock generation. However, it requires an additional detection circuit and control logic to enable the appropriate VCO depending on the output droop/overshoot. The latency of this detection circuit also limits the response time. A coarse-fine dual control scheme is presented in [5] and [11]. This approach also requires a detection circuit and a control state machine that increases the complexity while limiting the DLDO performance. Similarly, [7] and [13] involve an event-driven complex controller and a continuous-time 7-bit ADC.

In this paper, a time-quantizer-based DLDO is implemented using a VCO pair [12]. A phase-locked DLDO is proposed in [14] using a pair of VCO as well, but only the rising edges are compared using a binary phase detector. Therefore, this is also a 1-bit quantizer similar to the voltage comparator-based implementation mentioned earlier but implemented in a time domain. On the contrary, in this paper, the entire VCO period is quantized which provides a digital high-resolution ADC design solution, and the VCO phase quantization provides a first-order quantization noise shaping to improve the resolution without any added complexity. The proposed beat-frequency (BF)-based time-quantizer implementation enables adaptive control of f_s depending on the amount of voltage droop or overshoot in $V_{\mathrm{LDO\_OUT}}$. Higher f_s during droop or overshoot helps for faster recovery and eventually settles to a lower value in a steady state reducing the power consumption with excellent stability. In other words, for a given droop or overshoot and settling time, the load capacitor can be significantly scaled down reducing the form factor. Moreover, a steady-state voltage offset introduces active voltage positioning (AVP), which is an efficient technique for the reduction of peak-to-peak voltage deviation.

The remainder of this paper is organized as follows. The details of the proposed time quantizer-based DLDO is described in Section II. The AVP technique is illustrated in Section III. The small-signal model and loop stability analysis are performed in Section IV, followed by the circuit implementation details in Section V. Section VI summarizes the test-chip measurement results, and Section VII concludes this paper.

II. Proposed Time-Based Digital LDO

A time-based DLDO, as shown in Fig. 2, uses a pair of VCOs and a time quantizer instead of a voltage quantizer [12], [16]. The VCOs convert the reference and the output voltages V_{REF} and $V_{\mathrm{LDO\_OUT}}$ to equivalent clocks $\mathrm{CK_{REF}}$ and $\mathrm{CK_{OUT}}$ of proportional frequencies f_{REF} and f_{OUT}. The time

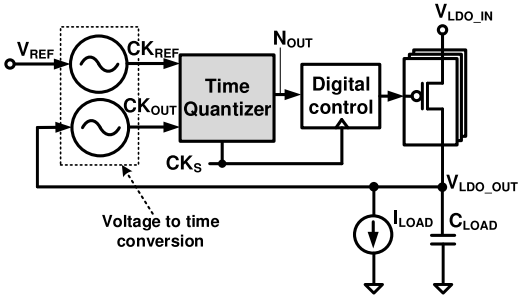


Fig. 2. Simplified block diagram of a time-based DLDO. The voltage quantizer in the ALDO is replaced with a pair of VCO and a time quantizer, making the overall implementation digital intensive.

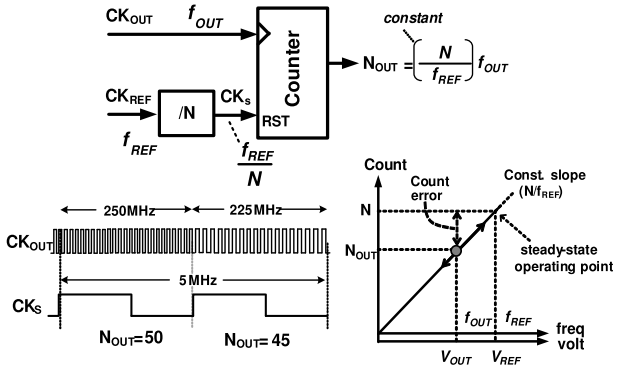


Fig. 3. Conventional linear time quantizer. A fixed sampling clock frequency makes the output count N_{OUT} proportional to f_{OUT} or V_{OUT}.

quantizer generates digital code (N_{OUT}) as a function of input frequencies. The digital control block compares N_{OUT} with the desired value (N) and the error $N - N_{\mathrm{OUT}}$ is accumulated and canceled by switching on/off the PMOS array elements that adjust $V_{\mathrm{LDO\_OUT}}$. The operation is similar to a frequency-locked loop (FLL) where $\mathrm{CK_{REF}}$ acts as the reference clock for the FLL to lock the frequency of $\mathrm{CK_{OUT}}$. This effectively makes $V_{\mathrm{LDO\_OUT}}$ follow V_{REF}. The time quantizer plays a critical role since its speed and resolution directly impact the DLDO performance. The design of a conventional linear time quantizer and the proposed BF quantizer are explained in Sections II-A and II-B.

A. Conventional Linear Time Quantizer

A time quantizer is conventionally implemented by counting the signal clock ($\mathrm{CK_{OUT}}$) edges for a fixed time duration generated by the sampling clock (CK_s) [15]. Fig. 3 explains the operation. The frequency of a reference oscillator is divided by a factor N to create CK_s, i.e., $f_s = f_{\mathrm{REF}}/N$. The output count can be expressed as

$$N_{\mathrm{OUT}} = \frac{f_{\mathrm{OUT}}}{f_s} = N\frac{f_{\mathrm{OUT}}}{f_{\mathrm{REF}}}. \tag{1}$$

Since the VCO voltage-to-frequency conversion provides a gain K_{VCO}, N_{OUT} is proportional to the signal voltage (V_{OUT}) or VCO frequency (f_{OUT}), generating a linear input-to-output transfer function. As shown in the example, if f_s is 5 MHz, 250- and 225-MHz $\mathrm{CK_{OUT}}$ generate N_{OUT} of 50 and 45, respectively. At steady state, when two VCOs operate at the

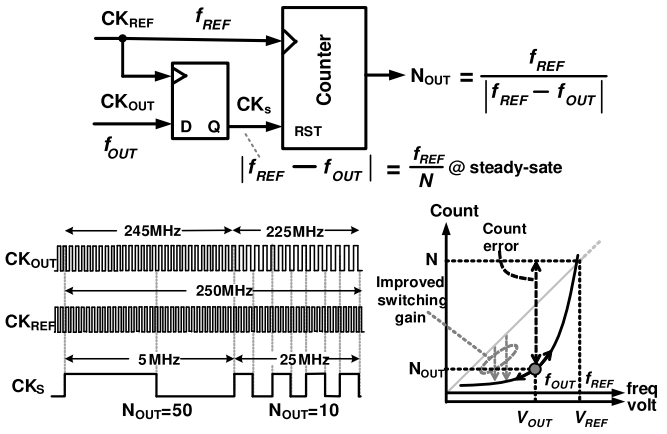


Fig. 4. Proposed BF-based time quantizer. Sampling frequency is proportional to the voltage error that results a non-linear transfer characteristic.

same frequency, we get $N_{\rm OUT} = N$. However, during droop or overshoot, any change in $f_{\rm OUT}$ changes $N_{\rm OUT}$ proportionally and the count error ($N - N_{\rm OUT}$) decides the number of PMOS switches need to be turned on/off to mitigate the voltage error ($V_{\rm REF} - V_{\rm OUT}$). Since two VCOs are identical in design and layout, the frequency variation over PVT will be similar on both. This greatly reduces the PVT sensitivity of the quantizer as $N_{\rm OUT}$ relies on the $f_{\rm OUT}/f_{\rm REF}$ ratio. Here, one thing to note is that higher N increases the slope of the transfer characteristic and improves the ADC resolution; this simultaneously makes $\rm CK_s$ slower increasing the response time.

B. Proposed Beat-Frequency Time Quantizer

In order to break the tradeoff between the speed and the resolution of the linear time quantizer, a BF-based implementation is proposed in this paper. One important thing to note is that high quantizer resolution is required only in the steady state to generate a precise output voltage, whereas higher f_s helps during any transient change in DLDO operation. The proposed BF quantizer takes complete advantage of it by making f_s high at the cost of degraded resolution but only during transient droop or overshoot. While in the steady state, lower f_s ensures high quantizer resolution.

A standard D-flip-flop is utilized as a digital frequency subtractor or BF generator [17]–[19], as shown in Fig. 4. To illustrate the operation better, let us assume $\rm CK_{REF}$ is 250 MHz and $\rm CK_{OUT}$ is 245 MHz, i.e., 2% lower than $\rm CK_{REF}$. If we sample $\rm CK_{OUT}$ by $\rm CK_{REF}$ using a D-flip-flip, it takes 50 cycles of $\rm CK_{REF}$ to cover the entire $\rm CK_{OUT}$ period and comes back to its initial sampling point. Therefore, the D-flip-flop output will generate a clock, $\rm CK_s$ of frequency 250 MHz/50 = 5 MHz, which is the absolute frequency error between $\rm CK_{REF}$ and $\rm CK_{OUT}$, i.e., $f_s = |f_{\rm REF} - f_{\rm OUT}|$. Counting the number of edges of $\rm CK_{REF}$ within one period of $\rm CK_s$ results an output count ($N_{\rm OUT}$) of 50. When $\rm CK_{OUT}$ drops to 225 MHz, f_s jumps to 25 MHz and $N_{\rm OUT}$ becomes 10. This BF relationship holds when $f_{\rm OUT}$ remains within the range 0.5 $f_{\rm REF}$ to 1.5 $f_{\rm REF}$. This can be easily ensured by designing the VCOs with a small tuning range.

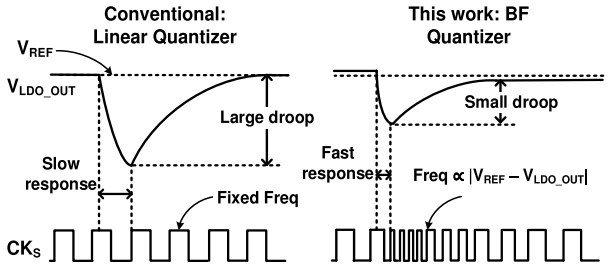


Fig. 5. Transient response of the linear and the BF DLDO. Adaptive sampling provides faster DLDO response and lower droop.

Now, if we look at the input frequency (or voltage) to the output count transfer characteristic, it is no longer linear and the expression is as follows:

$$N_{\rm OUT} = \frac{f_{\rm REF}}{f_s} = \frac{f_{\rm REF}}{|f_{\rm REF} - f_{\rm OUT}|}. \tag{2}$$

Using $\rm CK_s$ as the DLDO sampling clock can provide adaptive control of loop response depending on the amount of voltage transients. During voltage droop or overshoot, the frequency error increases which translates into a higher f_s and hence a faster response. However, under the steady-state condition, when $N_{\rm OUT} = N$, f_s settles to $f_{\rm REF}/N$, i.e., same as linear quantizer case while creating a fixed voltage offset $|V_{\rm REF} - V_{\rm OUT}| = f_{\rm REF}/(K_{\rm VCO}N)$. A lower steady-state f_s improves the quantizer resolution which is important to reduce the output ripple considering the fact that the quantizer output toggles between ± 1 LSB in steady state. Here, one thing to note is that the nonlinear characteristics in BF quantizer provide much higher resolution, i.e., sensitivity compared to the linear quantizer. When $f_{\rm OUT}$ is very close to $f_{\rm REF}$, a small change in input causes a large change in $N_{\rm OUT}$, making the quantizer highly sensitive to input change. To compare this with the linear quantizer case, a 10% change in $f_{\rm OUT}$ (or $V_{\rm OUT}$) results in 10% change in $N_{\rm OUT}$ for the linear quantizer, while the BF quantizer output changes by 80% for the same change in input. This large count error, i.e., $|N - N_{\rm OUT}|$ along with increased f_s during voltage droop or overshoot switches large numbers of PMOS at the output stage very fast, reducing the amount of voltage error while providing a faster recovery. However this high resolution does not come for free, as the fixed steady-state offset generated at the output degrades the dc regulation. However, the good thing about this fixed offset is that it is predictable and can be easily tuned as well. Moreover, it introduces an inherent feature called AVP for the reduction of transient peak-to-peak voltage deviation which is discussed in Section III.

The voltage droop/overshoot occurring at any instance is captured by the DLDO when the next sampling clock ($\rm CK_s$) edge appears, which depends on its frequency f_s. Hence, the voltage droop/overshoot is not only a function of the load capacitance $C_{\rm LOAD}$ but also depends on how fast the DLDO responds. The conventional and proposed DLDO behavior for an abrupt load current ($I_{\rm LOAD}$) step is shown in Fig. 5. Since f_s in BF quantizer is proportional to the amount of droop, when a droop occurs, the sampling frequency increases and the subsequent clock edge comes much earlier. This helps to

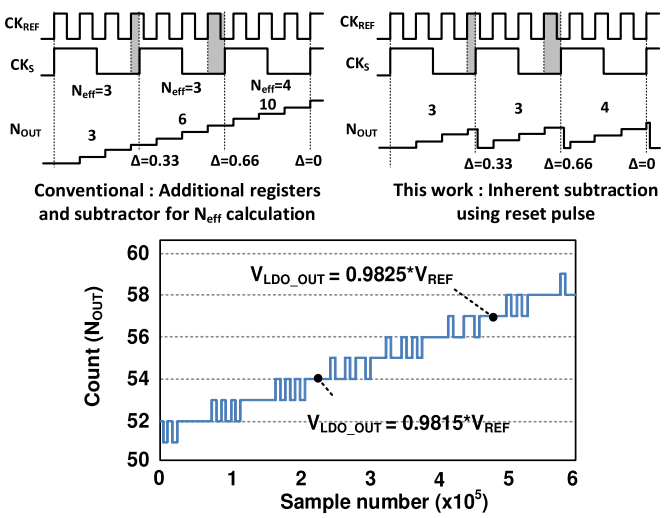


Fig. 6. Conventional and proposed noise shaping VCO phase quantization (top) simulated BF quantizer output (N_{OUT}) (bottom) for a slow ramp in V_{LDO_OUT} in open-loop showing the first-order noise shaping.

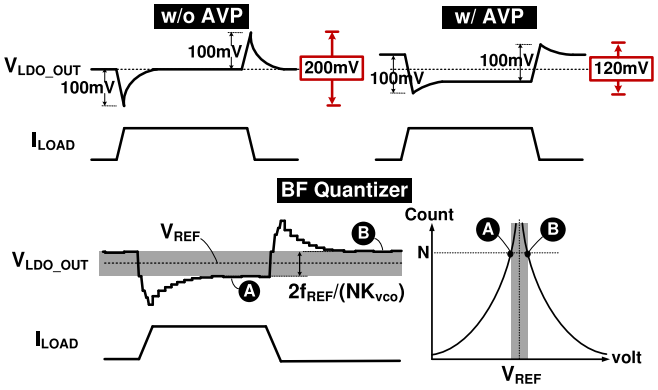


Fig. 7. AVP to reduce the transient voltage deviation. The inherent steady-state offset present in the BF DLDO introduces AVP.

react the DLDO immediately after the droop. In other words, C_{LOAD} required for a given voltage droop or settling time is much smaller due to adaptive sampling compared to fixed sampling.

The resolution of a VCO-based quantizer can be improved by continuously counting the VCO phase without resetting it. Thereby, the quantization error generated in each sampling period is preserved and accounted for in the subsequency period, providing first-order noise shaping. This noise-shaping property is present in any VCO-based time quantizer and an extensive analysis is performed in [15]. However, the continuous count of the VCO phase requires additional registers to store the previous count along with a digital subtractor to generate effective count value in each sampling period. In this implementation, a similar functionality is achieved by using a short reset pulse at the beginning of each count which resets the count value without impacting the VCO phase. The difference between the conventional implementation and the proposed implementation is illustrated in Fig. 6 (top) while achieving first-order noise-shaping characteristics in both cases. Simulated BF quantizer output in Fig. 6 (bottom) for a slow input ramp shows the noise shaping behavior similar to a first-order delta–sigma modulator. A detailed explanation and supporting measurement results for a noise-shaping BF quantizer-based ADC are provided in [17].

The BF quantizer, which was first introduced for circuit aging measurements [21]–[23] for its ability to precisely detect picosecond delay, shifts within a few microseconds. Since then, it has been utilized in many other applications such as ADC [17]–[19], adaptive phase-locked loop [20], and true random-number generator [24].

III. Active Voltage Positioning

Transient voltage deviation in power supply due to droop or overshoot is a key performance metric of a voltage regulator. "AVP (or adaptive voltage positioning)" is a popular technique for reducing the peak-to-peak deviation [25]–[28]. Here, the regulator is intentionally made imperfect by adjusting the output voltage depending on the load current. In other words, the steady state or dc regulation is compromised to significantly improve the transient response. Simple waveforms in Fig. 7 show how AVP reduces the peak-to-peak output excursion from 200 to 120 mV for the same amount of droop or overshoot. The basic idea is to set V_{LDO_OUT}at a slightly higher voltage than its nominal value under minimum load condition, so that the voltage undershoot due to sudden load current increase can be mitigated. Similarly, under the maximum load condition, V_{LDO_OUT} is set at a slightly lower voltage than the nominal value to reduce the overshoot noise. Overall, the maximum voltage error ($V_{LDO\_OUT} - V_{REF}$) reduces, minimizing the peak-to-peak deviation as the expense of an imperfect steady-state voltage.

An added benefit of AVP is the power reduction in a high-load state. In conventional designs, the supply voltage is usually set at a higher voltage to ensure circuit functionality with the presence of voltage droop. This translates into additional power dissipation in high-load state. However, with the presence of AVP, the supply voltage is set to the minimum operating voltage in the high-load state, which can reduce the power consumption.

In a BF quantizer-based DLDO, the non-linear transfer characteristic introduces a fixed voltage offset at the DLDO output when the loop is locked to $N_{OUT} = N$. As shown in Fig. 7, depending on the load current, the output can settle to either point A or point B generating a dc voltage error of $2f_{REF}/NK_{VCO}$. Therefore, AVP is inherently present. Tuning N depending on the requirement can easily control the voltage position. A large N has negligible dc voltage error, while smaller N suppresses transient deviation. For example, $N = 64$ causes a voltage error of 26 mV when f_{REF} and K_{VCO} are 250 MHz and 300 MHz/V, respectively. If the peak-to-peak deviation is 200 mV without AVP, it drops to 174 mV for $N = 64$ and 96 mV when $N = 16$.

IV. Small-Signal Model and Stability Analysis

A small-signal discrete-time model of the proposed DLDO is shown in Fig. 8(a). The VCO voltage-to-phase

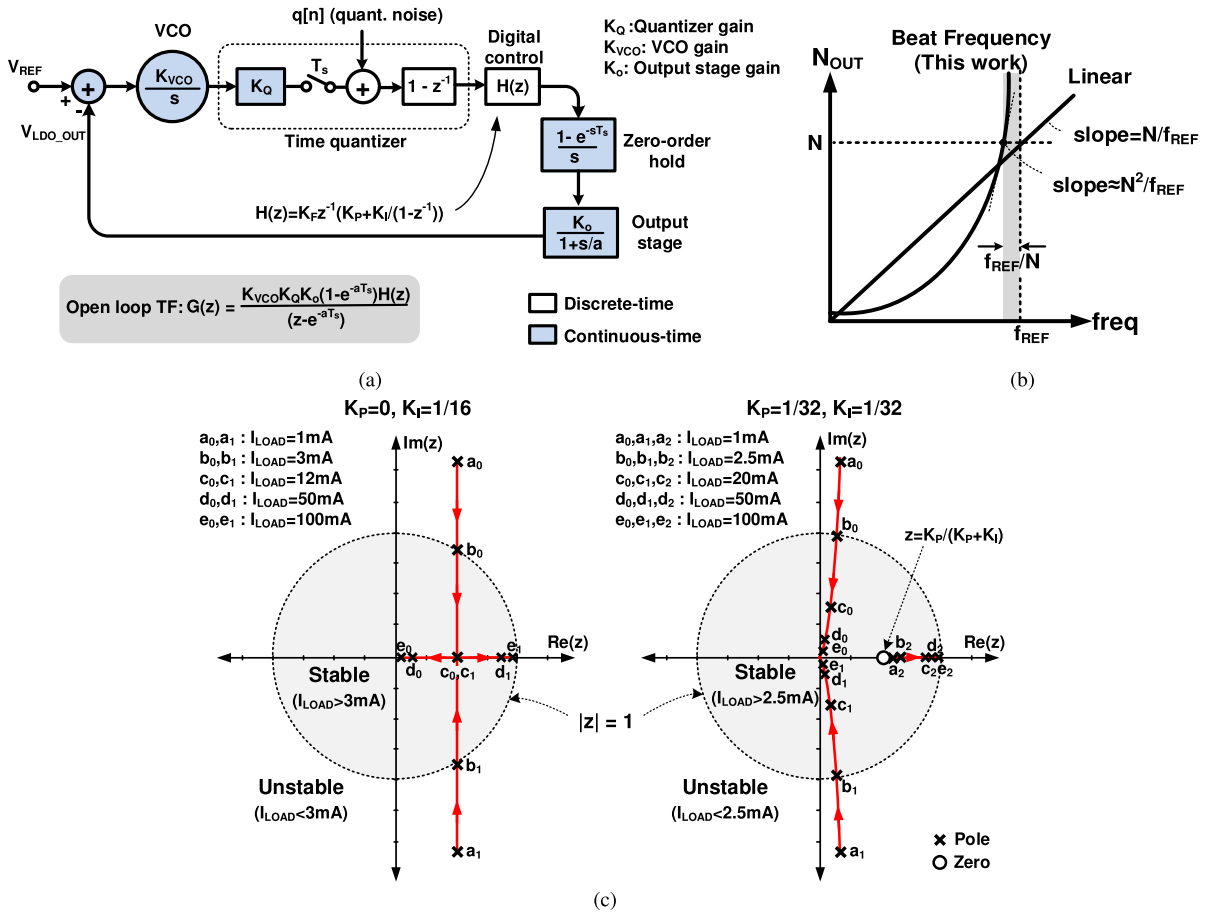


Fig. 8. (a) Small-signal equivalent model of the time-based digital LDO. (b) Quantizer gain (K_Q) of BF quantizer is very high K_Q due to nonlinear characteristic. (c) Simulated closed-loop discrete-time poles and zeros for two different loop filter gain settings showing the I_{LOAD} range for stability.

transformation is represented by $K_{\mathrm{VCO}}/\mathrm{s}$. K_Q is the time-quantizer gain, which is derived from the slope of the transfer characteristic ($\partial N_{\mathrm{OUT}}/\partial f_{\mathrm{OUT}}$). For the linear quantizer

$$K_Q|_{\mathrm{Linear}} = \frac{N}{f_{\mathrm{REF}}}. \tag{3}$$

However, in the case of a BF quantizer, the non-linear transfer characteristic makes K_Q dependent on N_{OUT} and it is derived as

$$K_Q|_{\mathrm{BF}} = \frac{f_{\mathrm{REF}}}{|f_{\mathrm{REF}-}f_{\mathrm{OUT}}|^2}\mathrm{sign}(f_{\mathrm{REF}-}f_{\mathrm{OUT}}) \tag{4}$$

$$= \begin{cases} \dfrac{N_{\mathrm{OUT}}^2}{f_{\mathrm{REF}}}, & \text{if } f_{\mathrm{OUT}} < f_{\mathrm{REF}} \\ -\dfrac{N_{\mathrm{OUT}}^2}{f_{\mathrm{REF}}}, & \text{if } f_{\mathrm{OUT}} > f_{\mathrm{REF}}. \end{cases} \tag{5}$$

Therefore, the magnitude of K_Q near steady state is N^2/f_{REF}, which is N times higher than the linear quantizer gain [shown in Fig. 8(b)]. From (5), it is evident that K_Q changes polarity when f_{OUT} crosses f_{REF}, requiring a polarity detector. Details about the polarity detector implementation are explained in Section V. For the stability analysis, K_Q is assumed to be always positive.

The output of the quantizer is updated at every rising edge of the sampling clock (i.e., beat period), so a sampling switch (T_s) is added. Since the counter is continuously counting the VCO edges, the count value in two consecutive sampling edges is subtracted to obtain the effective count. This introduces a $(1 - z^{-1})$ factor at the quatizer output. This also explains how the quatization noise ($q[n]$) is first-order noise shaped. The digital control consists of a proporional path of gain K_P, integral path of gain K_I, and overall forward path gain of K_F, generating a transfer function

$$H(z) = K_F z^{-1}\left(K_P + \frac{K_{\mathrm{I}}}{1 - z^{-1}}\right). \tag{6}$$

Since the digital control output is held constant till the next clock edge, a zero-order hold is placed before the output stage. The output stage comprises a PMOS switch array and load circuit, which can be approximated as an RC load. If the effective capacitance is C_{LOAD} and the PMOS array effective resistance is $R_{\mathrm{L}} = V_{\mathrm{DROP}}/I_{\mathrm{LOAD}}$, where V_{DROP} is the LDO dropout voltage, the output pole frequency is given by

$$a = \frac{1}{R_L C_{\mathrm{LOAD}}} = \frac{I_{\mathrm{LOAD}}}{V_{\mathrm{DROP}} C_{\mathrm{LOAD}}}. \tag{7}$$

This introduces a z-domain pole at $z = e^{-aT_s}$, where $T_s = 1/f_s$ is the sampling period. The dc gain of the output stage (K_o) is calculated from the effective change of output voltage for 1 LSB change in input code. If each PMOS switch

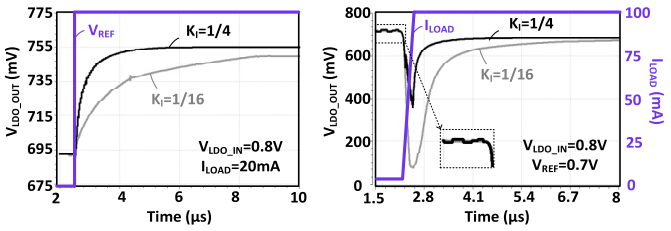


Fig. 9. Simulated V_{REF} and I_{LOAD} step response for different K_I values verifying the correctness of model. Lower K_I reduces the loop-gain increasing the settling time. Higher K_I reduces stability in low I_{LOAD}.

has a resistance R_u, and M number of switches are on for a given I_{LOAD} such that $R_L = R_u/M$, then K_o can be derived as

$$K_o = \left(\frac{R_u}{M} - \frac{R_u}{M+1}\right) I_{\mathrm{LOAD}} \approx \frac{R_u I_{\mathrm{LOAD}}}{M^2} = \frac{V_{\mathrm{DROP}}^2}{R_u I_{\mathrm{LOAD}}}. \quad (8)$$

From (8), it is evident that K_o is inversely proportional to I_{LOAD}. The open-loop transfer function in the z-domain is

$$G(z) = \frac{K_{\mathrm{VCO}} K_Q K_o (1 - e^{-aT_s}) H(z)}{z - e^{-aT_s}} \quad (9)$$

$$= \frac{K_T z^{-1}(z - K_P/(K_P + K_I))}{(z - e^{-aT_s})(z - 1)}. \quad (10)$$

Here, $K_T = K_{\mathrm{VCO}} K_Q K_o (1 - e^{-aT_s}) K_F (K_P + K_I)$ is the total forward-path gain [4]. When $K_P \neq 0$, the system has one zero and three poles, but for $K_P = 0$, it simplifies to a two-pole system. The closed-loop poles and zeros (i.e., root locus) are plotted in Fig. 8(c), by varying I_{LOAD} (i.e., K_T). The design parameters used in the calculation are as follows: $K_{\mathrm{VCO}} = 300$ MHz/V, $V_{\mathrm{DROP}} = 0.1$ V, $R_u = 1$ kΩ, $K_F = 1$, $C_{\mathrm{LOAD}} = 40$ pF, $N = 64$, and $f_{\mathrm{REF}} = 250$ MHz. The first plot is for $K_P = 0$, $K_I = 1/16$ which is a two-pole system and the closed-loop poles remain inside the unit circle for $I_{\mathrm{LOAD}} > 3$ mA making the system asymptotically stable. The second plot is for $K_P = K_I = 1/32$ keeping K_T the same as the previous case. This system has three poles and a zero at 0.5. Stability is achieved for $I_{\mathrm{LOAD}} > 2.5$ mA. Here, one thing to note is that f_s is much smaller than the output pole (i.e., $aT_s \gg 1$) which makes $z = e^{-aT_s} \approx 0$, nearly independent of f_s. This is possible due to the presence of a very low C_{LOAD} in the design that moves the output pole to a very high frequency (>1 GHz) and keeps the system stable for a much wider f_s range. The minimum I_{LOAD} requirement for the DLDO stability is dictated by the processor current consumption in the idle or low activity state. The minimum I_{LOAD} and maximum V_{DROP} decide the PMOS switch resistance since a minimum number of switches will be connected in parallel in this condition.

In order to verify the accuracy of the model, circuit-level transient simulations are performed. The DLDO output response for a 100-mV step in V_{REF} and the minimum 3 mA to maximum 100 mA step in I_{LOAD} are observed for two K_I values, as shown in Fig. 9. Higher K_I increases the gain K_T, and therefore, achieves faster loop stability, but it comes at the cost of reduced stability margin in low load currents as evident from the small ripples when $I_{\mathrm{LOAD}} = 3$ mA and $K_I = 1/4$.

V. Circuit Implementation Details

Fig. 10 demonstrates the architecture of the proposed time-based DLDO implemented in a 65-nm CMOS technology. It comprises the conventional linear quantizer as a baseline and the proposed BF quantizer to compare the performances while keeping all parameters identical. SEL_Q selects the desired quantizer. The output of the quantizer (N_{OUT}) is compared with an external code N and the difference goes to the 10-bit proportional–integral (PI) digital control block to switch 1024 PMOS array at the output stage to keep $V_{\mathrm{LDO\_OUT}}$ nearly constant irrespective of the load current. As the BF quantizer detects the absolute voltage difference (ΔV) between V_{REF} and $V_{\mathrm{LDO\_OUT}}$, the loop feedback becomes positive when ΔV changes its polarity. Therefore, during BF quantizer operation, a digital comparator is used to detect the voltage polarity and keeps the loop always in the negative feedback configuration. The on-chip load capacitance is 40 pF. A programmable load current generation block generates current from 0 to 400 mA with a wide variation in rise/fall time. The implementation details of different building blocks of the DLDO are described in Sections V-A–V-D.

A. BF Quantizer

The BF quantizer, as previously mentioned, counts the number of $\mathrm{CK_{REF}}$ edges within a single beat period. Fig. 11 shows the circuit implementation. Since the BF clock is synchronized to the rising edge of $\mathrm{CK_{REF}}$, the counter increments at the negative edge. After reading the count (D_{OUT}) at the beginning of every cycle, a reset pulse (RST) restarts the counter. This reset pulse only resets the count value to 0 before the next VCO clock edge without impacting its phase. This keeps the VCO always ON preserving the quantization error information in the subsequent cycle providing first-order noise shaping, as shown in Fig. 6. This avoids the requirement of the digital subtractor and registers, which is otherwise required to get the effective count from the phase count stored in two consecutive cycles.

B. Voltage-Controlled Oscillator

Fig. 12 (left) illustrates the design of the VCO. It comprises a voltage-to-current converter followed by a five-stage ring oscillator-based current-controlled oscillator (CCO). A 5-bit coarse control achieves a wide tuning range by adjusting the CCO current. This ensures the desired frequency of oscillation for optimum performance over a wide input–output voltage range.

Any parasitic or device mismatch present between two VCOs introduces an additional systematic voltage offset at the DLDO output during the steady state. A 4-bit switched capacitor array performs the fine frequency tuning in order to compensate this offset. Although this one-time trimming is unable to track any dynamic VCO frequency variation due to temperature drift, thermal and packaging stress, the offset due to this dynamic variation will be relatively small as VCOs are compact and placed side-by-side in the layout.

Both coarse and fine controls are externally calibrated and are not a part of the LDO loop. A part of the CCO current

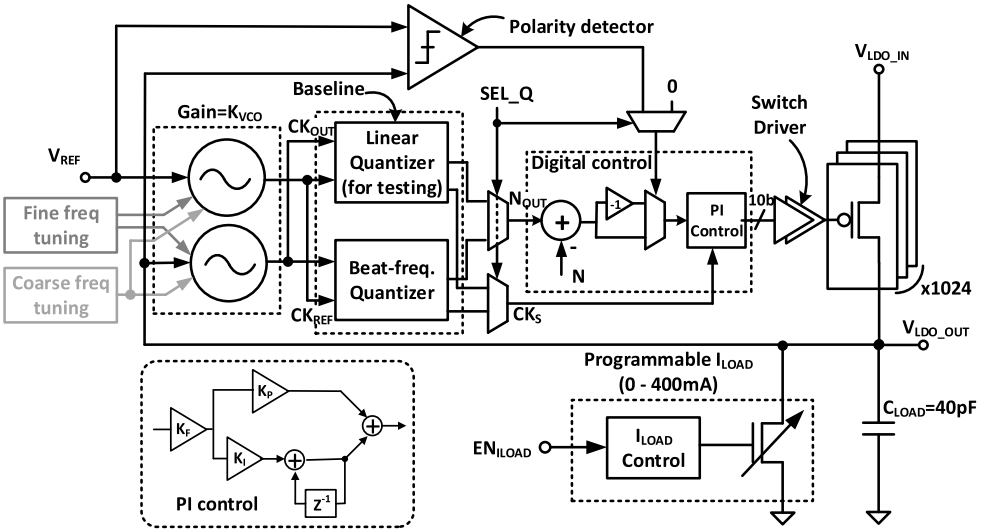


Fig. 10. Complete top-level block diagram of the proposed digital LDO. Linear quantizer is also present for performance comparison.

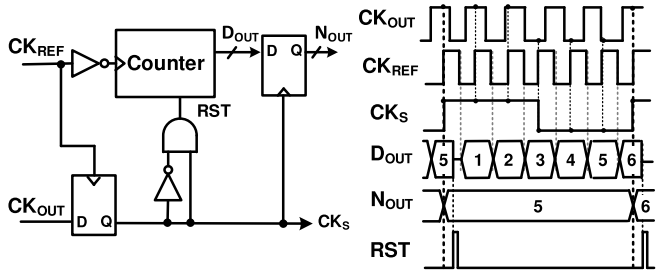


Fig. 11. Implementation of the BF quantizer.

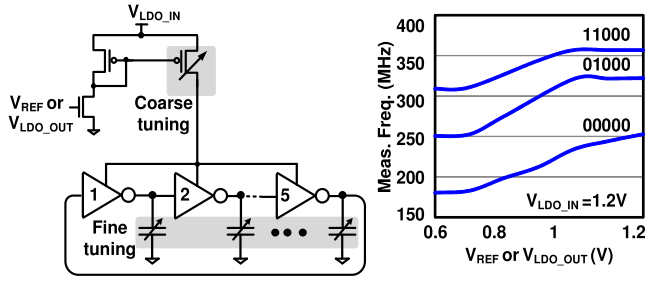


Fig. 12. Schematic of the five-stage ring VCO (left) and measured frequency tuning characteristics (right).

is proportional to the input voltage (V_{REF} or V_{LDO_OUT}) while the remaining portion is kept fixed. This ensures VCO oscillation during DLDO startup and keeps f_{OUT} within a small range around f_{REF} for accurate BF operation. The measured VCO tuning for different coarse codes is shown in Fig. 12 (right).

C. Driver and Output Stage

A 10-bit binary code (C_9–C_0) from the digital PI control tunes the 1024 PMOS switch array at the output stage. Since each bit drives different number of switches, effective load due to PMOS gate capacitance is different as well. Therefore, the load needs to be balanced among all bits in order to keep the rise and fall times the same. Any large imbalance

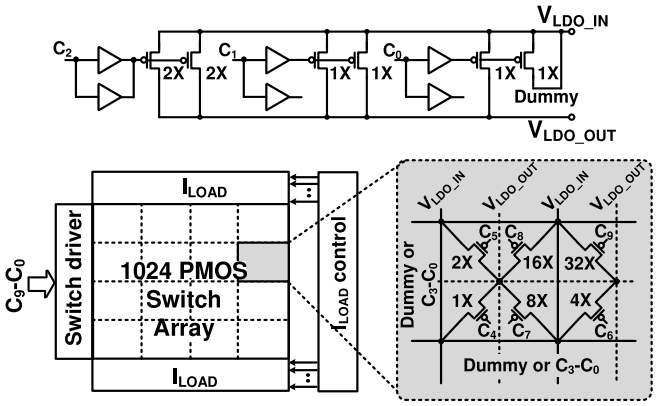


Fig. 13. Driver design for PMOS switch array (top). A 3-bit example showing the balanced loading. Uniformly distributed layout strategy of PMOS switch array (bottom).

in the rise/fall time during code transition will appear as a transient glitch at V_{LDO_OUT}. A balanced loading is achieved by using dummy drivers as well as switches, as shown in the 3-bit example of Fig. 13. Apart from these 1024 switches, additional 64 switches are also added in parallel which are always ON. This sets the maximum resistance value when C_9–C_0 are in the minimum code setting. Moreover, since each of these switches acts as a resistor, the resistance change should be monotonic with input code. Therefore, the device-to-device matching is critical, especially when many such switches are already ON (i.e., low R_L case). The parasitic resistance due to additional metal routing while connecting the source and the drain terminals also contributes to the resistance mismatch. All of these are taken care of by a uniformly distributed layout design as evident in Fig. 13. Entire area is divided into 4×4 subgroups each having 32 switches driven by C_9, 16 switches driven by C_8, and so on.

D. Programmable I_{LOAD} Generator

To verify the DLDO functionality over a wide operating condition, an on-chip programmable I_{LOAD} generation block

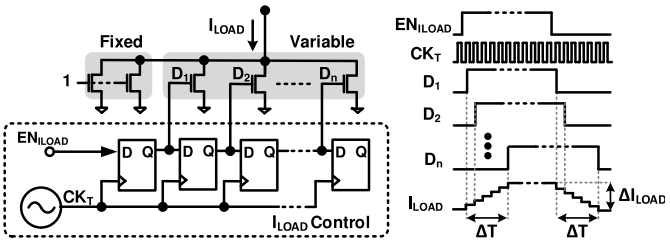


Fig. 14. Programmable I_{LOAD} generator. Rise/fall time (ΔT) tunability: 16 ns–9 μs and ΔI_{LOAD} range: 0–400 mA.

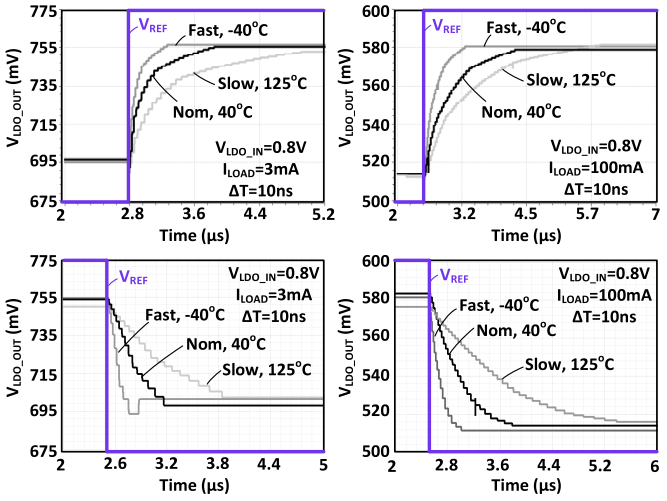


Fig. 15. Simulated V_{REF} step response of the implemented DLDO in different process and temperature corners under minimum and maximum I_{LOAD} condition.

with varying magnitude (ΔI_{LOAD}) and rise/fall time (ΔT) is incorporated. As illustrated in Fig. 14, NMOS transistor-based unit current elements are designed. The current flowing through each element and the total number of such elements are programmable using scan bits. I_{LOAD} rise/fall is initiated by the external control EN_{ILOAD}. Some elements are kept always ON to draw a fixed minimum I_{LOAD}. In a real application, this minimum I_{LOAD} will be decided by the current consumption in the idle or low-activity mode of the processor, which is powered by this DLDO. Remaining elements are sequentially turned on/off using a test clock (CK_T) generated from an on-chip ring oscillator that drives a series of shift registers. The oscillator frequency is tuned between 11 and 750 MHz, and the number of shift-register stages is programmed between 12 and 96 to control ΔI_{LOAD} and ΔT. ΔI_{LOAD} can vary between 0 and 400 mA, and ΔT can also be controlled between 16 ns and 9 μs. During our tests, I_{LOAD} was kept under 100 mA due to the limited current carrying capability of the IOs.

The DLDO operation is verified from simulations across different input–output voltage and maximum/minimum load current conditions in the presence of process and temperature variations. Simulated V_{REF} step response is shown in Fig. 15. The difference in settling time among different corners is due to the change in the VCO operating frequency and gain, as well as the PMOS switch resistance, which leads to different

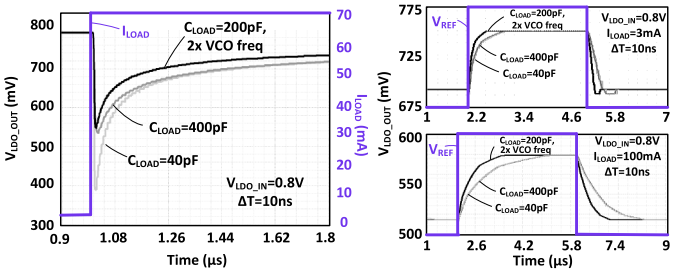
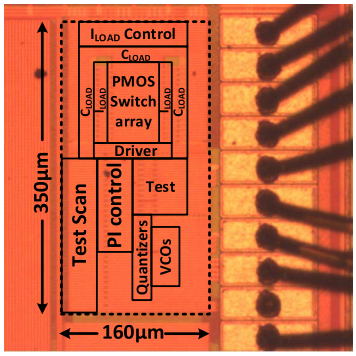


Fig. 16. DLDO response for a sharp ΔI_{LOAD} step causing larger droop which can be mitigated by larger C_{LOAD} and higher VCO frequency (left). System stability is ensured from V_{REF} step response (right).



Area (mm^2)	
VCOs	0.002
Other digital	0.0174
PMOS array	0.008
C_{LOAD}	0.01
Test	0.0186
Total	0.056
Power Diss. (mW) @ V_{LDO_IN}=1V	
VCOs	0.60
Other digital	0.20
Total	0.80

Fig. 17. 65-nm test-chip micrograph with area and power breakdown.

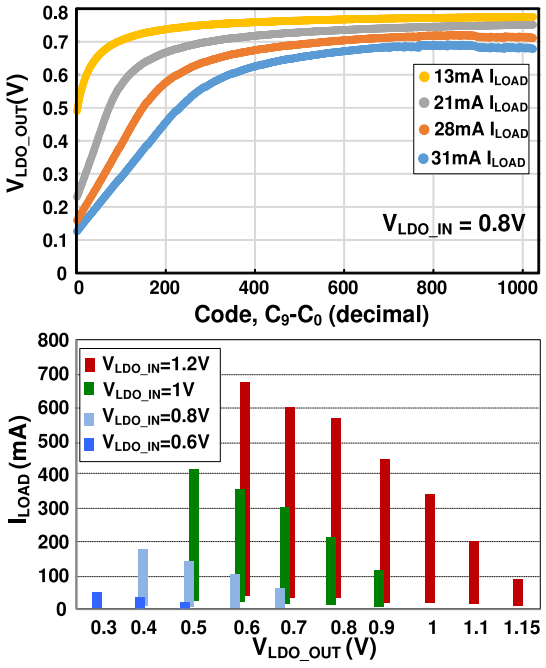


Fig. 18. Measured DLDO open loop characterization. Open-loop output voltage by sweeping 10-bit switch code (top). Calculated I_{LOAD} range of operation from the measured dropout voltage and PMOS switch resistance (bottom).

loop gain. Here, one thing to note is that C_{LOAD} and f_s are optimized for the desired maximum $\Delta I_{LOAD}/\Delta T$. Therefore, a much sharper ΔI_{LOAD} step introduces larger droop which requires higher C_{LOAD} or f_s to mitigate this, as evident from

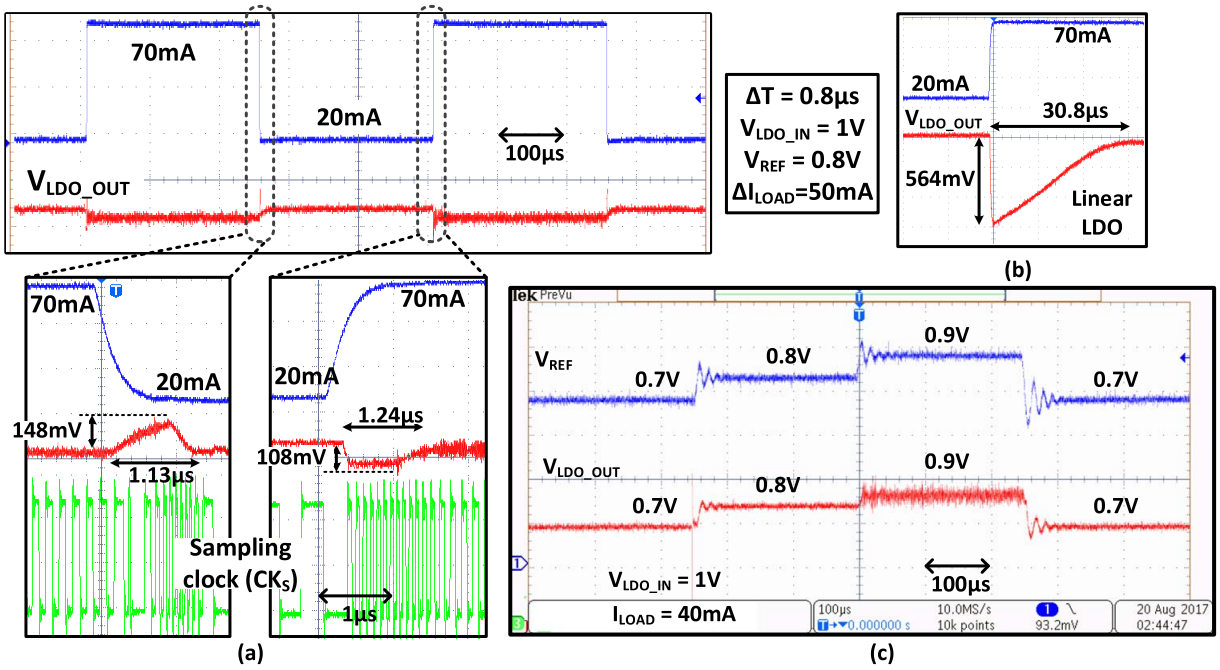


Fig. 19. Measured transient response of (a) proposed adaptive DLDO and (b) baseline DLDO. The response in V_{REF} transient variation is shown in (c).

the simulated step response in Fig. 16 (left). Increasing C_{LOAD} by 10× has a similar droop reduction as increasing both C_{LOAD} and f_s by 5× and 2×, respectively. However, higher f_s in the second case makes the DLDO response faster. As discussed in Section IV, increasing C_{LOAD} or f_s makes aT_s smaller which moves the output pole, $z = e^{-aT_s}$ toward unity circle, reducing the stability margin. However, the high-resolution BF quantizer in this paper achieves a fast response using very low f_s which makes $aT_s > 25$; even for the highest if_s, the DLDO can operate during droop/overshoot. As a result, the system is quite stable even if aT_s drops by 10×. This has been verified from the V_{REF} step response shown in Fig. 16 (right).

VI. Measurement Results

The test chip was fabricated in a 1.2-V 65-nm low power CMOS technology. The die micrograph is shown in Fig. 17 along with the breakdown of area and power dissipation. Total core area is 0.0374 mm^2 including the integrated 40 pF C_{LOAD}. The DLDO is first characterized in an open-loop configuration where the 10-bit code (C_9–C_0) at the PMOS array input is applied externally and swept for a fixed I_{LOAD} to observe the variation in $V_{\mathrm{LDO\_OUT}}$, as shown in Fig. 18 (top). The resistance of each PMOS switch is measured from the effective change in $V_{\mathrm{LDO\_OUT}}$ for a given code change. Measurements are performed for different $V_{\mathrm{LDO\_IN}}$ and I_{LOAD}. Based on this, the I_{LOAD} range is calculated for any desired input–output voltage as observed in Fig. 18 (bottom). Here, the maximum and the minimum I_{LOAD} are calculated assuming C_9–C_0 in the maximum and minimum code settings, respectively. This provides the maximum I_{LOAD} operating range of the DLDO. Fig. 19(a) and (b) plots the closed-loop transient response of the proposed BF quantizer-based DLDO and the linear quantizer-based baseline design, respectively, for a load step from 20 to 70 mA, i.e., $\Delta I_{\mathrm{LOAD}} = 50$ mA. In steady state, both operate at a 3.9-MHz sampling clock. Due to the increased sampling frequency during load transients, the voltage droop (ΔV) and settling time (T_{SET}) are reduced from 564 to 108 mV (i.e., 5×) and from 30.8 to 1.24 μs (i.e., 25×) compared to the baseline. As observed, due to the low f_s, the linear quantizer has a really poor performance which is unacceptable in any practical application. However, simply replacing the frequency divider in a linear quantizer with a D-flip-flop can significantly improve the performance while keeping the rest of the design identical. The response is also fast for any transient variation in V_{REF}, as shown in Fig. 19(c). ΔV and T_{SET} are measured for a wide variation under load condition. In Fig. 20 (top), the rise time of load current (ΔT) is varied while keeping ΔI_{LOAD} fixed at 50 mA which gives 5×–10× lower ΔV and 20×–35× faster settling compared to the baseline. In Fig. 20 (bottom), ΔT is kept constant at 0.25 μs while sweeping ΔI_{LOAD} across 18–65 mA. ΔV reduction was 5×–4× and improvement in T_{SET} was 15×–30× due to adaptive sampling. The steady-state measurement results of the DLDO are plotted in Fig. 21. DLDO output variation, ΔV_o with $V_{\mathrm{LDO\_IN}}$ is within 41 mV (±2%) and 43 mV (±5%) for $V_{\mathrm{REF}} = 0.9$ V and $V_{\mathrm{REF}} = 0.4$ V, respectively. Similarly, ΔV_o over the I_{LOAD} range of 8–100 mA remains within ±2.9%.

Fig. 22 verifies the AVP operation of the proposed DLDO, as described in Section III. For a large N value of 64, the dc offset is very low, providing a good dc regulation. However, the peak-to-peak deviation is 260 mV. Now, as we keep reducing N, AVP becomes stronger. For $N = 16$, it decreases to 120 mV. The measured current efficiency is more than 93% over 10× variation in load current achieving a maximum

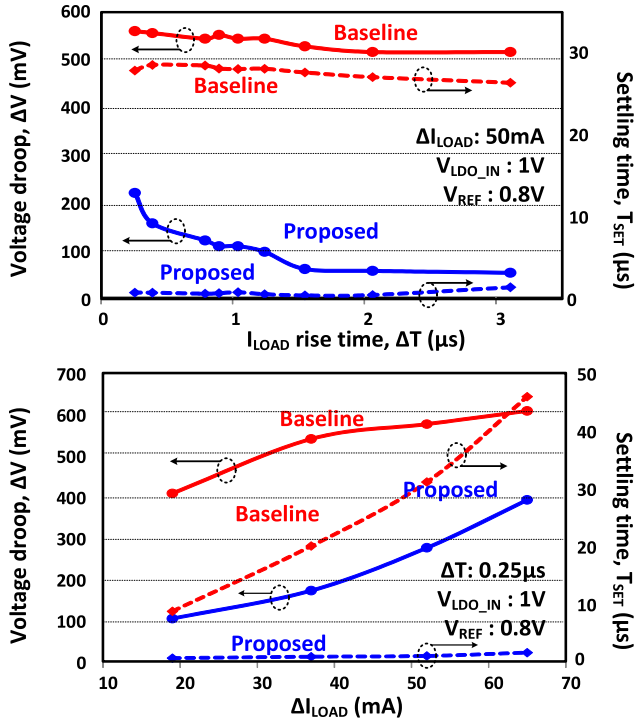


Fig. 20. Voltage droop and settling time measurements by varying rise time (top) and magnitude of ΔI_{LOAD} (bottom).

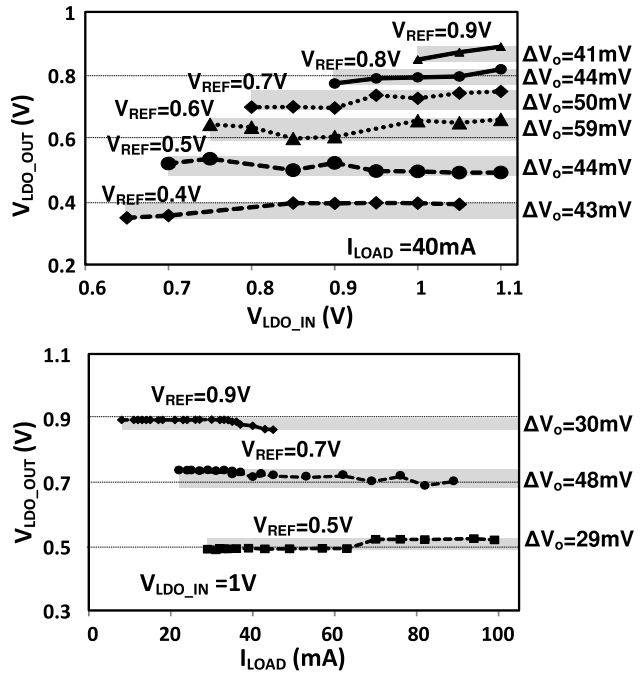


Fig. 21. Measured steady-state performance for different V_{REF}.

of 99.5%, as shown in Fig. 23. The power supply rejection ratio (PSRR) is measured by providing a 100-mVpp sinusoidal wave noise at $V_{\mathrm{LDO\_IN}}$ and observing the peak-to-peak swing at $V_{\mathrm{LDO\_OUT}}$. The PSRR, as shown in Fig. 24, is below −30 dB for noise frequencies up to 5 MHz. The high PSRR is primarily due to the high gain of the BF quantizer. Moreover,

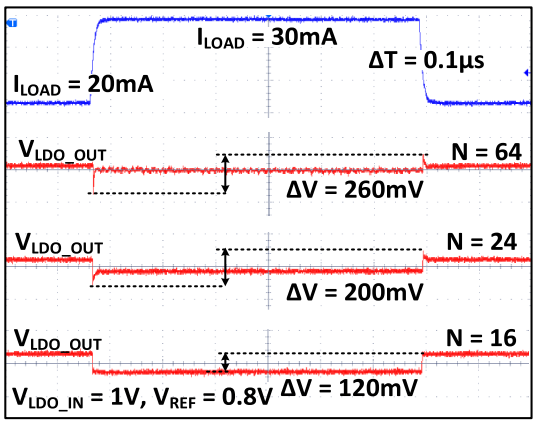


Fig. 22. Reduction of peak-to-peak voltage deviation by AVP.

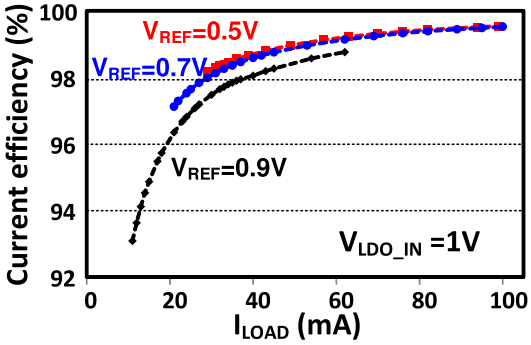


Fig. 23. Current efficiency versus I_{LOAD} measurement results.

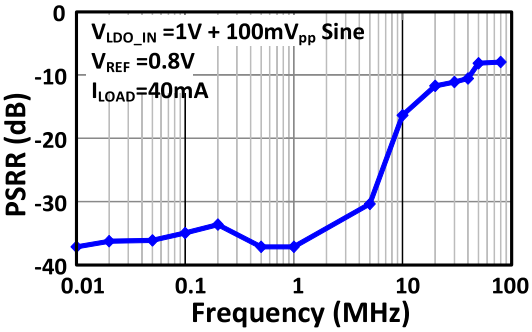


Fig. 24. Measured PSRR.

the quantizer based on two identical VCOs is highly insensitive to common-mode power supply variation.

Finally, this paper is compared with other state-of-the-art LDO architectures in Table I. References [4], [9], and [10] are voltage comparator-based DLDO architectures. Each uses large off-chip $C_{\mathrm{LOAD}}$for droop and settling time reduction. Reference [9] has a better figure of merit (FOM_1) than this paper but it uses a 20-nF off-chip C_{LOAD}. Higher C_{LOAD} helps to achieve higher ΔI_{LOAD} while reducing ΔV. Since FOM_1 is proportional to $1/(\Delta I_{\mathrm{LOAD}})^2$, higher C_{LOAD} naturally has better FOM_1. However, utilizing adaptive sampling and high-resolution VCO quantizer proposed design uses the lowest C_{LOAD} but still achieves comparable FOM_1. In terms of FOM_2, this paper is better than the state-of-the-art DLDOs

TABLE I
PERFORMANCE COMPARISON

	[29]Bulzacchelli, JSSC'12	[2] Lu, TCASI'15	[4] Nasir, TPE'16	[5] Lee, JSSC'17	[7] Kim, JSSC'17	[8] Yang, JSSC'17	[9] Tsou, ISSCC'17	[6] Salem, JSSC'18	[10] Lin, ISSCC'18	This Work
Type	Analog	Analog	Digital	Digital	Digital	Digital	Digital	Digital	Digital	Digital
Process	45nm SOI	65nm	130nm	28nm	65nm	65nm	40nm	65nm	40nm	65nm
Architecture	Dual-loop	Tri-loop	Shift Reg	Shift Reg+ADC	Event driven ADC	Asynchronous Pipeline	Dead-zone Control	SAR ADC	Burst Mode	VCO based ADC
Adaptive sampling/ AVP	NA / No	NA / No	Yes / No	No / No	Yes / No	Yes / No	No / No	No / No	Yes / No	Yes / Yes
V_{LDO_IN} (V)	1.179 – 1.625	1	0.5 – 1.2	1.1	0.45 – 1	0.6 – 1	0.6 – 1.1	0.5 – 1	0.6 – 1.1	0.6 – 1.2
V_{LDO_OUT} (V)	0.9 – 1.1	0.85	0.45 – 1.14	0.9	0.4 – 0.95	0.55 – 0.95	0.5 – 1	0.3 – 0.45	0.5 – 1	0.4 – 1.1
Max .I_{LOAD} (mA)	42	10	4.6	200	3.36	500	210	2	20	100
DC Load Reg.(mV/mA)	0.083	1.1	NA	0.035	NA	0.25	0.075	5.6	0.1	0.638**
I_Q (mA)	12	0.05 – 0.09	0.024 – 0.22	0.11	0.08 – 0.26	0.3	0.02 – 0.1	0.014	0.02	0.1 – 1.07
C_{LOAD} (nF)	1.46	0.14 (integrated)	1	23.5	0.1 (Integrated)	1.5 (Integreated)	20	0.4 (Integrated)	4.7	0.04 (Integrated)
PSRR(dB)	NA	-12 @ 5MHz	-16 @ 10MHz	NA	-20 @ 10KHz	-21.2 @ 1MHz	NA	NA	NA	-38 @ 1MHz
Max current efficiency (%)	77.5	99.1	98.3	99.94	99.2	99.94	99.99	99.8	99.8	99.5
$\Delta V, T_{SET}$ @ ΔI_{LOAD}	NA	43mV,0.1µs @10mA	90mV,1.1 µs @1.4mA	120mV,40 µs# @180mA	34mV,11.2 µs @1.44mA	50mV, 0.04µs @100mA	36mV,1.3 µs @200mA	40mV,0.1 µs @1.06mA	40mV,1.3 µs @19mA	108mV,1.24 µs @ 50mA
Area (mm^2)	0.075	0.0234	0.355	0.021	0.03*	0.158*	0.1926	0.0023*	0.18	0.0374
FOM_1 (ps)	62.4	5.74	10100	9.57	20	2.3	0.4	199	10.4	1.38
FOM_2 (pF)	NA	0.067	20.2	1.914	0.064	0.383	0.16	0.47	0.19	0.086

From oscilloscope waveform
*Without C_{LOAD}

$FOM_1=C_{LOAD}(\Delta V/\Delta I_{LOAD})(I_Q/\Delta I_{LOAD})$
$FOM_2=C_{LOAD}(\Delta V/V_{LDO\_OUT})(I_Q/\Delta I_{LOAD})$
} Smaller value is better

**Measured at V_{LDO_OUT}=0.9V

except in [7], which have a fairly large settling time. Our work is also the first DLDO that incorporates AVP. Although the performance of this DLDO is quite competitive or better than the state-of-the-art, with a few design changes, it can be improved further. A multi-phase clocking similar to that in [16] utilizing all the phases of the ring oscillator VCO, which are generated inherently, can provide a much faster response during droop/overshoot. In addition, a coarse-fine-based two separate PMOS switch arrays can ensure stability in much lower I_{LOAD} values and also improves the overall I_{LOAD} range of operation.

VII. CONCLUSION

The proposed fully integrated DLDO using a VCO-based time quantizer provides dynamically adaptive sampling clock for droop/overshoot reduction enabling an output load capacitance of only 40 pF. It also has an inherent feature of AVP for the reduction of peak-to-peak voltage deviation. The maximum current efficiency and FoM measured from a 65-nm test-chip are 99.5% and 1.38 ps, respectively.

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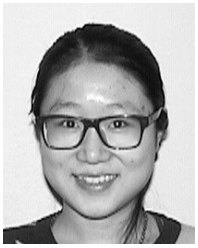

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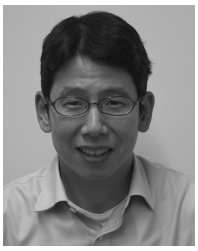

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