A Fully Integrated 40pF Output Capacitor Beat-Frequency-Quantizer-Based Digital LDO with Built-In Adaptive Sampling and Active Voltage Positioning

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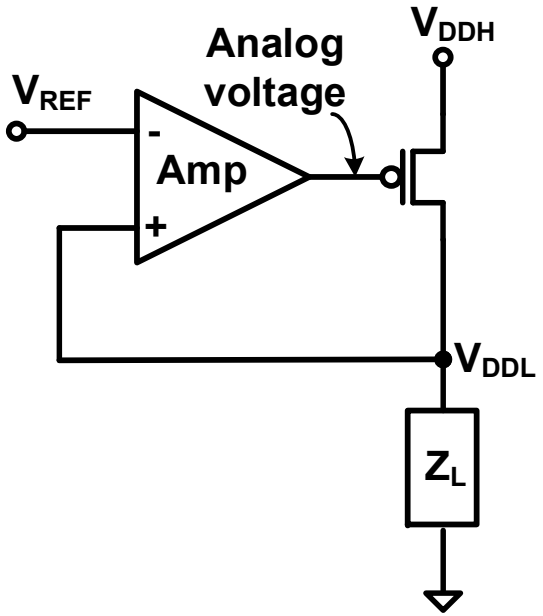
Outline

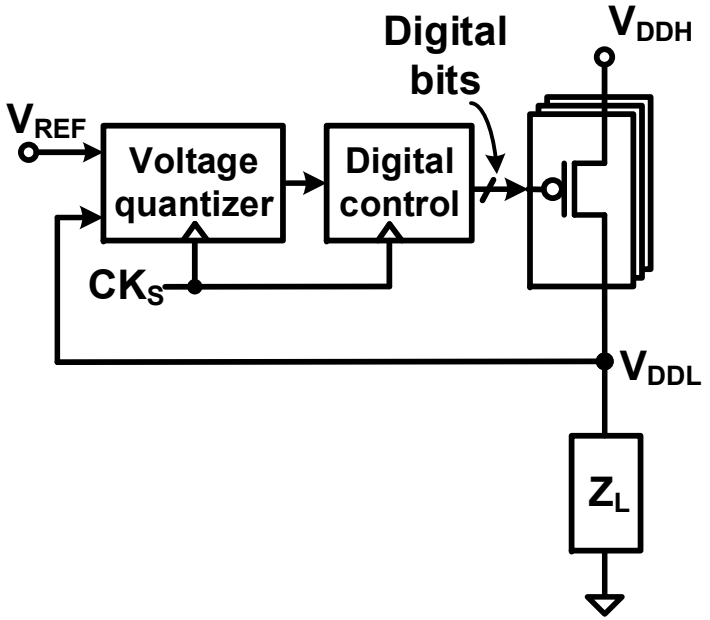
- Background: Analog vs. Digital LDO
- Time based Digital LDO
- Beat-Frequency Quantizer
- Active Voltage Positioning (AVP)
- 65nm Test Chip Results
- Conclusion

Analog vs. Digital LDO

Analog LDO



Digital LDO

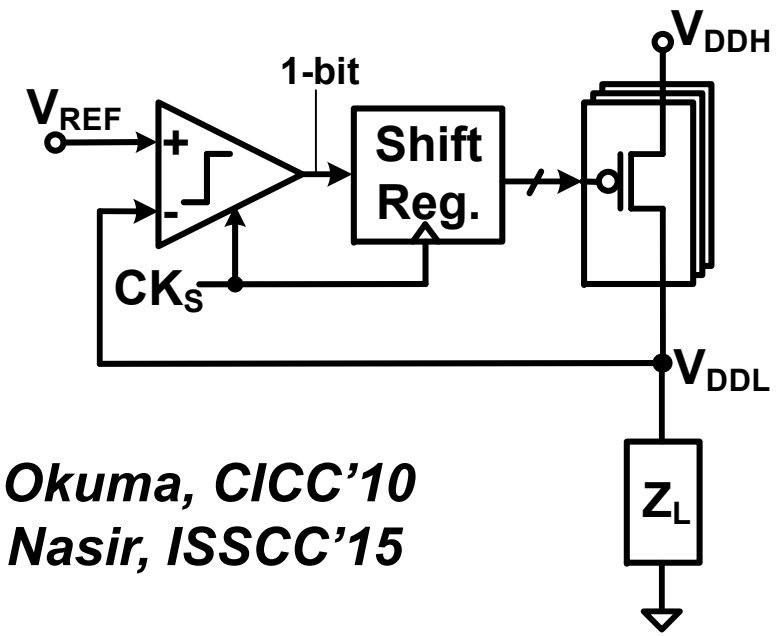


- **Benefits of digital implementation:**
  - ✓ Scalability with technology
  - ✓ Low voltage operation → DVFS
  - ✓ Loop parameters controlled digitally

Ref: Y. Okuma, CICC'10

Digital LDO Architectures

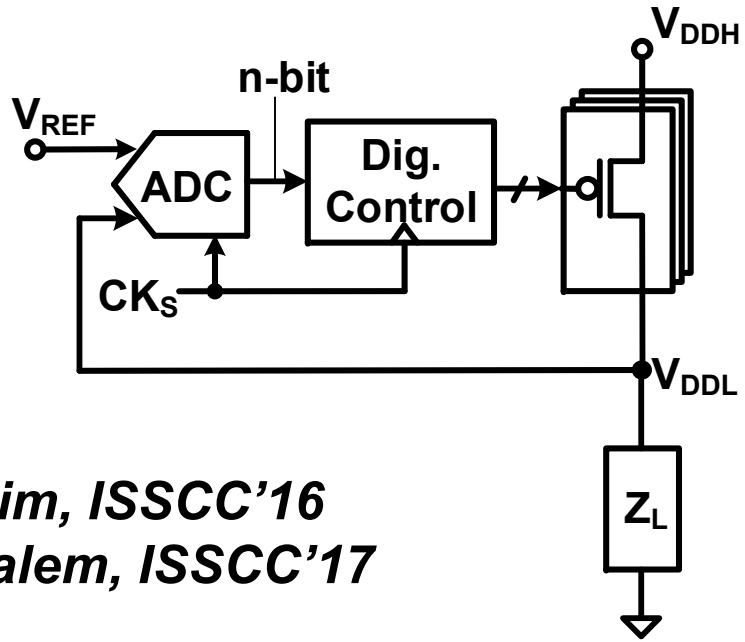
Single-bit Quantizer



Y. Okuma, CICC'10
S. Nasir, ISSCC'15

✓ Low complexity
X Slow response
X Poor stability

Multi-bit Quantizer



D. Kim, ISSCC'16
L. Salem, ISSCC'17

X High complexity
✓ Fast response
✓ Good stability

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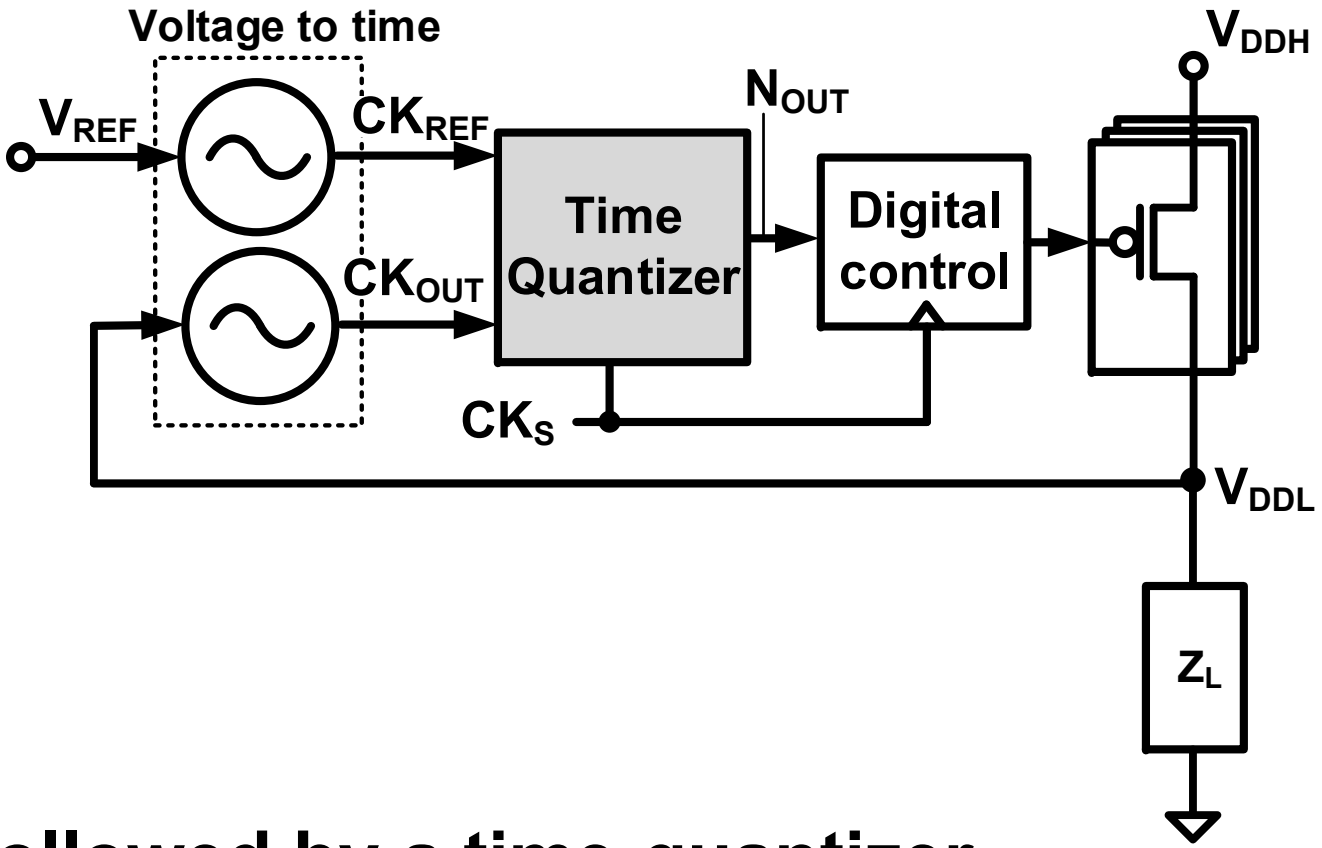
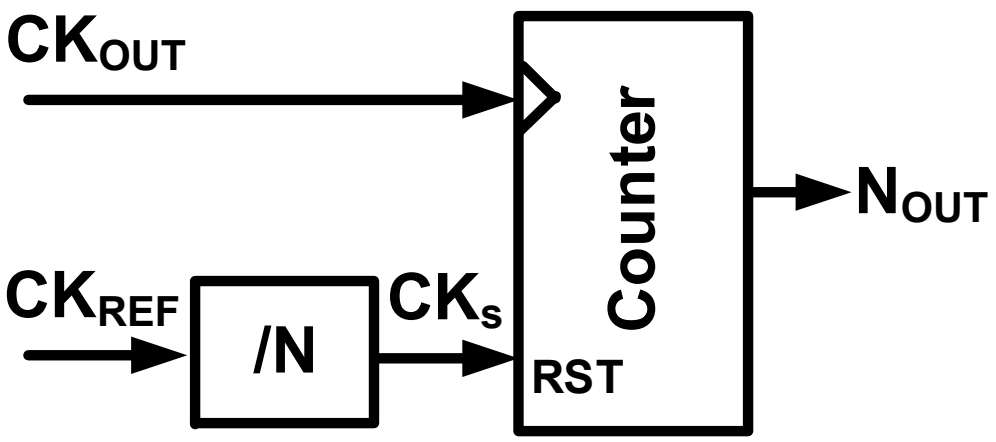
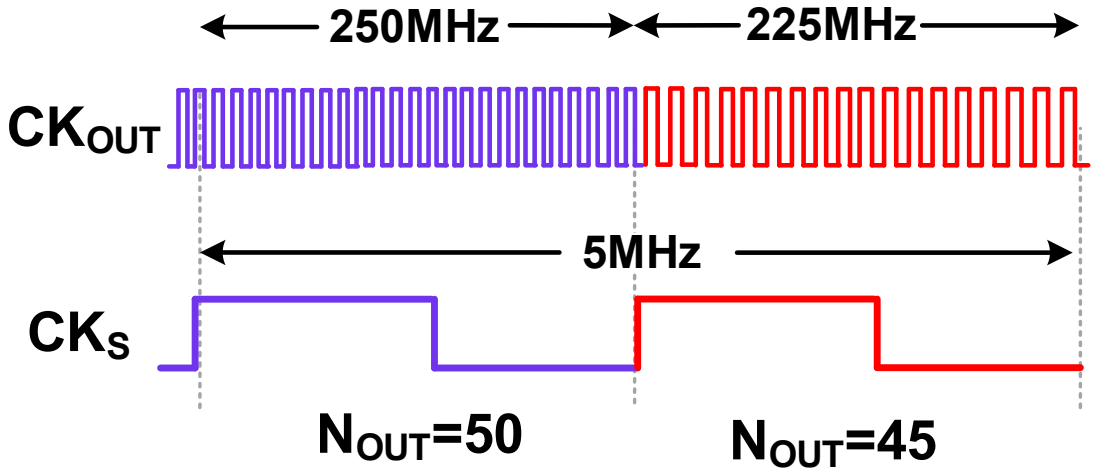
Time based Digital LDO



- VCO followed by a time-quantizer
- Fully digital voltage quantization
- 1st order quantization noise shaping

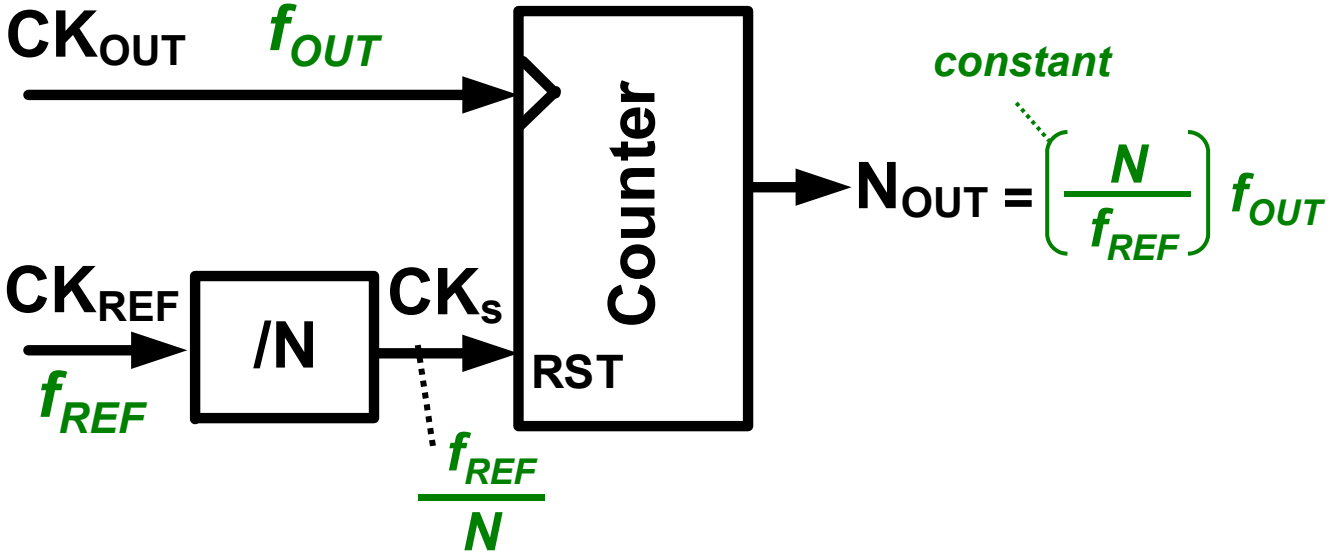
Conventional Linear Time-Quantizer

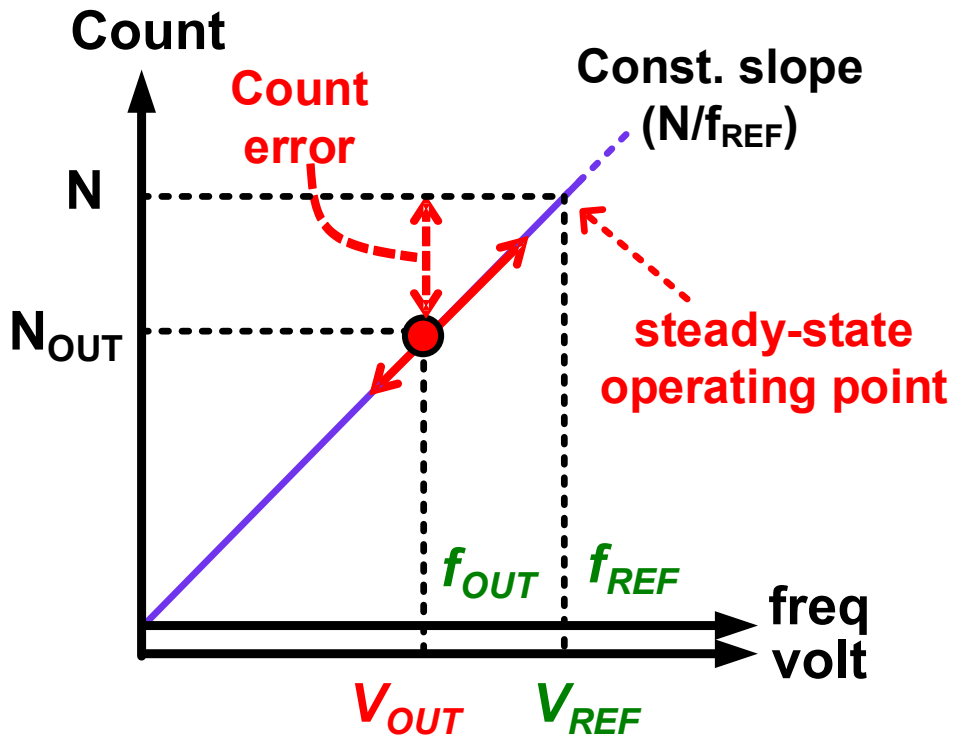




- N_{OUT} = # of CK_{OUT} periods within a sampling period
- Constant sampling period

Conventional Linear Time-Quantizer





- N_{OUT} proportional to CK_{OUT}
- $|N-N_{OUT}|$ provides amount of pMOS switching
- Large N improves resolution but slow response

Trade-off between speed and power/stability

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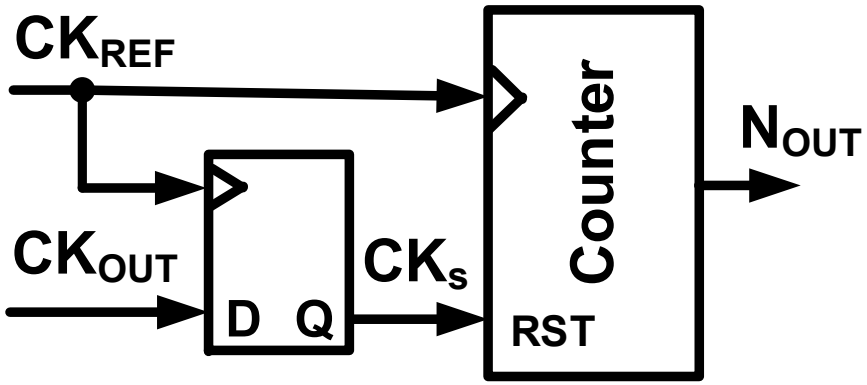
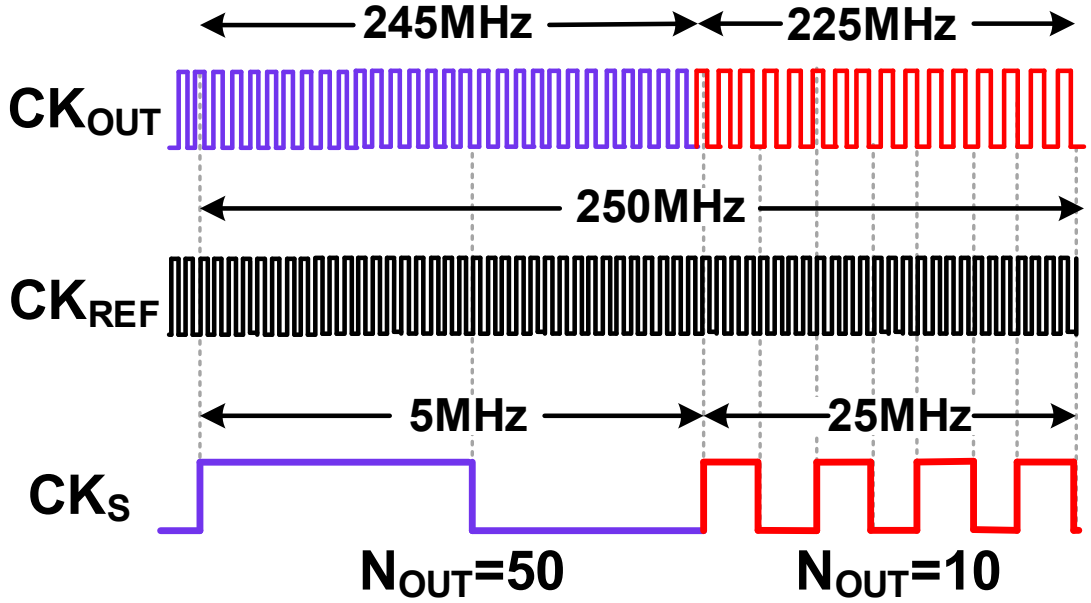
Proposed Beat Frequency Time-Quantizer

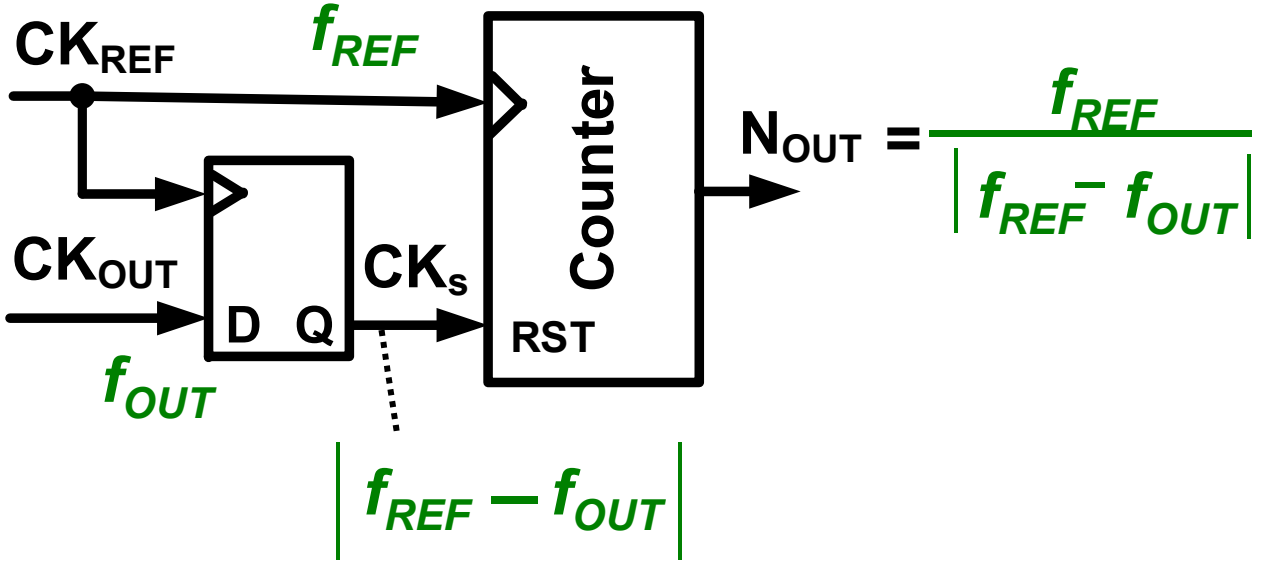




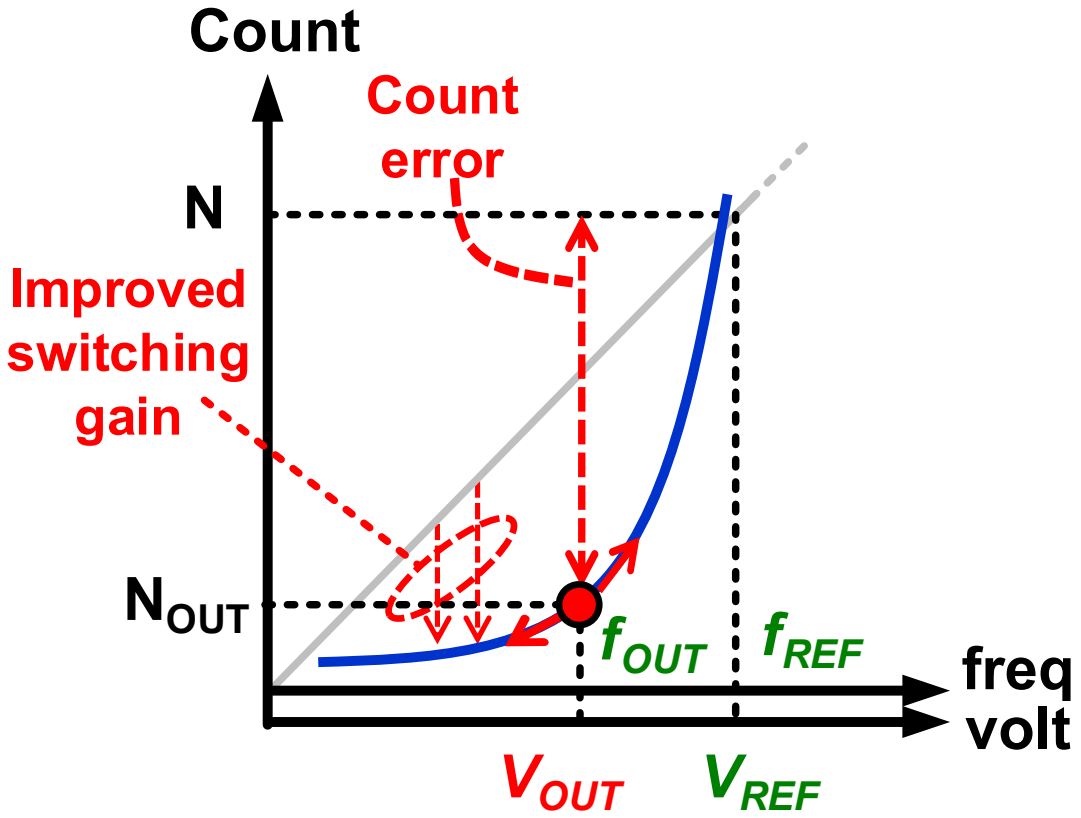
- D-flip-flop acts as a beat frequency generator
- Larger frequency difference generates higher f_S

B. Kim, VLSI'15 (BF-PLL)
S. Kundu, CICC'15 (BF-ADC)
This work (BF-LDO)

Proposed Beat Frequency Time-Quantizer

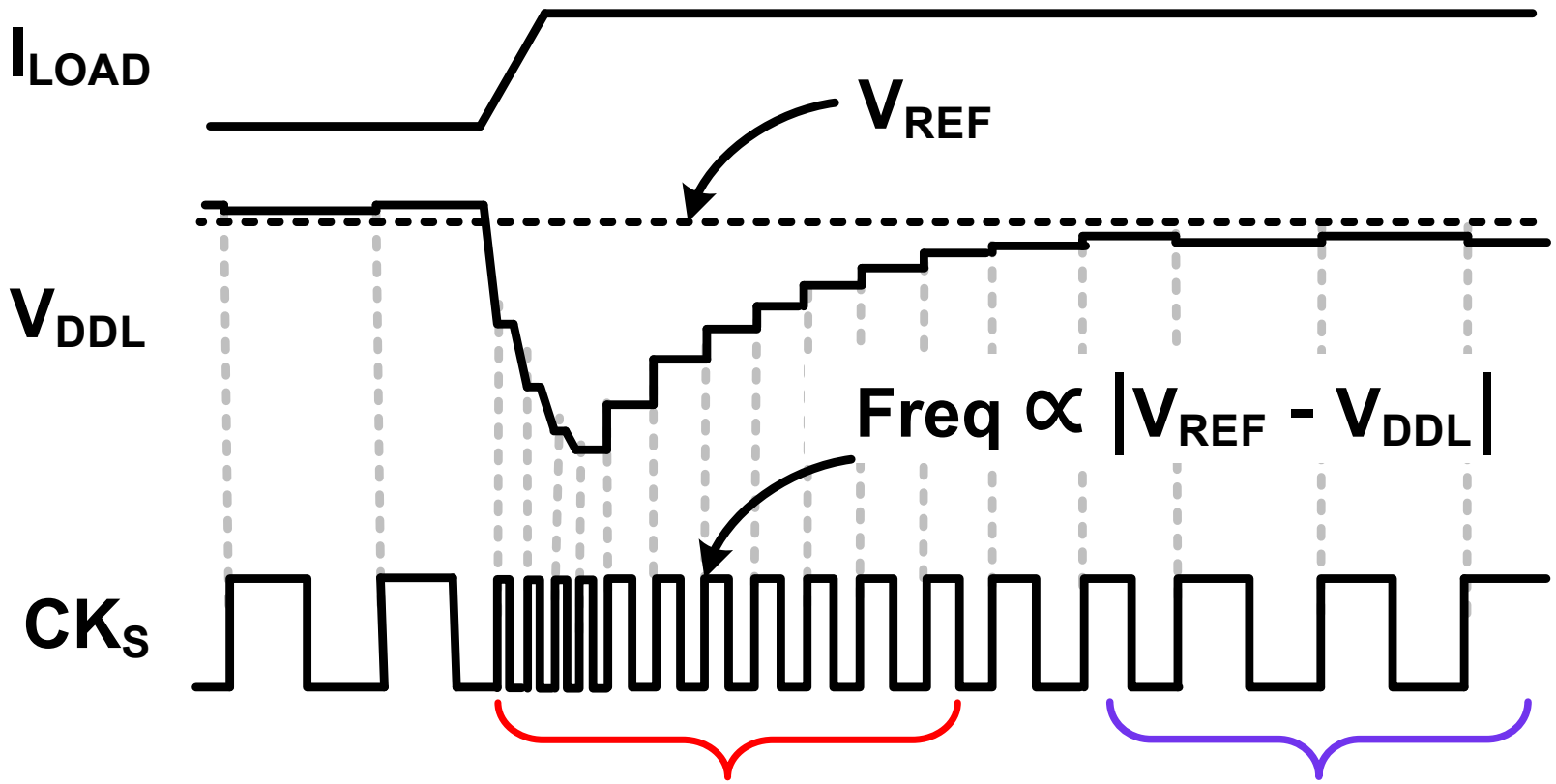


$$N_{OUT} = \frac{f_{REF}}{|f_{REF} - f_{OUT}|}$$



- When | V_{REF} – V_{OUT} | is larger:
  - pMOS switching frequency becomes faster
  - pMOS switching amount increases due to large |N - N_{OUT}|

Beat Frequency for Adaptive Sampling



- Fast settling
- low droop

- High resolution
- Low dyn. Power
- Good stability

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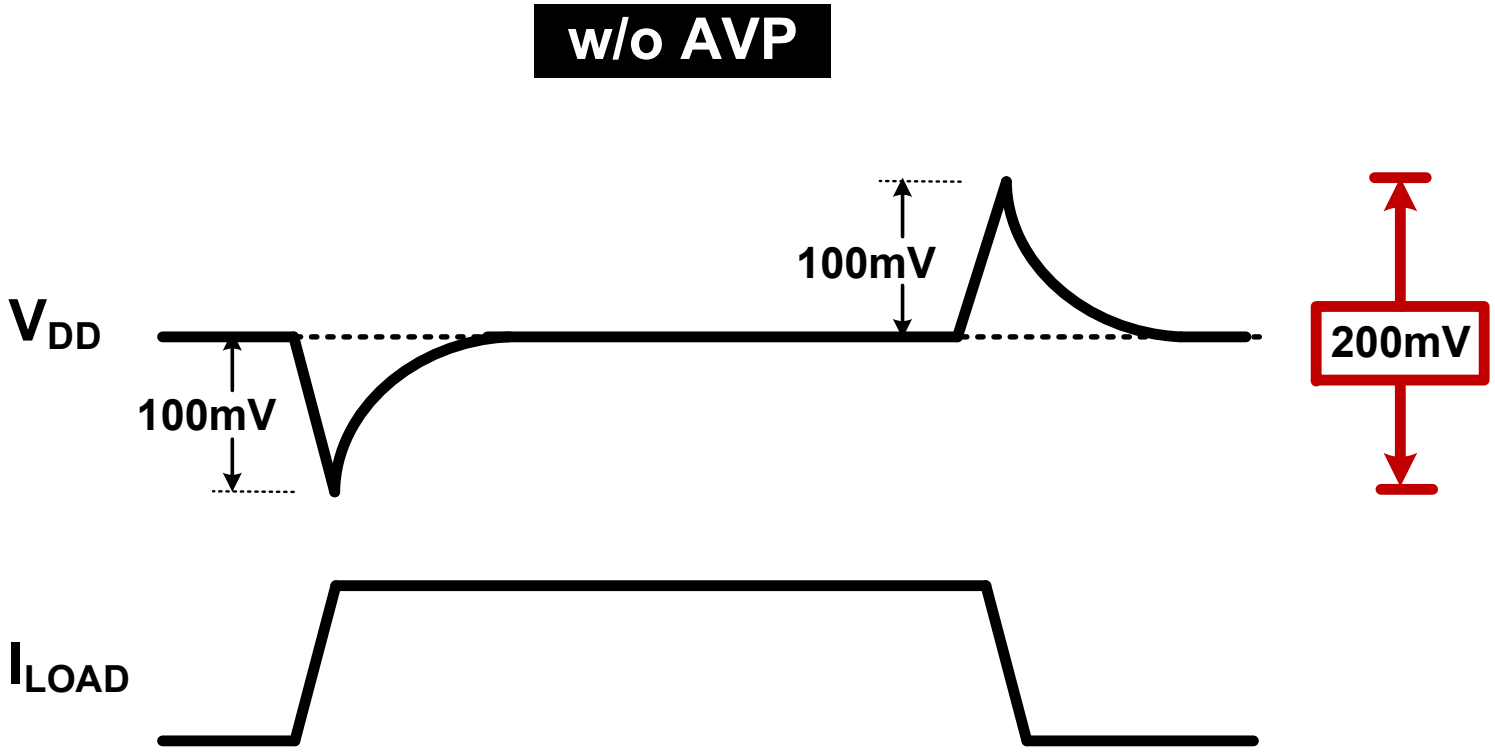
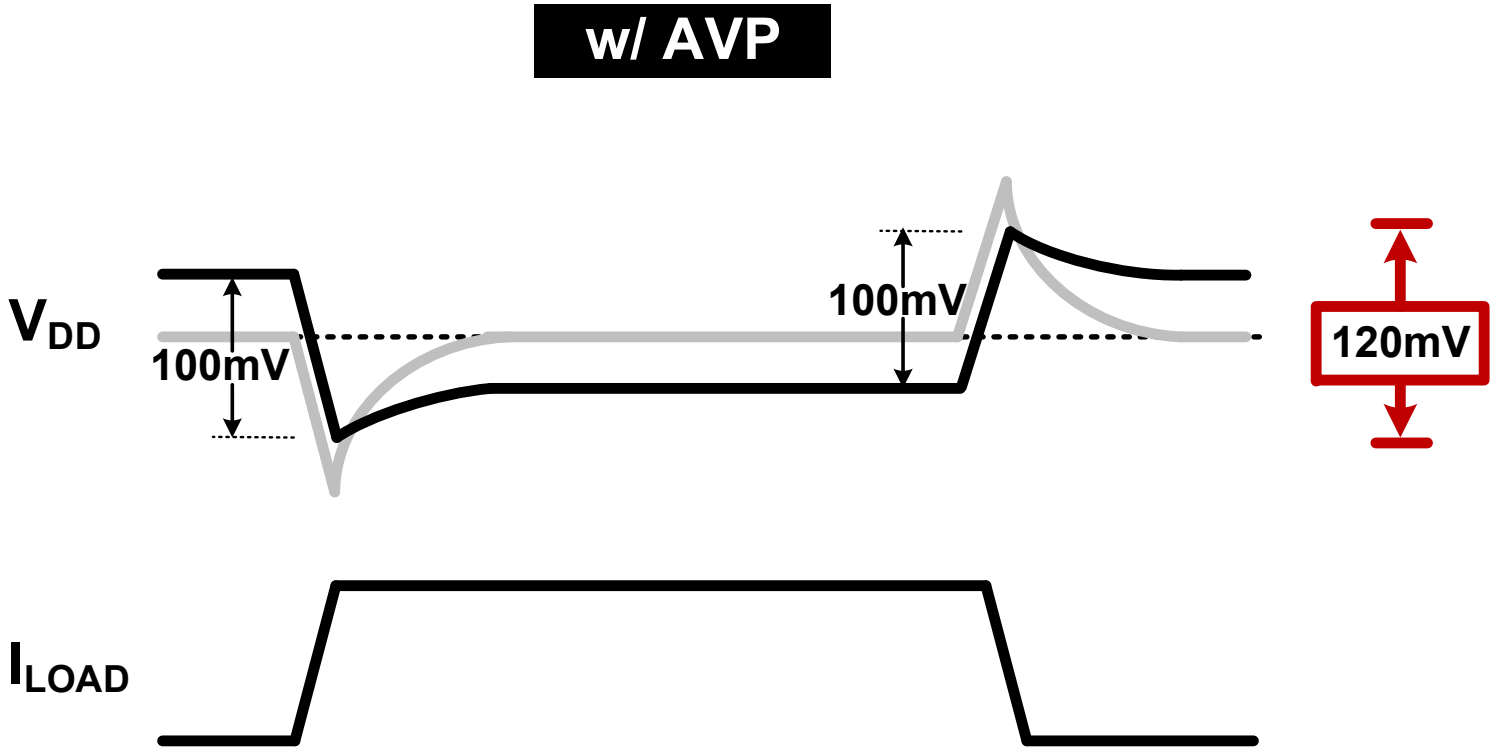
Active Voltage Positioning



Ref: K. Yao, APEC'2004

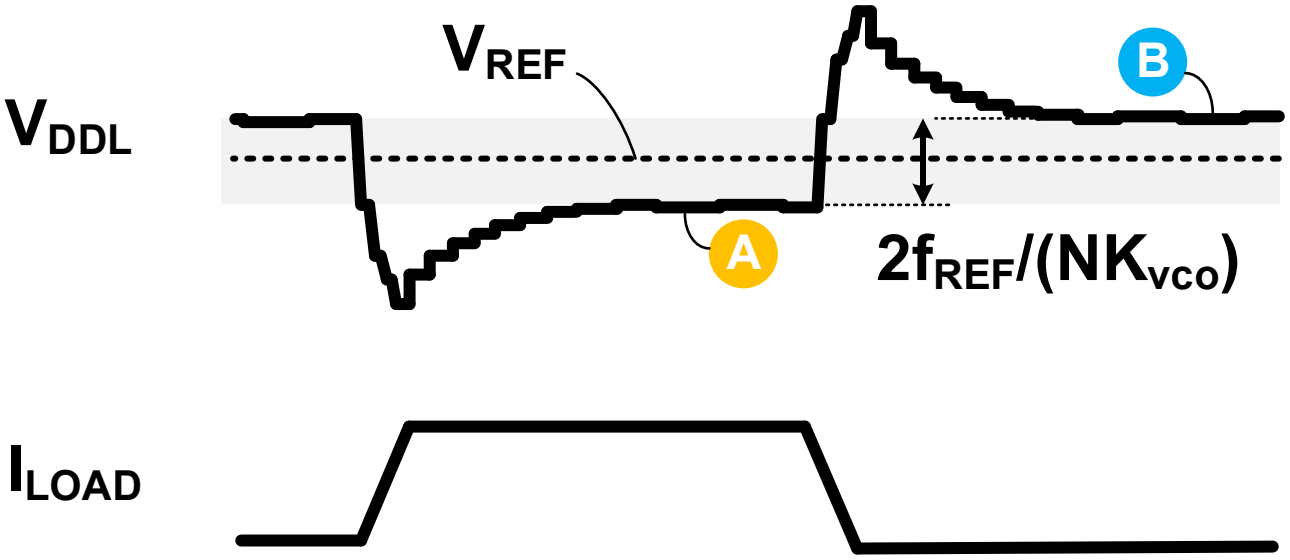
Active Voltage Positioning

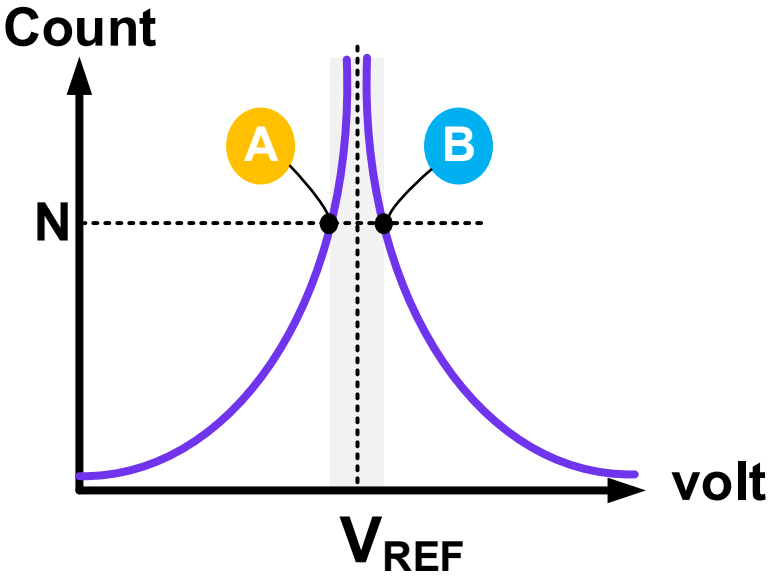


Ref: K. Yao, APEC'2004

Active Voltage Positioning

BF Quantizer





- BF quantizer provides inherent AVP
- Voltage position is set by N

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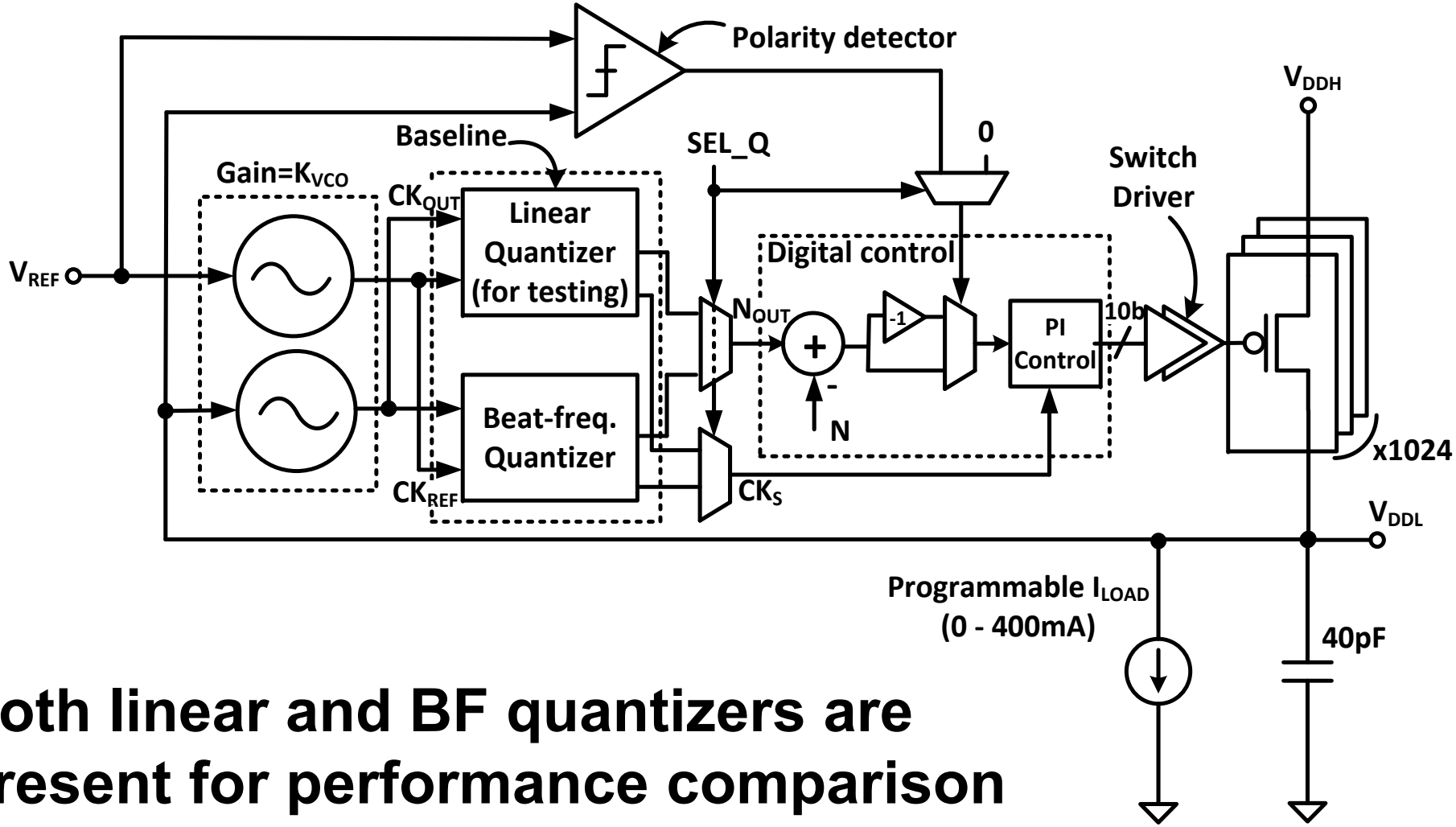
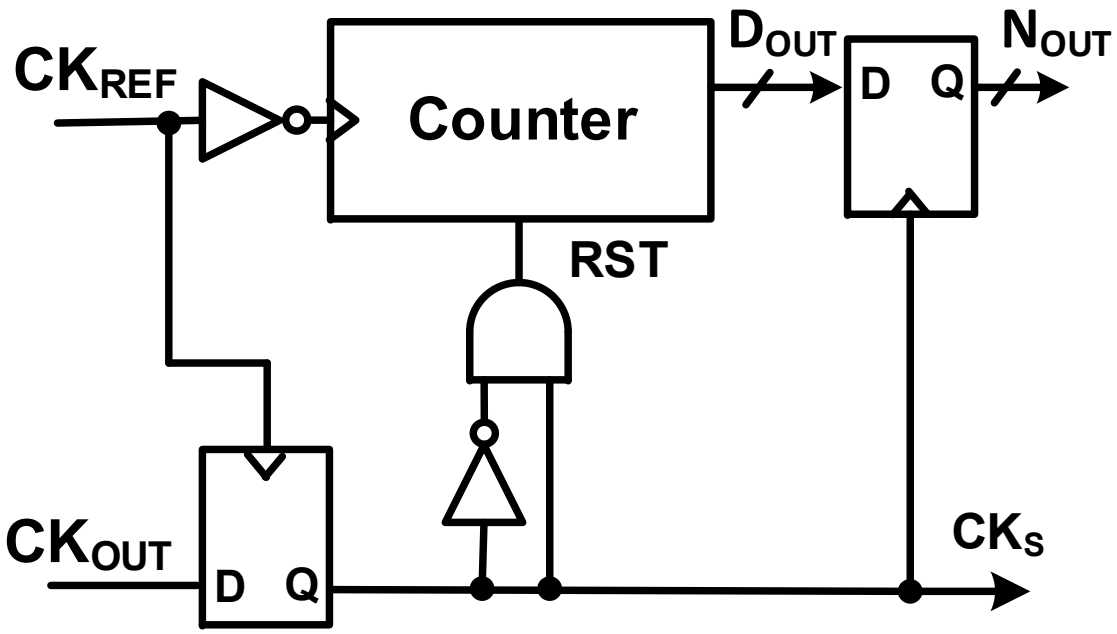
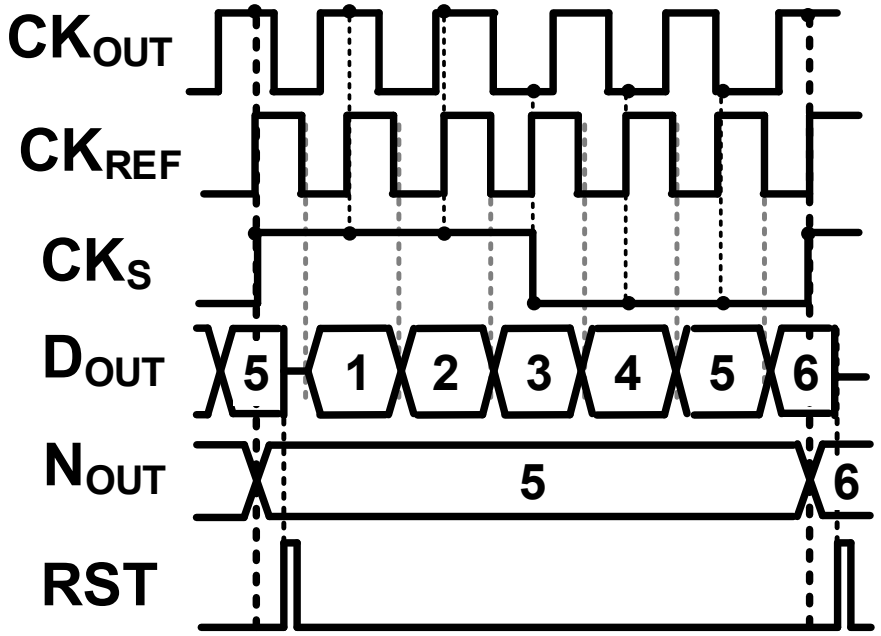
Complete Block Diagram of Digital LDO



- **Both linear and BF quantizers are present for performance comparison**

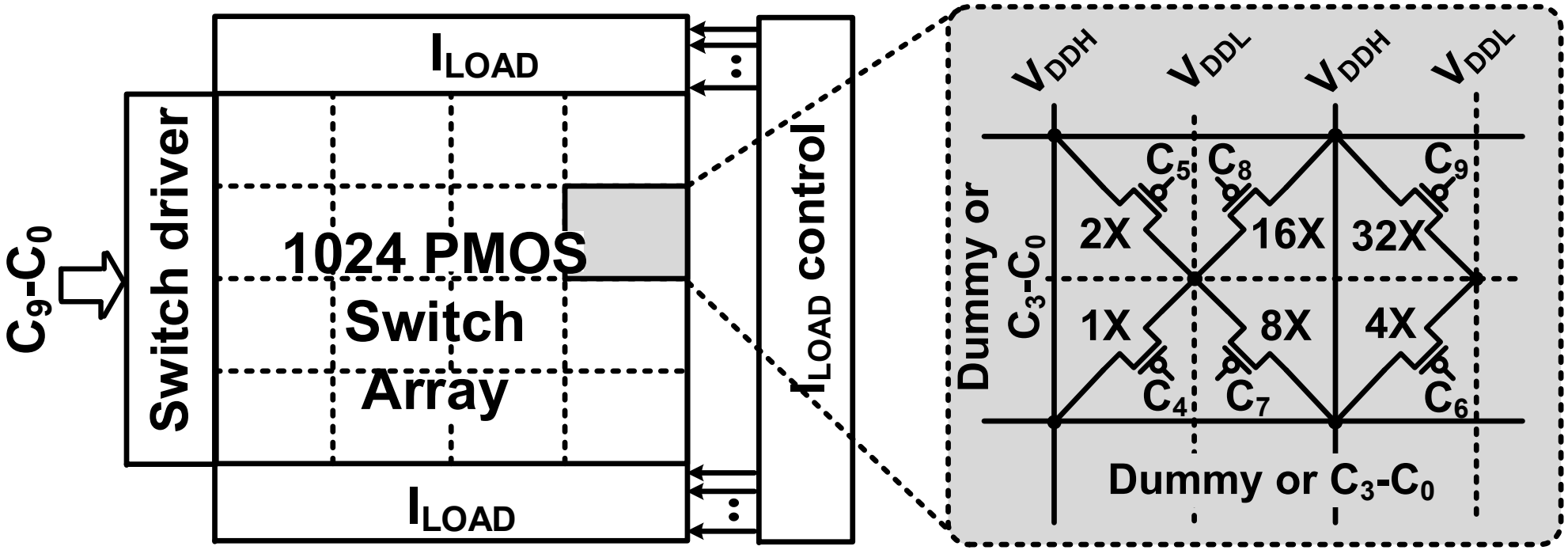
BF Quantizer Design





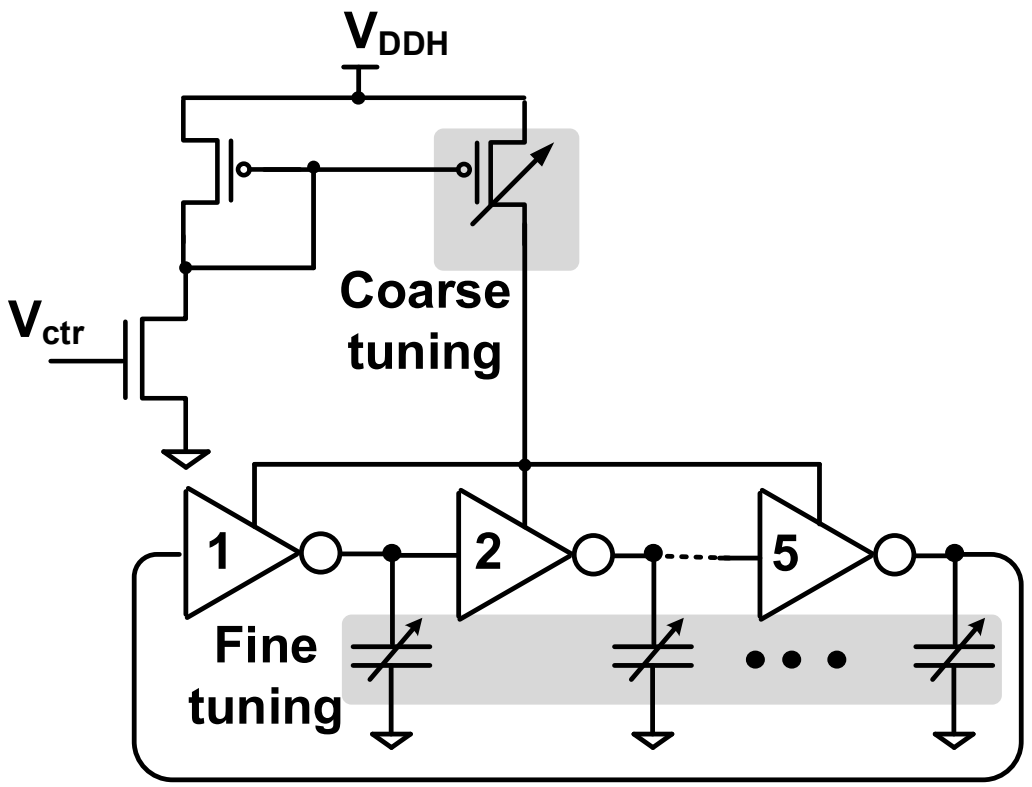
- An 8-bit counter counts the number of CK_{REF} periods in a beat period
- Counter resets at the beginning of each beat period

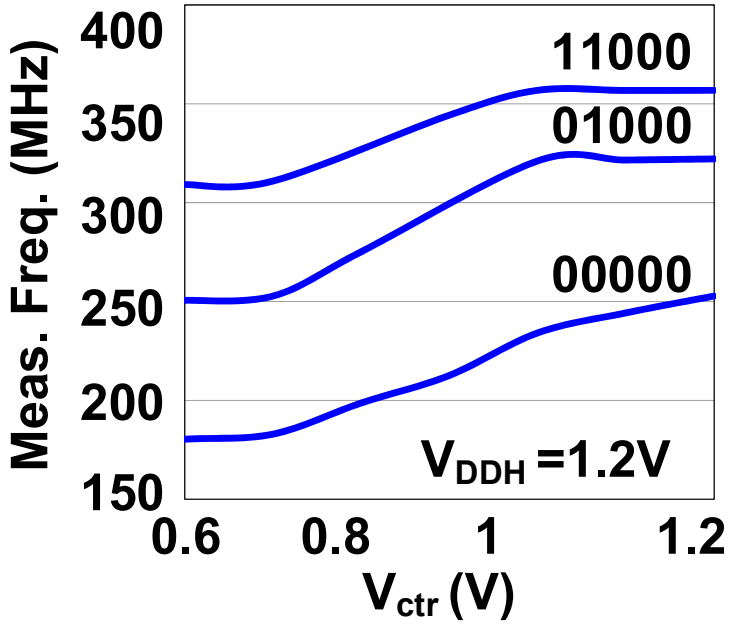
PMOS Switch Array and Driver



- **Uniformly distributed layout for matching**
- **Equal loading for all bits (C_9-C_0) using dummies**

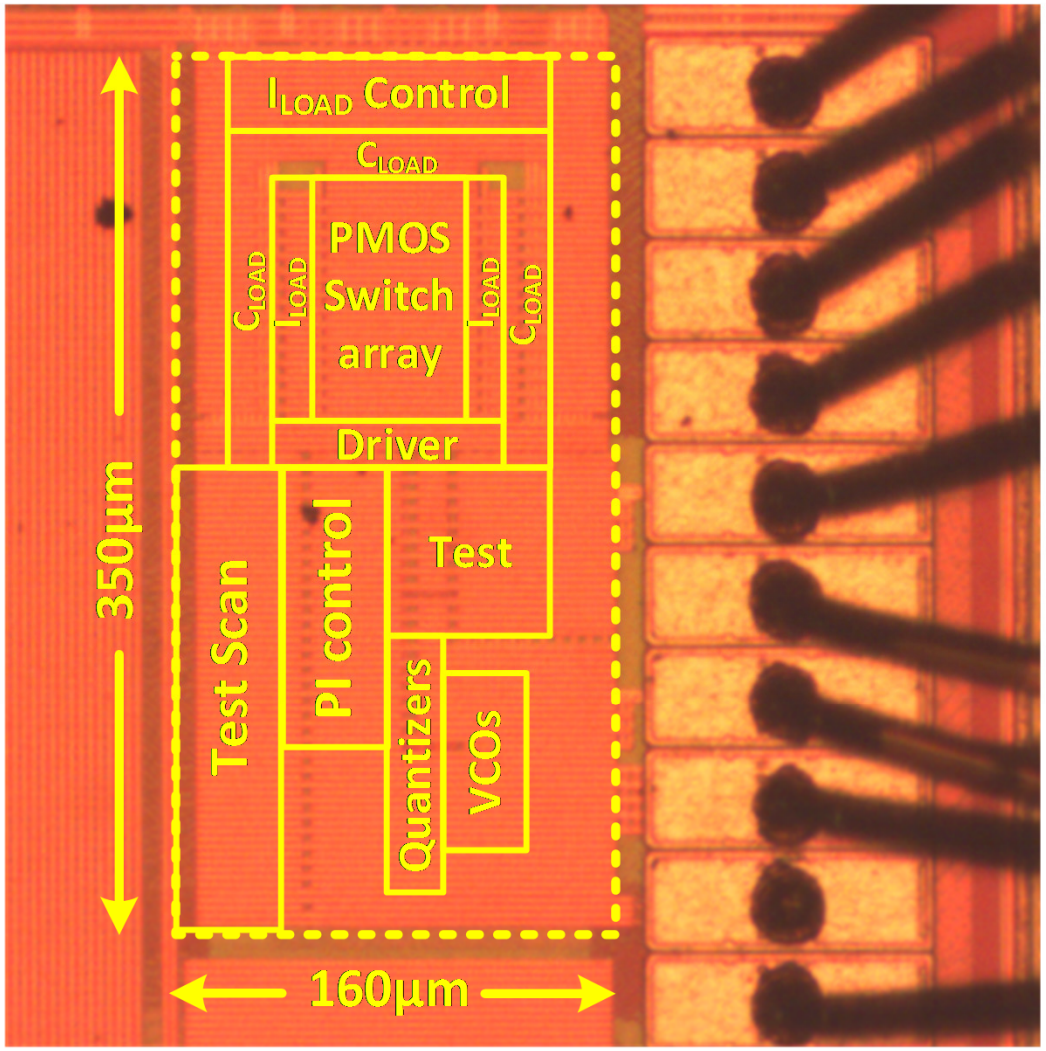
VCO Schematic





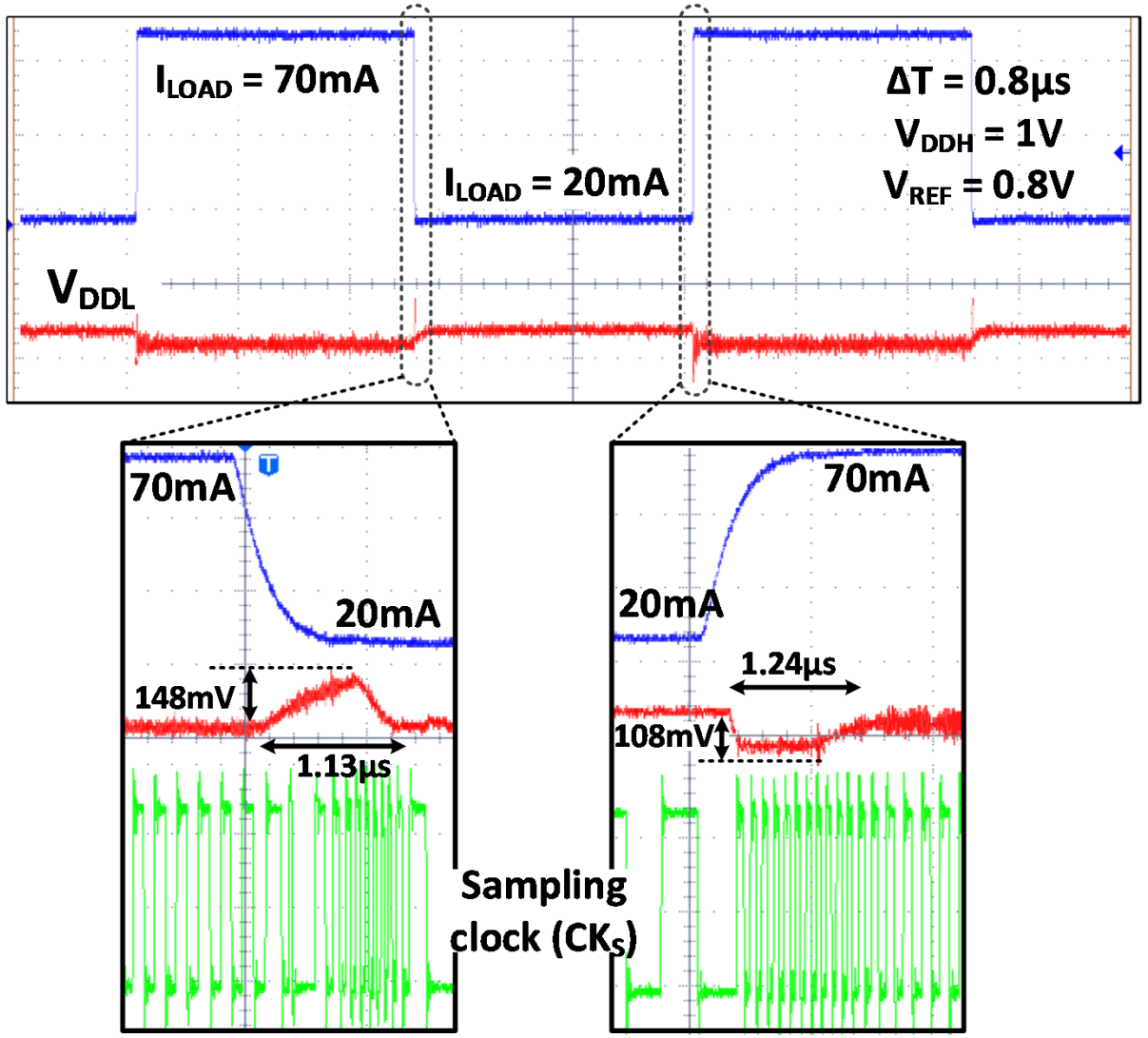
- Coarse tuning: wide range of input/output voltage
- Fine tuning: compensates any mismatch between VCO pair

65nm Chip Micrograph



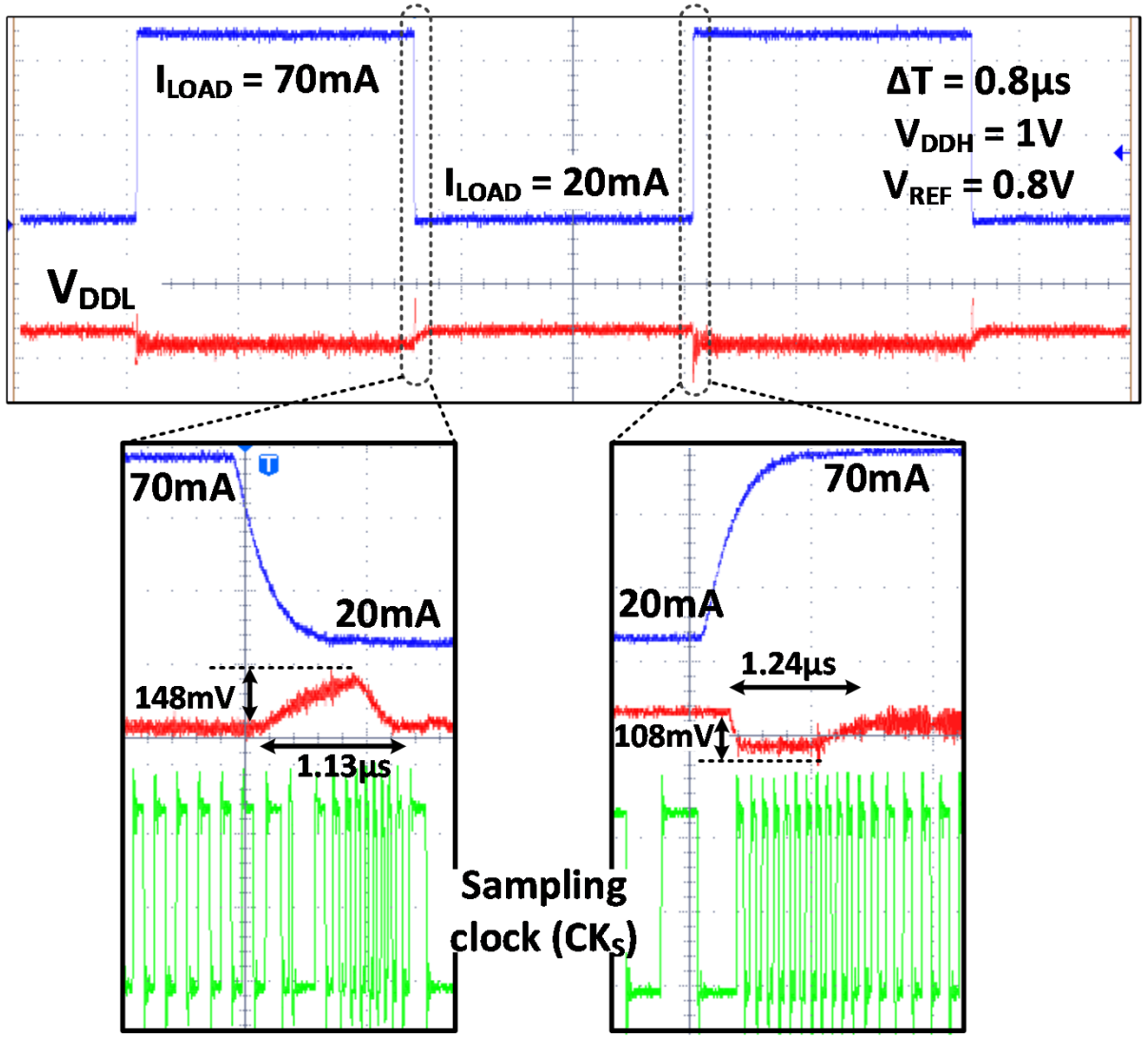
Chip Area
Core: 0.0374 mm^2
Test circuits: 0.0186 mm^2
Total: 0.056 mm^2

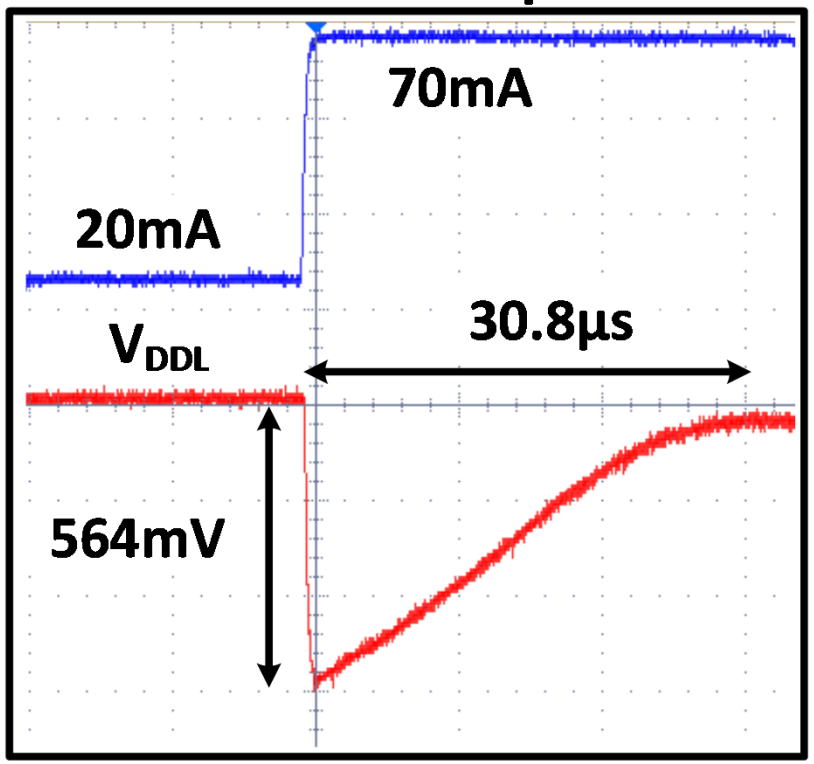
Measured Transient Response: I_{LOAD} step



- Higher sampling frequency during I_{LOAD} transition
- 108mV droop and 148mV overshoot for 50mA I_{LOAD} step

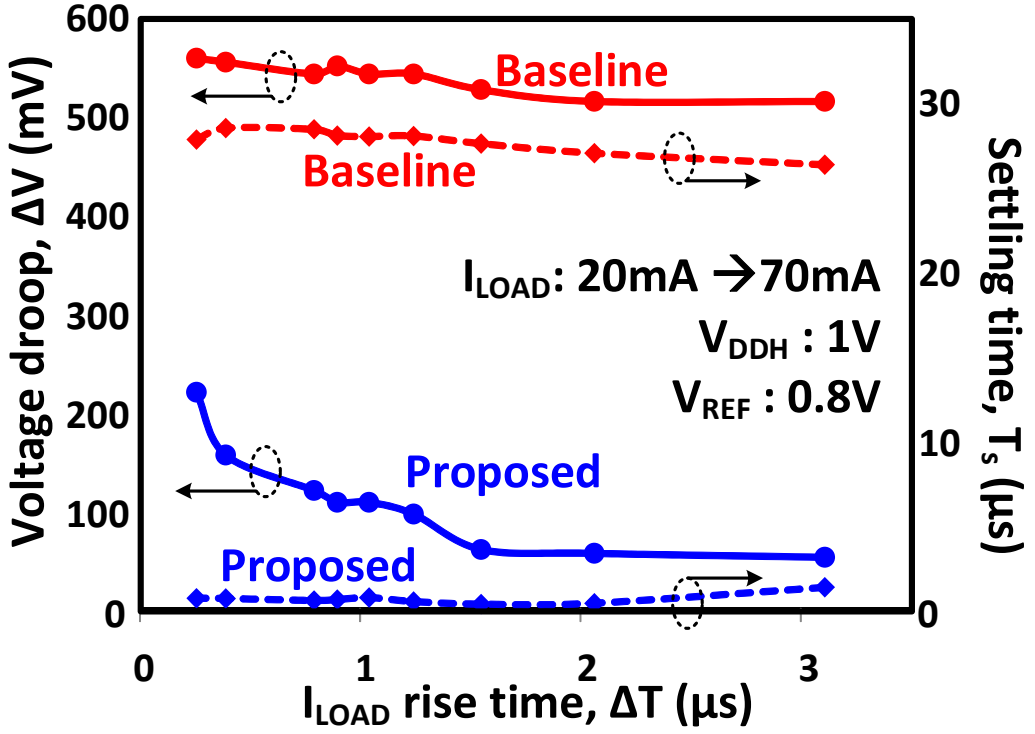
Measured Transient Response: I_{LOAD} step

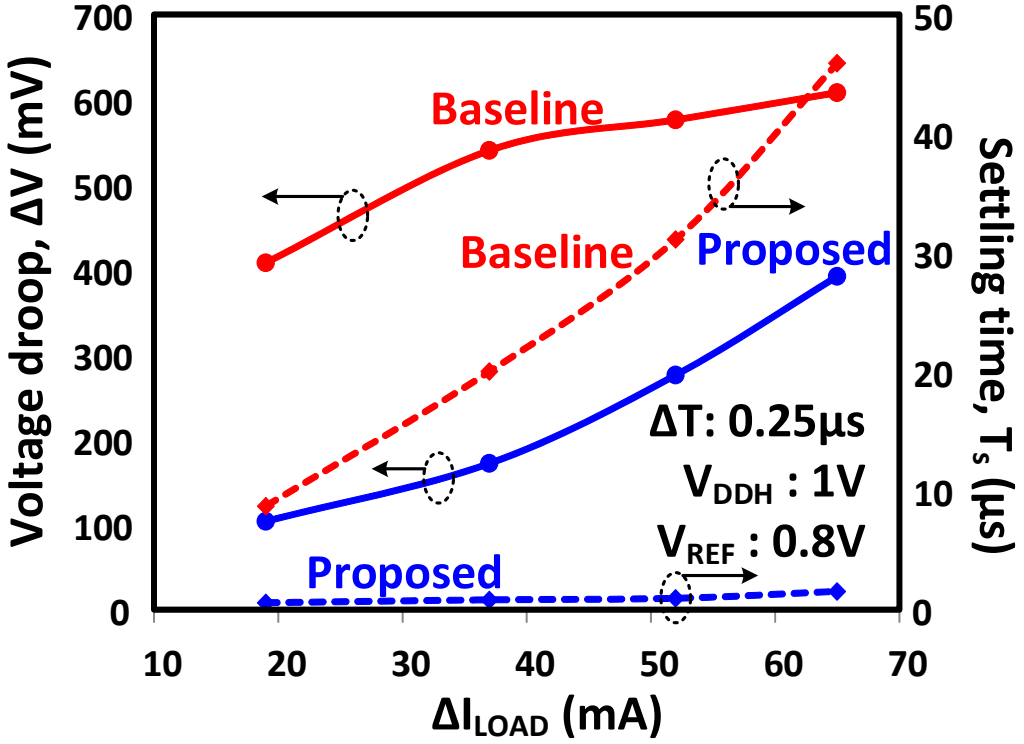




- 5x droop and 25x settling time for baseline

Voltage Droop and Settling Time Measurements

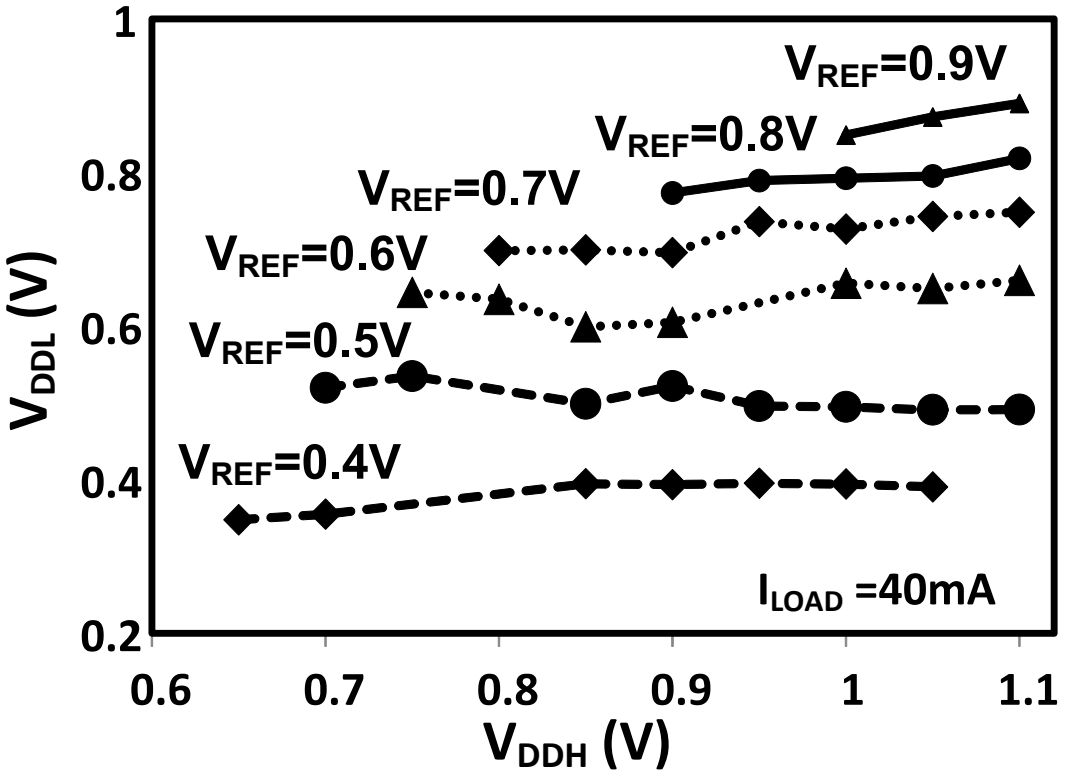


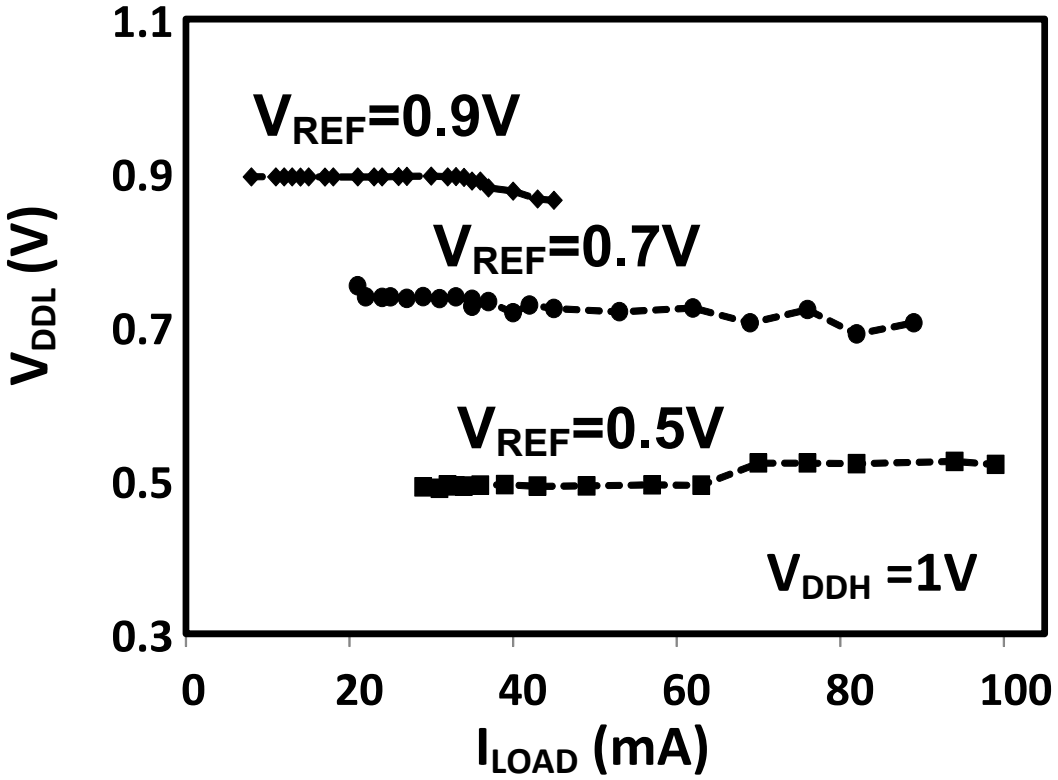


- ΔV improvement: 5X – 10X
- T_s improvement: 20X – 35X

- ΔV improvement: 1.5X – 4X
- T_s improvement: 15X – 30X

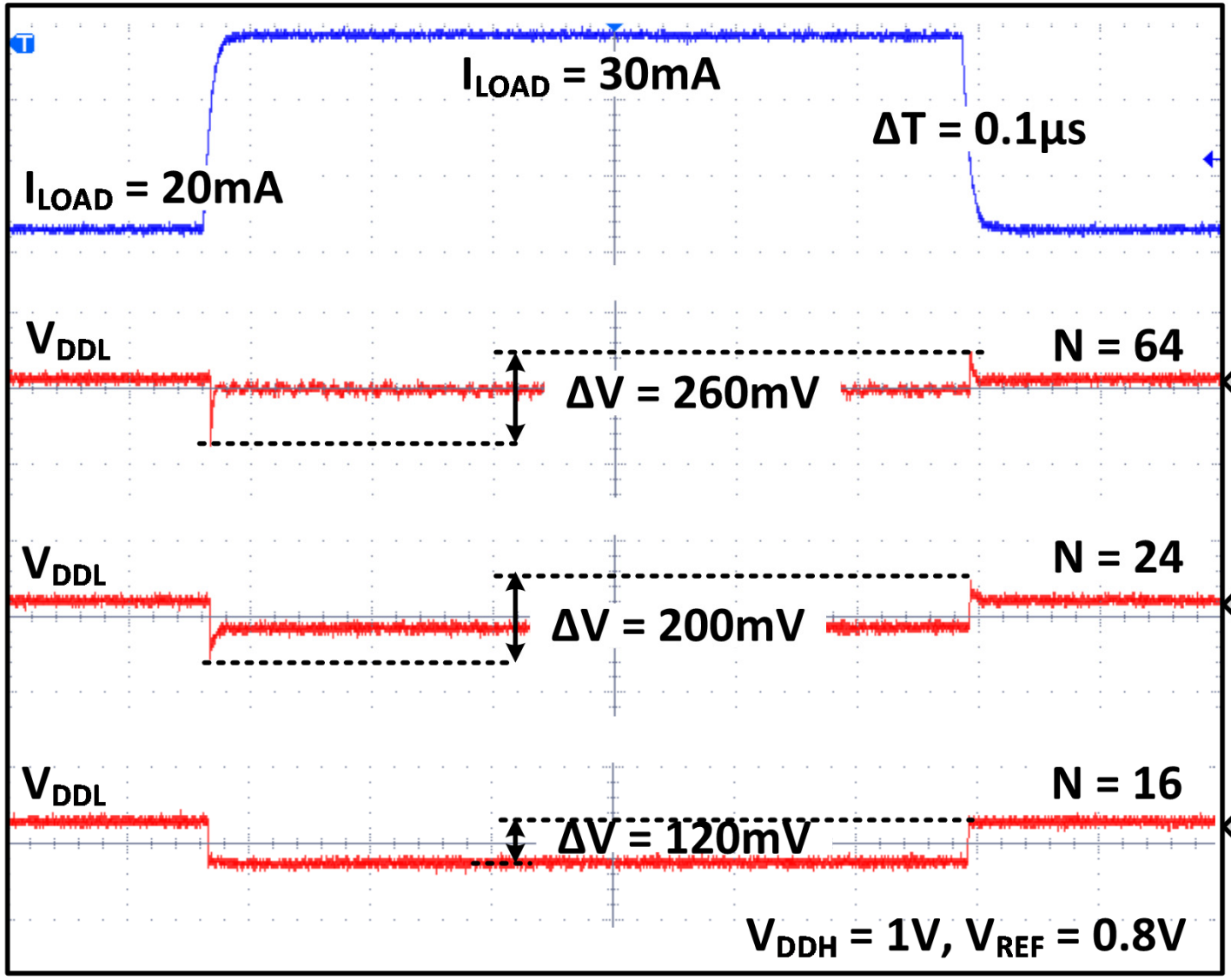
Measured Line and Load Regulation





- Line regulation for V_{REF} > 0.4V
- Load regulation for 10x variation in I_{LOAD}

Active Voltage Positioning Measurements

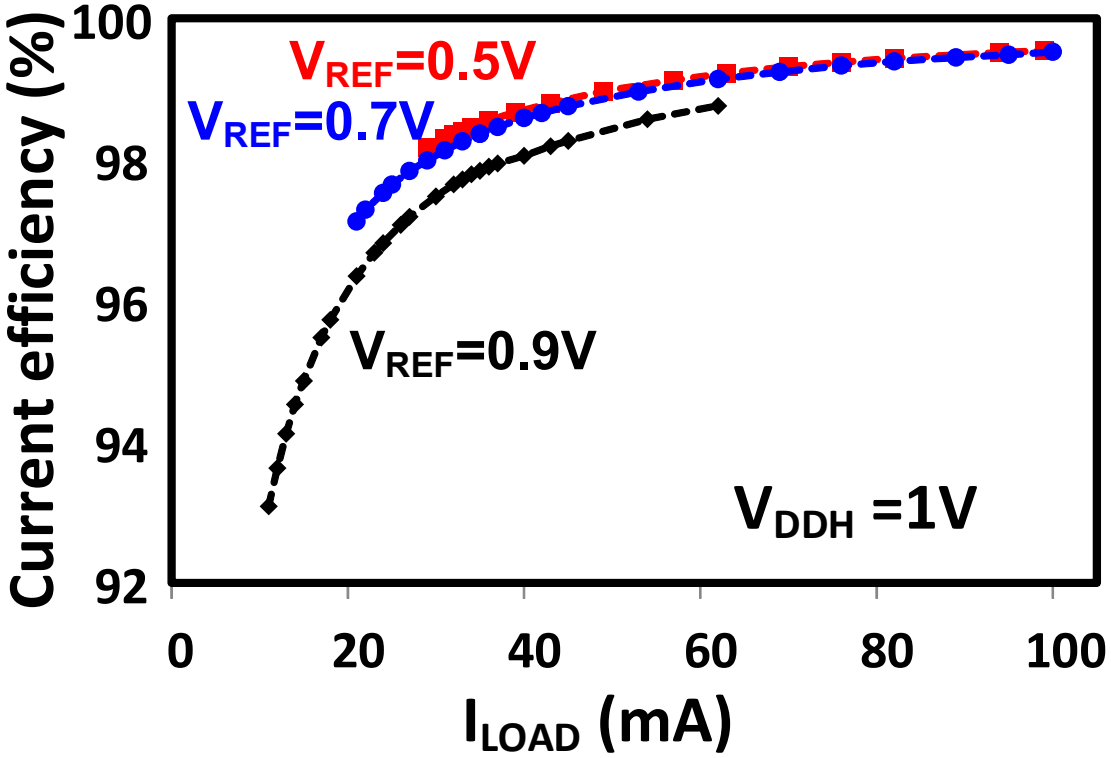


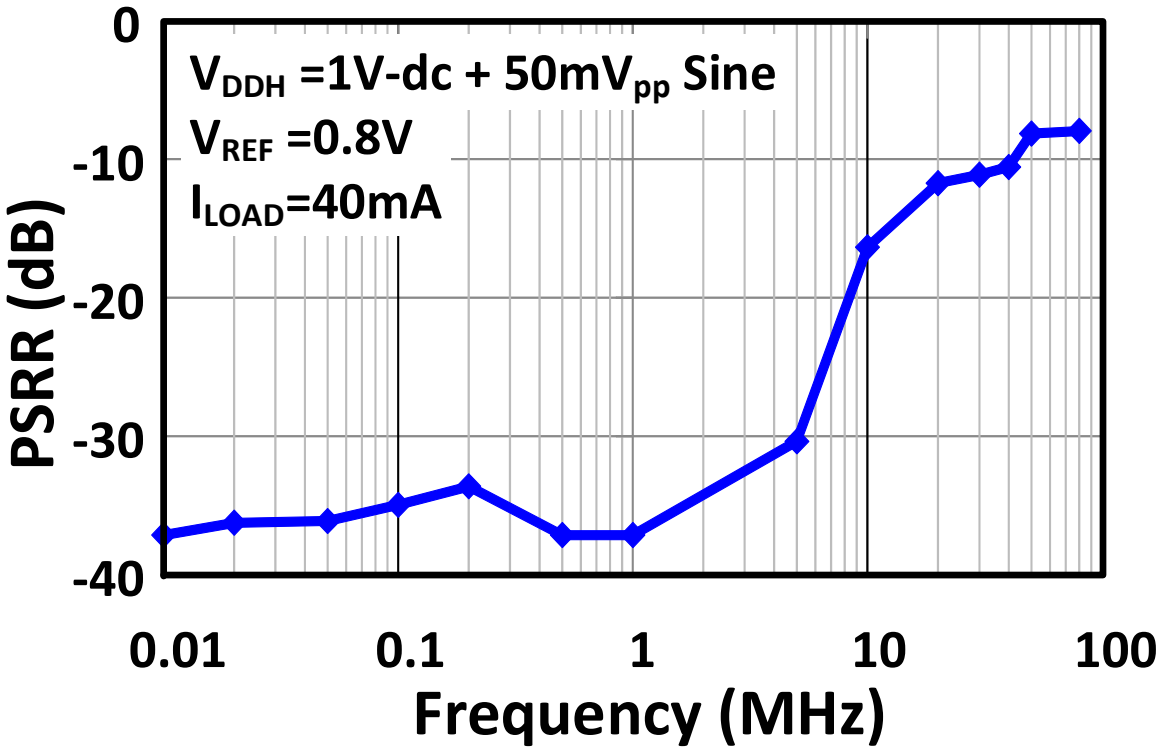
Weak AVP
DC regulation=4%

Moderate AVP
DC regulation=8%

Strong AVP
DC regulation=15%

Measured Current Efficiency and PSRR





- Current efficiency >93% for 10-100mA I_{LOAD} with max of 99.5%
- Low frequency PSRR of -38dB

Performance Comparison Table

	Nasir, ISSCC'15	Lee, ISSCC'16	Salem, ISSCC'17	Kim, ISSCC'17	This Work
Process	130nm	28nm	65nm	65nm	65nm
Architecture	Shift Reg	Shift Reg+ADC	SAR ADC	Event-driven ADC	VCO based ADC
Adaptive sampling/ AVP	Yes / No	No / No	No / No	Yes / No	Yes / Yes
V_{LDO_IN}(V)	0.5– 1.2	1.1	0.5– 1	0.45– 1	0.6– 1.2
V_{LDO_OUT}(V)	0.45– 1.14	0.9	0.3– 0.45	0.4– 0.95	0.4– 1.1
Max .I_{LOAD} (mA)	4.6	200	2	3.36	100
I_Q (mA)	0.024– 0.22	0.11	0.014	0.08– 0.26	0.1– 1.07
C_{LOAD} (nF)	1	23.5	0.4 (Integrated)	0.1 (Integrated)	0.04 (Integrated)
Max current efficiency (%)	98.3	99.94	99.8	99.2	99.5
ΔV,Ts @ΔI_{LOAD}	90mV,1.1µs@ 1.4mA	120mV,40 µs# @180mA	40mV,0.1µs @1.06mA	34mV.11.2µs @1.44mA	108mV,1.24µs @50mA
Area (mm^2)	0.355	0.021	0.0023*	0.03*	0.0374
FOM (ps)**	10100	9.57	199	20	1.38

From oscilloscope waveform *Without C_{LOAD} **FOM=$C_{LOAD}\Delta V*I_Q/(\Delta I_{LOAD})^2$. Smaller FOMs are better

Conclusion

- A fully integrated digital LDO using VCO based time quantization
- Adaptive sampling clock utilizing beat-frequency
- Built-in active voltage positioning
- Measured max current efficiency is 99.5% with FOM of 1.38ps in 65nm CMOS