A Fully Integrated 40pF Output Capacitor Beat-Frequency-Quantizer-Based Digital LDO with Built-In Adaptive Sampling and Active Voltage Positioning

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Outline

- Background: Analog vs. Digital LDO
- Time based Digital LDO
- Beat-Frequency Quantizer
- Active Voltage Positioning (AVP)
- 65nm Test Chip Results
- Conclusion
Analog vs. Digital LDO

• Benefits of digital implementation:
  ✓ Scalability with technology
  ✓ Low voltage operation → DVFS
  ✓ Loop parameters controlled digitally

Ref: Y. Okuma, CICC’10
Digital LDO Architectures

Single-bit Quantizer

- Low complexity
- Slow response
- Poor stability

Y. Okuma, CICC’10
S. Nasir, ISSCC’15

Multi-bit Quantizer

- High complexity
- Fast response
- Good stability

D. Kim, ISSCC’16
L. Salem, ISSCC’17
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Time based Digital LDO

- VCO followed by a time-quantizer
- Fully digital voltage quantization
- $1^{st}$ order quantization noise shaping
Conventional Linear Time-Quantizer

- \( N_{\text{OUT}} \) = \# of \( CK_{\text{OUT}} \) periods within a sampling period
- Constant sampling period
Conventional Linear Time-Quantizer

- $N_{OUT}$ proportional to $CK_{OUT}$
- $|N-N_{OUT}|$ provides amount of pMOS switching
- Large $N$ improves resolution but slow response

Trade-off between speed and power/stability
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Proposed Beat Frequency Time-Quantizer

- D-flip-flop acts as a beat frequency generator
- Larger frequency difference generates higher \( f_S \)

B. Kim, VLSI’15 (BF-PLL)
S. Kundu, CICC’15 (BF-ADC)
This work (BF-LDO)
Proposed Beat Frequency Time-Quantizer

- When $|V_{REF} - V_{OUT}|$ is larger:
  - pMOS switching frequency becomes faster
  - pMOS switching amount increases due to large $|N - N_{OUT}|$

Count

$N_{OUT} = \frac{f_{REF}}{f_{REF} - f_{OUT}}$
Beat Frequency for Adaptive Sampling

- Fast settling
- Low droop
- High resolution
- Low dyn. Power
- Good stability
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Active Voltage Positioning

Ref: K. Yao, APEC’2004
Active Voltage Positioning

Ref: K. Yao, APEC'2004
Active Voltage Positioning

BF Quantizer

- BF quantizer provides inherent AVP
- Voltage position is set by N
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Both linear and BF quantizers are present for performance comparison.
BF Quantizer Design

- An 8-bit counter counts the number of $\text{CK}_{\text{REF}}$ periods in a beat period
- Counter resets at the beginning of each beat period
• Uniformly distributed layout for matching
• Equal loading for all bits ($C_9$-$C_0$) using dummies
VCO Schematic

- Coarse tuning: wide range of input/output voltage
- Fine tuning: compensates any mismatch between VCO pair
65nm Chip Micrograph

<table>
<thead>
<tr>
<th>Chip Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core: 0.0374 mm²</td>
</tr>
<tr>
<td>Test circuits: 0.0186 mm²</td>
</tr>
<tr>
<td>Total: 0.056 mm²</td>
</tr>
</tbody>
</table>
Measured Transient Response: $I_{\text{LOAD}}$ step

- Higher sampling frequency during $I_{\text{LOAD}}$ transition
- 108mV droop and 148mV overshoot for 50mA $I_{\text{LOAD}}$ step
Measured Transient Response: $I_{\text{LOAD}}$ step

- 5x droop and 25x settling time for baseline
Voltage Droop and Settling Time Measurements

- ΔV improvement: 5X – 10X
- $T_s$ improvement: 20X – 35X

- ΔV improvement: 1.5X – 4X
- $T_s$ improvement: 15X – 30X
Measured Line and Load Regulation

- Line regulation for $V_{\text{REF}} > 0.4V$
- Load regulation for 10x variation in $I_{\text{LOAD}}$
Active Voltage Positioning Measurements

Weak AVP
DC regulation = 4%

Moderate AVP
DC regulation = 8%

Strong AVP
DC regulation = 15%

$I_{LOAD} = 20\text{mA}$

$V_{DDL}$

$\Delta V = 260\text{mV}$

$\Delta V = 200\text{mV}$

$\Delta V = 120\text{mV}$

$V_{DDL} = 1\text{V}$, $V_{REF} = 0.8\text{V}$

$I_{LOAD} = 30\text{mA}$

$\Delta T = 0.1\mu\text{s}$

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Measured Current Efficiency and PSRR

- Current efficiency >93% for 10-100mA $I_{LOAD}$ with max of 99.5%
- Low frequency PSRR of -38dB
## Performance Comparison Table

<table>
<thead>
<tr>
<th></th>
<th>Nasir, ISSCC’15</th>
<th>Lee, ISSCC’16</th>
<th>Salem, ISSCC’17</th>
<th>Kim, ISSCC’17</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>130nm</td>
<td>28nm</td>
<td>65nm</td>
<td>65nm</td>
<td>65nm</td>
</tr>
<tr>
<td>Architecture</td>
<td>Shift Reg</td>
<td>Shift Reg+ADC</td>
<td>SAR ADC</td>
<td>Event-driven ADC</td>
<td>VCO based ADC</td>
</tr>
<tr>
<td>Adaptive sampling/ AVP</td>
<td>Yes / No</td>
<td>No / No</td>
<td>No / No</td>
<td>Yes / No</td>
<td>Yes / Yes</td>
</tr>
<tr>
<td>$V_{\text{LDO,IN}}$ (V)</td>
<td>0.5– 1.2</td>
<td>1.1</td>
<td>0.5– 1</td>
<td>0.45– 1</td>
<td>0.6– 1.2</td>
</tr>
<tr>
<td>$V_{\text{LDO,OUT}}$ (V)</td>
<td>0.45– 1.14</td>
<td>0.9</td>
<td>0.3– 0.45</td>
<td>0.4– 0.95</td>
<td>0.4– 1.1</td>
</tr>
<tr>
<td>Max $I_{\text{LOAD}}$ (mA)</td>
<td>4.6</td>
<td>200</td>
<td>2</td>
<td>3.36</td>
<td>100</td>
</tr>
<tr>
<td>$I_Q$ (mA)</td>
<td>0.024– 0.22</td>
<td>0.11</td>
<td>0.014</td>
<td>0.08– 0.26</td>
<td>0.1– 1.07</td>
</tr>
<tr>
<td>$C_{\text{LOAD}}$ (nF)</td>
<td>1</td>
<td>23.5</td>
<td>0.4 (Integrated)</td>
<td>0.1 (Integrated)</td>
<td>0.04 (Integrated)</td>
</tr>
<tr>
<td>Max current efficiency (%)</td>
<td>98.3</td>
<td>99.94</td>
<td>99.8</td>
<td>99.2</td>
<td>99.5</td>
</tr>
<tr>
<td>$\Delta V,T_s @\Delta I_{\text{LOAD}}$</td>
<td>90mV,1.1µ<a href="mailto:s@1.4mA">s@1.4mA</a></td>
<td>120mV,40µs@180mA</td>
<td>40mV,0.1µ<a href="mailto:s@1.06mA">s@1.06mA</a></td>
<td>34mV,1.2µ<a href="mailto:s@1.44mA">s@1.44mA</a></td>
<td>108mV,1.24µs@50mA</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>0.355</td>
<td>0.021</td>
<td>0.0023*</td>
<td>0.03*</td>
<td>0.0374</td>
</tr>
<tr>
<td>FOM (ps)**</td>
<td>10100</td>
<td>9.57</td>
<td>199</td>
<td>20</td>
<td>1.38</td>
</tr>
</tbody>
</table>

*# From oscilloscope waveform **Without $C_{\text{LOAD}}$ *\text{FOM}=C_{\text{LOAD}}\Delta V*I_Q/((\Delta I_{\text{LOAD}})^2. Smaller FOMs are better
Conclusion

- A fully integrated digital LDO using VCO based time quantization
- Adaptive sampling clock utilizing beat-frequency
- Built-in active voltage positioning
- Measured max current efficiency is 99.5% with FOM of 1.38ps in 65nm CMOS