18.5 A Fully Integrated 40pF Output Capacitor Beat-Frequency-Quantizer-Based Digital LDO with Built-In Adaptive Sampling and Active Voltage Positioning

Somnath Kundu[1], Muqing Liu[1], Richard Wong[2], Shi-Jie Wen[2], Chris H. Kim[1]

[1]University of Minnesota, Minneapolis, MN
[2]Cisco Systems, San Jose, CA

Integrated voltage regulators with a wide output current/voltage dynamic range are required to support fast dynamic voltage and frequency scaling (DVFS). Low Dropout Regulators (LDOs) based on digital-intensive circuits have been gaining popularity [1]–[4] due to their compactness, process scalability, high immunity to process-voltage-temperature (PVT) variations and easy programmability for design optimization. Conventional digital LDOs utilizing a comparator and shift-registers [1] suffer from a slow response time during a large/fast change in load current (I_{LOAD}). Higher sampling frequency (f_S) improves the response time, but at the cost of increased power consumption and reduced loop stability. Multi-bit quantizers utilizing ADCs [2-4] can reduce the settling time, however, the presence of a high resolution ADC and the control logic increases the design complexity. Moreover, the ADC resolution limits the maximum f_S. In order to overcome the trade-off between speed and power, adaptive sampling techniques were incorporated in [1], [4]. But the overhead of multiple VCOs operating simultaneously and a separate overshoot/droop detection circuitry [1], or an event-driven controller with 7b ADC [4], increase the complexity and power consumption. Furthermore, none of the previous designs incorporated active voltage positioning (AVP), a popular ripple-suppression technique, whereby the LDO output is set slightly above (in low-activity state) or below (in high-activity state) the reference voltage depending on the processor workload conditions [5].

In this work, a beat-frequency quantizer-based digital LDO (BF-LDO) is described, where a pair of ring VCOs and simple digital blocks are used to generate an adaptive-sampling clock. It has several critical benefits: 1) Time quantization utilizing the VCO and counter provides a highly digital and tunable ADC design solution. The VCO phase quantization provides 1st-order noise shaping achieving high resolution. 2) Dynamically adaptive f_S proportional to the output voltage error reduces droop/overshoot and settling time by increasing f_S during transient ripples. Low f_S near steady state improves the quantizer resolution, LDO power efficiency and stability margin. 3) Inherent AVP reduces the transient ripple further by dynamically controlling the steady-state voltage. 4) The design is very robust to PVT variations, as the quantizer output is a function of the ratio of two VCO frequencies, cancelling frequency variations due to common-mode effects.

Figure 18.5.1 shows the basic operation of a time-based digital LDO. The VCO pair converts the reference and the output voltages (V_{REF}, V_{LDO_OUT}) to clock pulses (CK_{REF}, CK_{OUT}) of proportional frequency (f_{REF}, f_{OUT}). The time quantizer calculates the frequency difference, $f_{REF} - f_{OUT}$ to generate a digital code N_{OUT}. By comparing N_{OUT} with a predefined N, the digital controller adjusts the number of PMOS switches to keep V_{LDO_OUT} constant for a given I_{LOAD} range. A time quantizer is conventionally implemented by counting CK_{OUT} edges in a fixed sampling period (CK_s), which is generated by dividing CK_{REF} by a factor N. A higher N improves the quantizer resolution and the loop stability margin, but at the cost of slow response time and large transient ripple. To overcome this limitation, an adaptive sampling technique is proposed that utilizes a D-flip-flop (DFF) as a digital frequency subtractor, also known as a BF quantizer [6]. Using the beat frequency for loop sampling makes f_S proportional to $|V_{REF}–V_{LDO\_OUT}|$. During I_{LOAD} transients, V_{LDO_OUT} experiences a large ripple, increasing f_S for faster recovery. On the other hand, near steady state, f_S reduces as $|V_{REF}–V_{LDO\_OUT}|$ is very small. This improves the quantizer resolution to set V_{LDO_OUT} very precisely, and at the same time reduces the switching power dissipation with excellent loop stability. The counter counts the CK_{REF} edges in a sampling period generating $N_{OUT}=f_{REF}/|f_{REF}-f_{OUT}|$. Once steady state is reached, $N_{OUT}=N$ makes $f_S=f_{REF}/N$, causing a fixed offset at V_{LDO_OUT}. This inherent offset enables AVP, which is addressed later. In addition, since the VCOs are operating continuously without phase reset, the quantization noise is 1st-order high-pass filtered, increasing the resolution [6].

The voltage offset, i.e. $|V_{REF}-V_{LDO\_OUT}|$, can also be written as $f_{REF}/K_{VCO}\cdot N_{OUT}$, where K_{VCO} is the VCO voltage-to-frequency conversion gain. It reaches a minimum value of $f_{REF}/K_{VCO}\cdot N$ during steady state. In theory, N can be set to infinity in order to cancel this steady-state offset. However, the maximum value of N is defined by the size of the BF counter, the digital control logic, as well as the number of PMOS switches. In this implementation, for 10b PMOS control, N is nominally set to 64, introducing an offset of 16mV for the VCO pair operating at 250MHz frequency with K_{VCO} of 250MHz/V.

Figure 18.5.2 illustrates the BF-LDO architecture. It comprises the proposed BF quantizer and the conventional linear quantizer as a baseline for performance comparison. SEL_Q selects the desired quantizer. Since the BF quantizer detects the absolute voltage difference between V_{REF} and V_{LDO_OUT}, a simple 1b comparator is introduced for polarity detection to keep the loop in a negative feedback configuration at all times. The BF quantizer operation is explained in the timing diagram. The quantizer output is subtracted from the external code N and the difference goes to a 10b proportional-integral (PI) control to tune 1024 PMOS switches. The PI control parameters, K_F, K_P and K_I are fully programmable. I_{LOAD} is generated from an NMOS array driven by a test VCO that triggers a series of DFFs. The wide programmability in the VCO frequency, as well as in the number of DFFs enable an I_{LOAD} range of 0-400mA and a rise/fall time range of 16ns–9µs with a resolution of 1mA and 1.3ns, respectively.

AVP as illustrated in Fig. 18.5.3 (left), compromises the DC voltage regulation to reduce the transient ripple significantly [5]. In the proposed BF-LDO, a positive step in I_{LOAD} causes a droop in V_{LDO_OUT} and it settles at an offset, $f_{REF}/K_{VCO}N$ below V_{REF}. Similarly, a negative I_{LOAD} step brings V_{LDO_OUT} above V_{REF} with the same offset achieving built-in AVP. Although the offset is negligible for a large N providing good DC regulation, it can be easily increased for ripple reduction by reducing N. Measured waveforms in Fig. 18.5.3 show the ripple reduction from 260mV to 120mV by reducing N from 64 (=weak AVP) to 16 (=strong AVP). The PMOS switch array and the VCO implementations are shown in Fig. 18.5.3 (right). A switch driver with dummy buffers and PMOS branches keep balanced loading for the 10b binary PMOS switches, as shown in the example for 3b. This removes glitches due to rise/fall-time imbalance during code transition. Uniformly distributed layout also reduces any mismatch among PMOS branches. The VCOs have both coarse and fine frequency tuning to achieve wide frequency range and to compensate any frequency offset between them.

Figure 18.5.4 shows the measured transient response from a 65nm test-chip. I_{LOAD} steps between 20mA and 70mA in 0.8µs cause a 108mV droop and a 148mV overshoot with a settling time of 1.24µs and 1.13µs, respectively. The steady state f_S is 3.9MHz, but it increases to a much higher value during I_{LOAD} transition. The baseline LDO with a fixed 3.9MHz f_S experiences a 564mV (i.e. 5×) droop (ΔV) and a 30.8µs (i.e. 25×) settling time (Ts). The BF-LDO also achieves a fast response in V_{REF} step (Fig. 18.5.4, bottom right), which is critical for fast DVFS systems. Fig. 18.5.5 (top) compares ΔV and Ts of the proposed BF-LDO with the baseline for different rise-time, ΔT and load step, ΔI_{LOAD} showing a significant benefit of adaptive sampling. The line and load regulation are shown in Fig. 18.5.5 bottom verifying the BF-LDO functionality over wide operating conditions. The current efficiency plot in Fig. 18.5.6 shows >93% efficiency over 10× variation in I_{LOAD} with a peak value of 99.5%. Utilizing the frequency ratio of the two VCOs makes the quantizer insensitive to supply variation as evident from the measured low frequency PSRR of -38dB. The comparison table in Fig. 18.5.6 shows comparable ΔV and Ts with much lower C_{LOAD} achieving the best FOM. The active area is 0.0374mm^2 including C_{LOAD}, as shown in Fig. 18.5.7.

References:

[1] B. Nasir, et al., "0.13µm Fully Digital Low-Dropout Regulator with Adaptive Control and Reduced Dynamic Stability for Ultra-Wide Dynamic Range," *ISSCC*, pp. 98-99, 2015.
[2] Y. J. Lee, et al., "A 200mA Digital Low-Drop-Out Regulator with Coarse-Fine Dual Loop in Mobile Application Processors," *ISSCC*, pp. 148-149, 2016.
[3] L. G. Salem, et al., "A 100nA-to-2mA Successive-Approximation Digital LDO with PD Compensation and Sub-LSB Duty Control Achieving a 15.1ns Response Time at 0.5V," *ISSCC*, pp. 340-341, 2017.
[4] D. Kim, et al., "A 0.5V-VIN 1.44mA-Class Event-Driven Digital LDO with a Fully Integrated 100pF Output Capacitor," *ISSCC*, pp. 148-149, 2017.
[5] A. Paul, et al., "System-Level Power Analysis of a Multicore Multipower Domain Processor with ON-Chip Voltage Regulators," *IEEE TVLSI,* vol. 24, no. 12, pp. 1-4, 2016.
[6] S. Kundu, et al., "Two-step Beat Frequency Quantizer Based ADC with Adaptive Reference Control for Low Swing Bio-potential Signals," *CICC*, pp. 1-4, 2015.

 978-1-5090-4940-0/18/$31.00

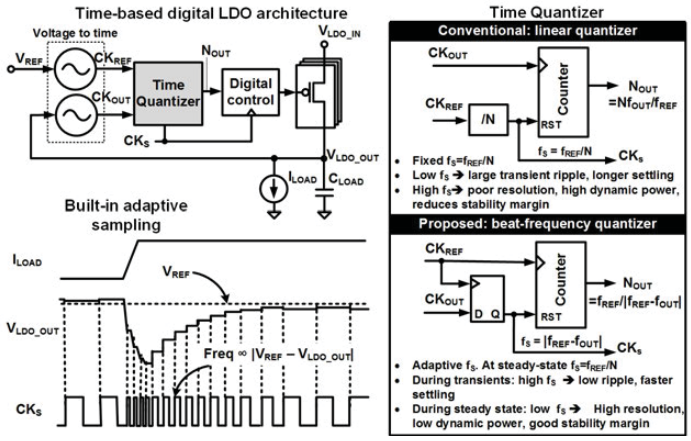


Figure 18.5.1: (Upper left) Basic operation of a time-based digital LDO. (Lower left) Adaptive sampling utilizing beat-frequency. (Right) Linear and beat-frequency time quantizer circuits.

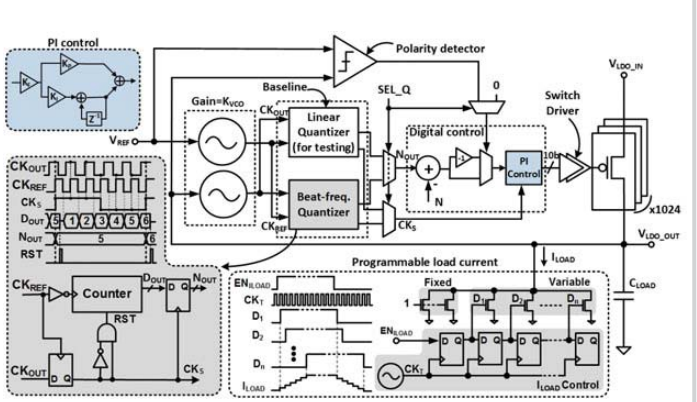


Figure 18.5.2: Implementation of beat-frequency quantizer-based digital LDO. The conventional linear quantizer was also implemented for performance comparison.

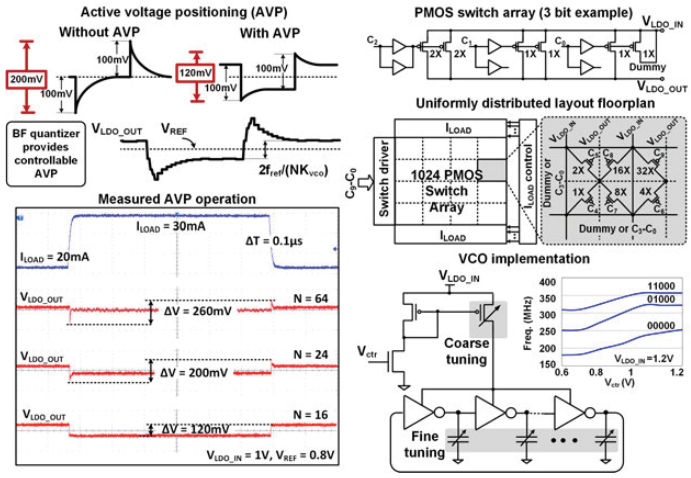


Figure 18.5.3: (Left) BF quantizer-based digital LDO provides inherent AVP. (Upper right) Implementation of the PMOS switch array. (Lower right) Implementation of the VCO.

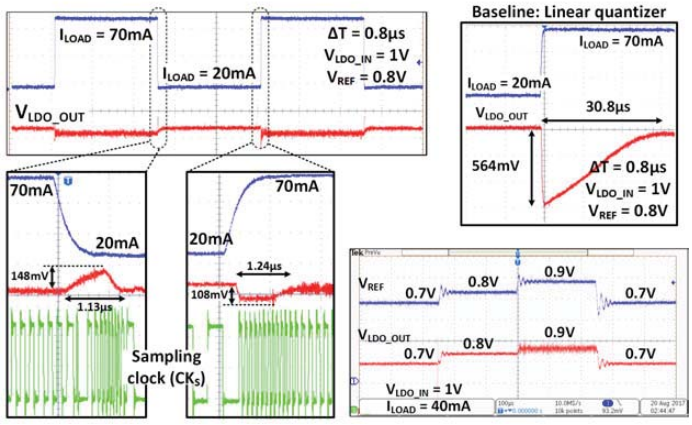


Figure 18.5.4: Measured transient response of the BF-LDO. The built-in adaptive sampling in BF-LDO provides 25× faster settling and 5× lower droop compared to the baseline.

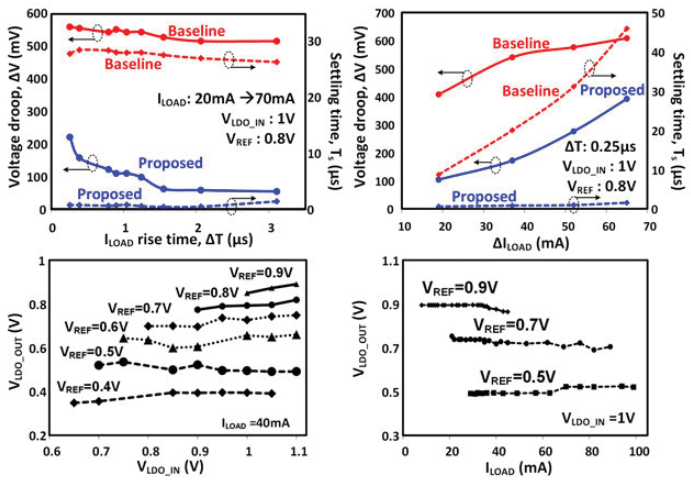
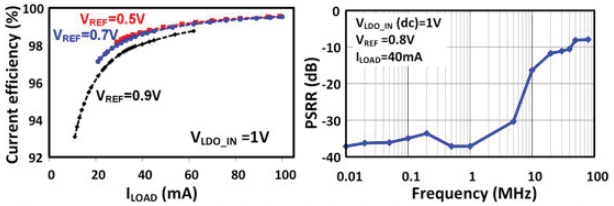


Figure 18.5.5: (Top) Measured voltage droop and settling time for different I_{LOAD} rise time and ΔI_{LOAD}. (Bottom) Measured line and load regulation for different V_{REF}.

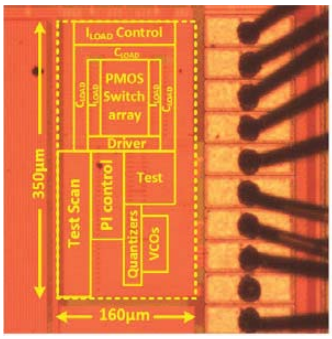


	[1] Nasir, ISSCC'15	[2] Lee, ISSCC'16	[3] Salem, ISSCC'17	[4] Kim, ISSCC'17	This Work
Process	130nm	28nm	65nm	65nm	65nm
Architecture	Shift Reg	Shift Reg+ADC	SAR ADC	Event-driven ADC	VCO based ADC
Adaptive sampling/ AVP	Yes / No	No / No	No / No	Yes / No	Yes / Yes
V_{LDO_IN} (V)	0.5 – 1.2	1.1	0.5 – 1	0.45 – 1	0.6 – 1.2
V_{LDO_OUT} (V)	0.45 – 1.14	0.9	0.3 – 0.45	0.4 – 0.95	0.4 – 1.1
Max ΔI_{LOAD} (mA)	4.6	200	2	3.36	100
I_Q (mA)	0.024 – 0.22	0.11	0.014	0.08 – 0.26	0.1 – 1.07
C_{LOAD} (nF)	1	23.5	0.4 (Integrated)	0.1 (Integrated)	0.04 (Integrated)
Max current efficiency (%)	98.3	99.94	99.8	99.2	99.5
ΔV, Ts @ ΔI_{LOAD}	90mV,1.1µs @ 1.4mA	120mV,40µs# @180mA	40mV,0.1µs @1.06mA	34mV,11.2µs @1.44mA	108mV,1.24µs @50mA
Area (mm²)	0.355	0.021	0.0023*	0.03*	0.0374
FOM (ps)**	10100	9.57	199	20	1.38

From oscilloscope waveform *Without C_{LOAD} **FOM=$C_{LOAD}\Delta V*I_Q/(\Delta I_{LOAD})^2$. Smaller FOMs are better

Figure 18.5.6: (Top) Measured current efficiency and PSRR. (Bottom) performance comparison with state-of-the-art digital LDOs.

18



	Proposed	Baseline
Process	65nm CMOS	
AVP	Yes	No
Steady-state f_s	3.9MHz @ V_{LDO_IN}=1V, V_{REF}=0.9V	
I_{LOAD}	8-100mA	
I_Q	0.8mA @ V_{LDO_IN}=1V,V_{REF}=0.9V (VCOs: 0.6mA (sim.), Switching: 0.2mA)	
C_{LOAD}	40pF	
ΔV, Ts @ ΔI_{LOAD}=50mA	108mV, 1.24µs	564mV, 30.8µs
Area (mm^2)	Core: 0.0374 (VCOs, quantizer, dig:0.015, Switch:0.008, C_{LOAD}:0.01) Test circuits: 0.0186 Total: 0.056	
FOM	1.38ps	7.21ps

Figure 18.5.7: Chip microphotograph and results summary.

978-1-5090-4940-0/18/$31.00