All-Digital PLL Frequency and Phase Noise Degradation Measurements Using Simple On-Chip Monitoring Circuits

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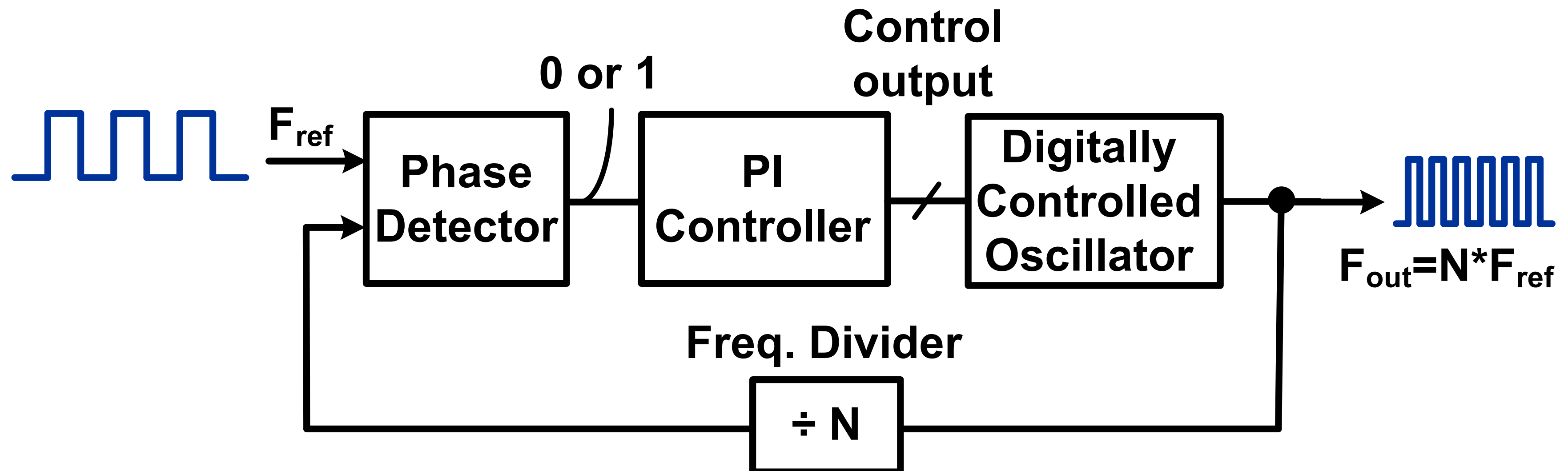
Purpose

- **Experimental study of all-digital PLL (ADPLL) reliability issues**
- **ADPLL frequency and phase window measurements using on-chip monitors**

Outline

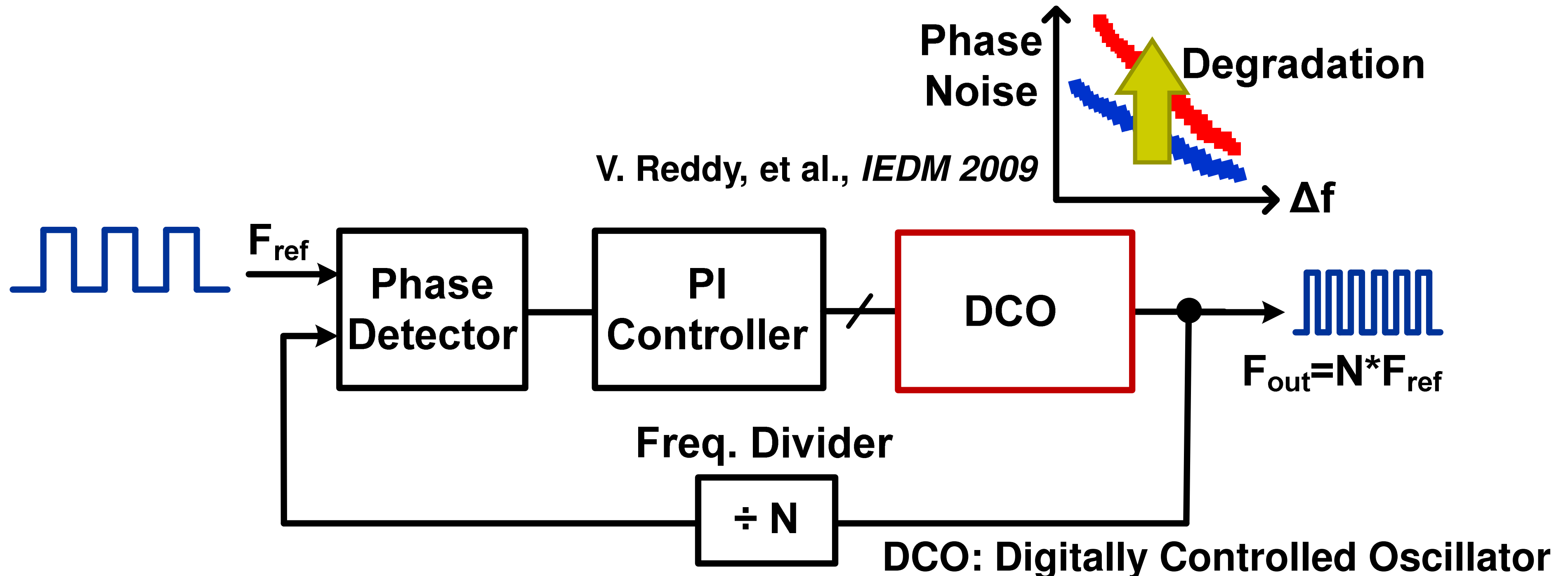
- Motivation
- Proposed on-chip monitors
- 65nm ADPLL chip test setup
- Stress, recovery, annealing results
- Conclusions

Target Circuit: All-Digital Phase Locked Loop (ADPLL)



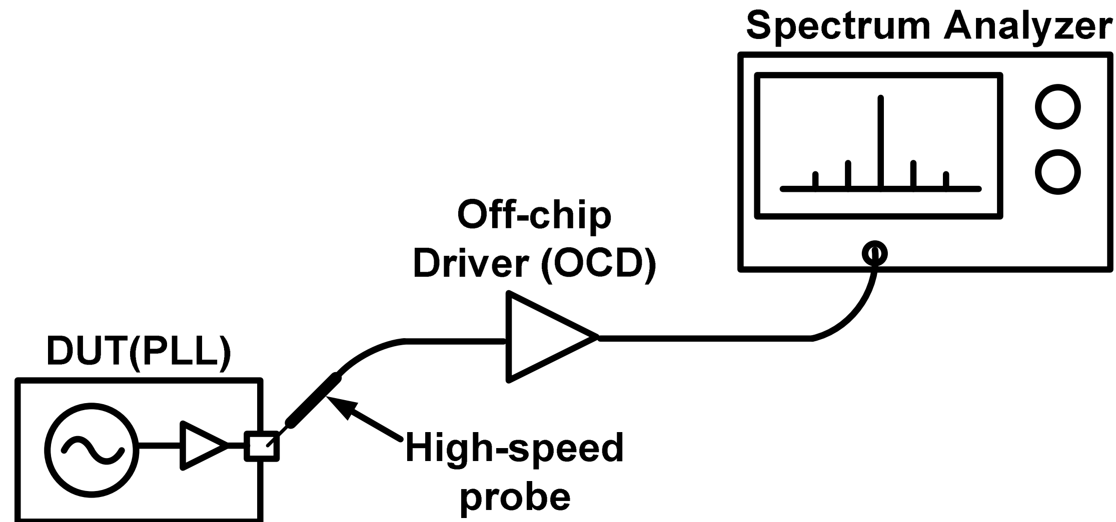
- Key building block for processor clock generation and wireless communication
- No prior work on ADPLL reliability behavior

ADPLL Reliability Figure-of-Merit



- **Frequency: open-loop and closed-loop**
- **Phase noise, jitter degradation**

Drawback of Conventional Off-chip Measurement



- Requires high speed probes or packages, off-chip drivers and connectors
- Each of these components introduces inaccuracy in the measurement

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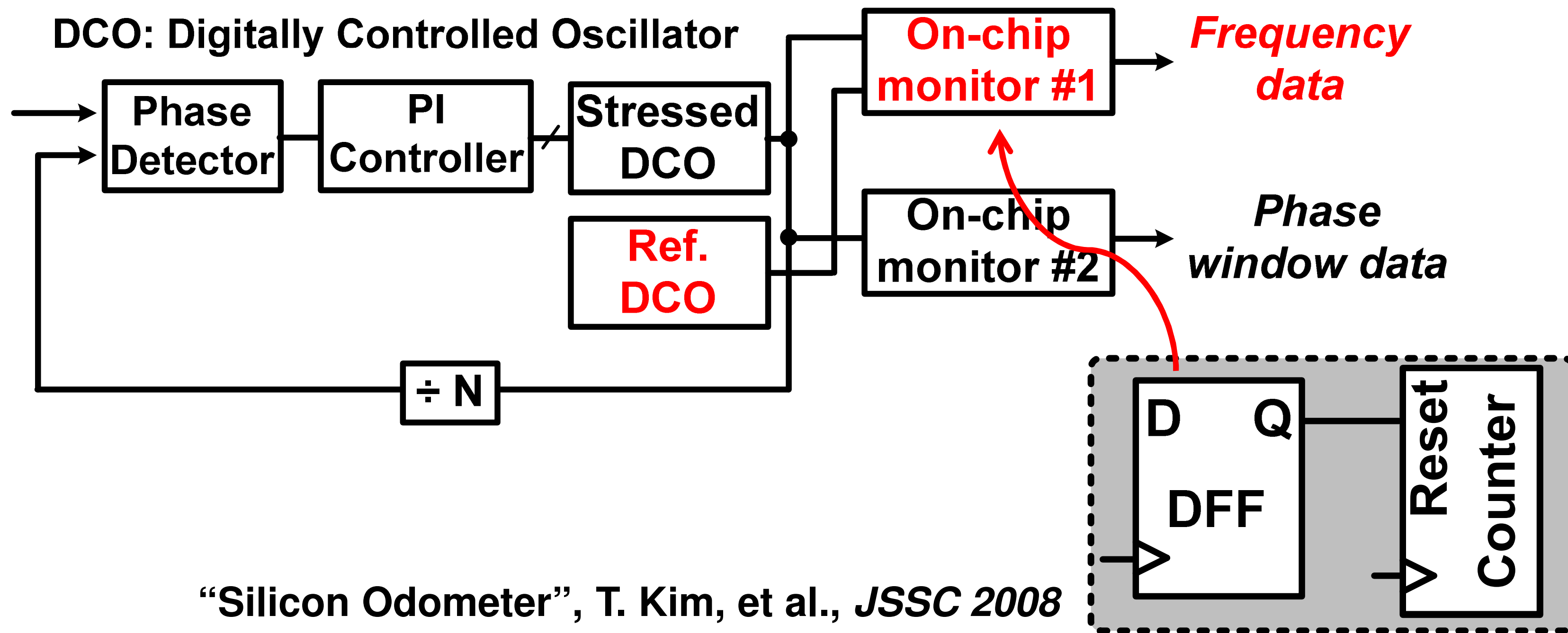
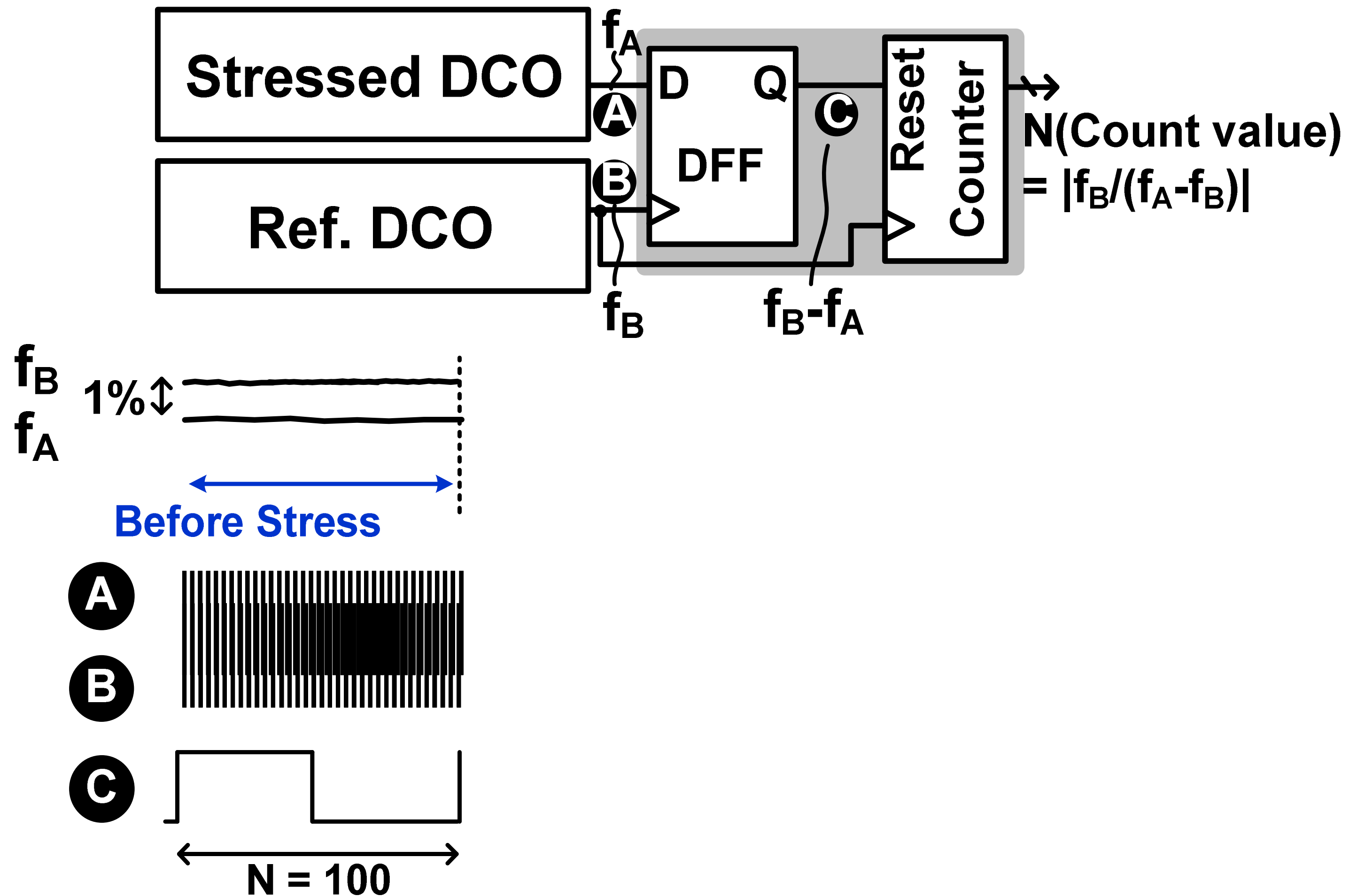
Beat Frequency Monitor

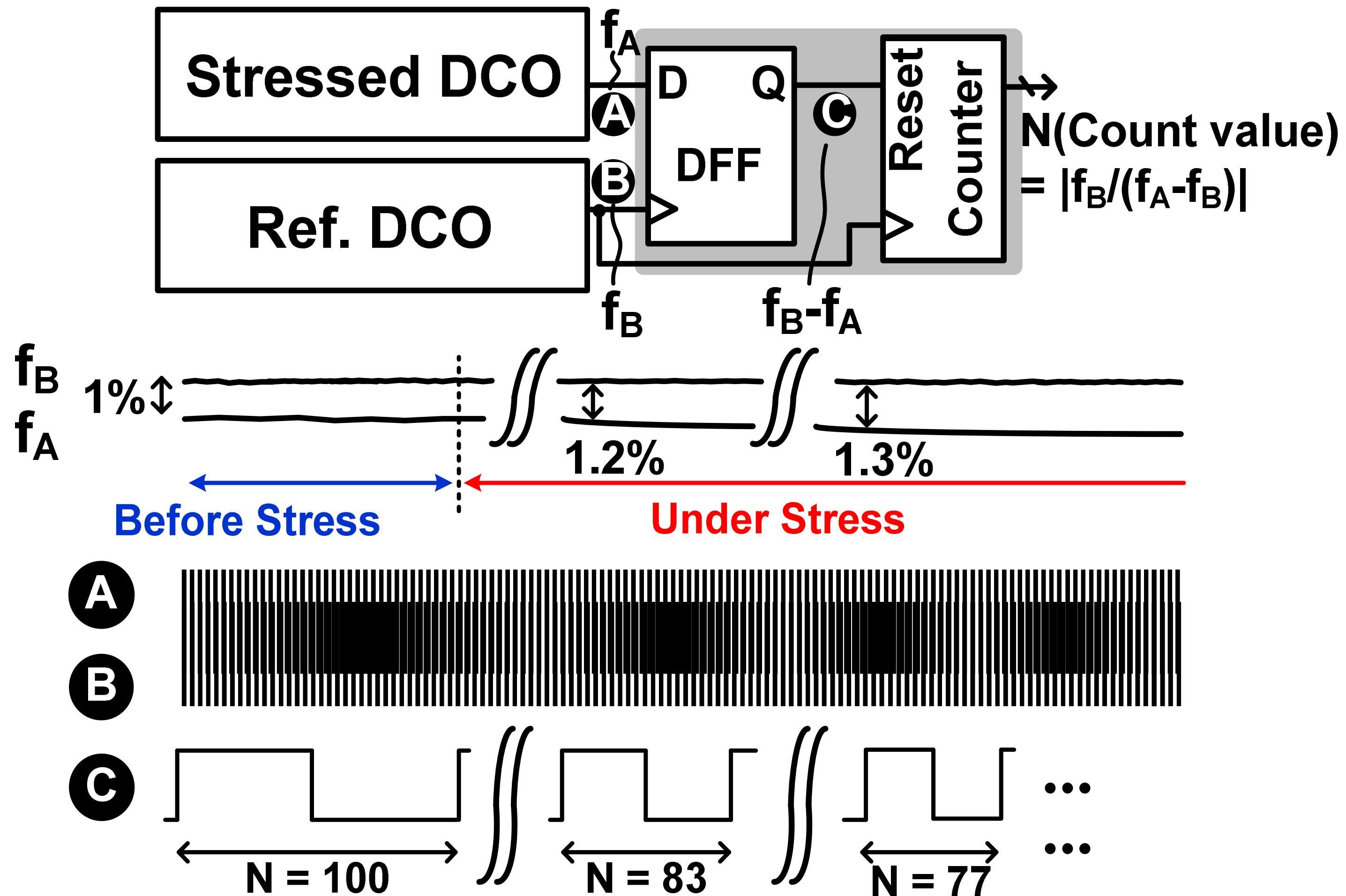


- "Silicon odometer" beat frequency detection circuit adopted for frequency measurements
- Higher precision (~ps) and shorter measurement time (~μs) compared to simple counter based scheme

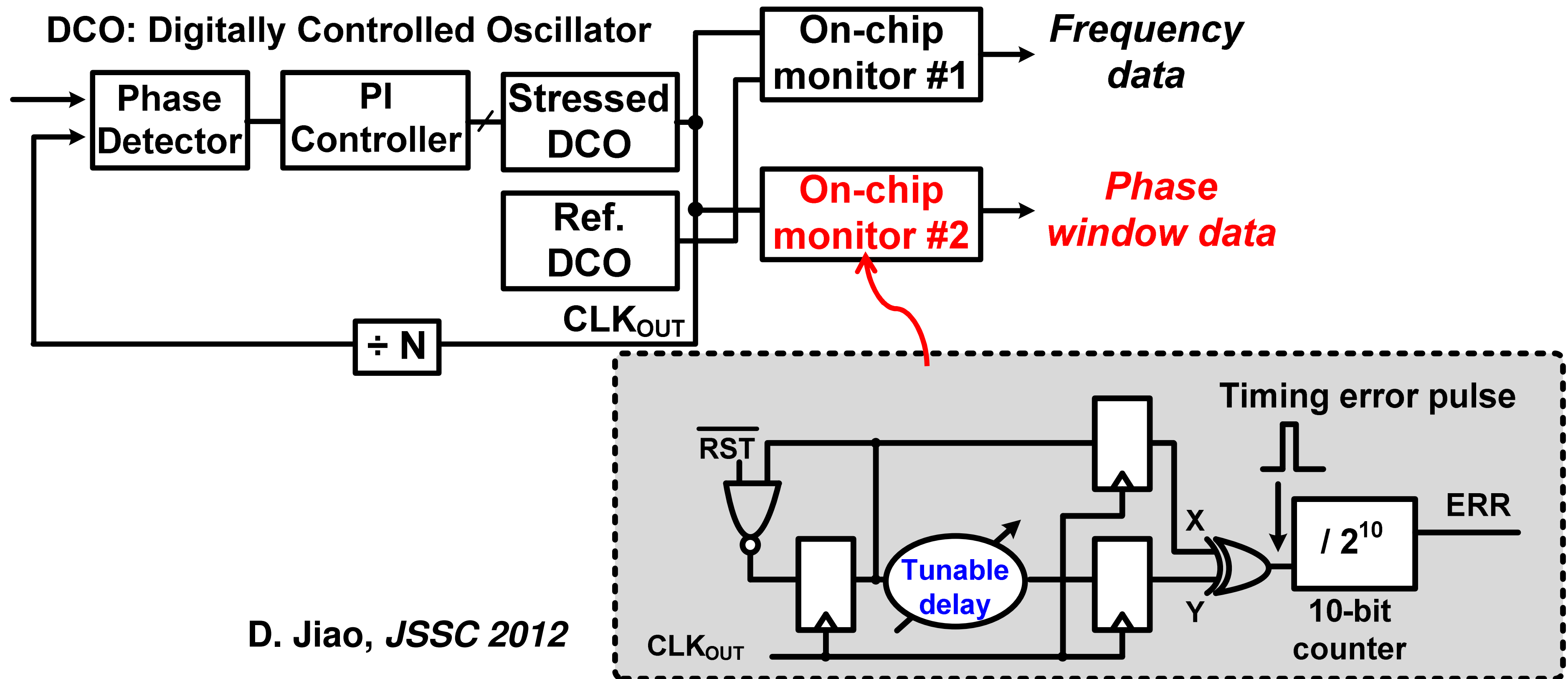
Beat Frequency Monitor Before Stress



Beat Frequency Monitor Under Stress

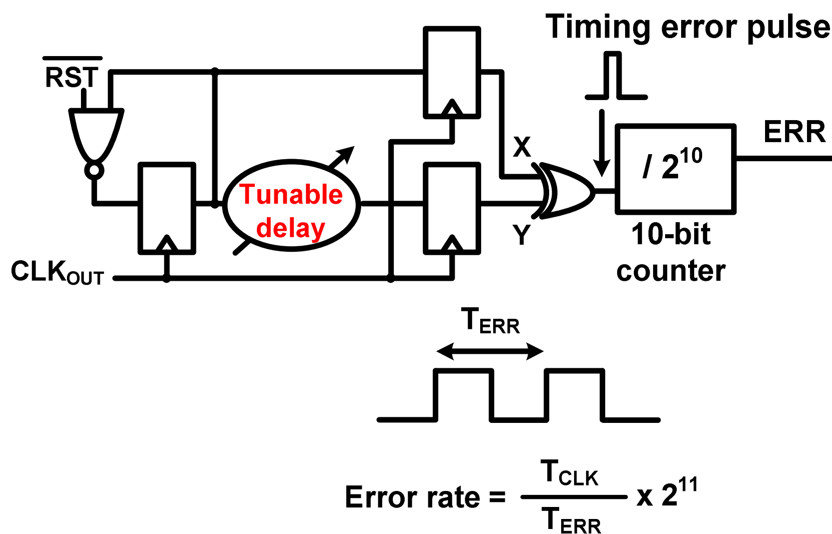


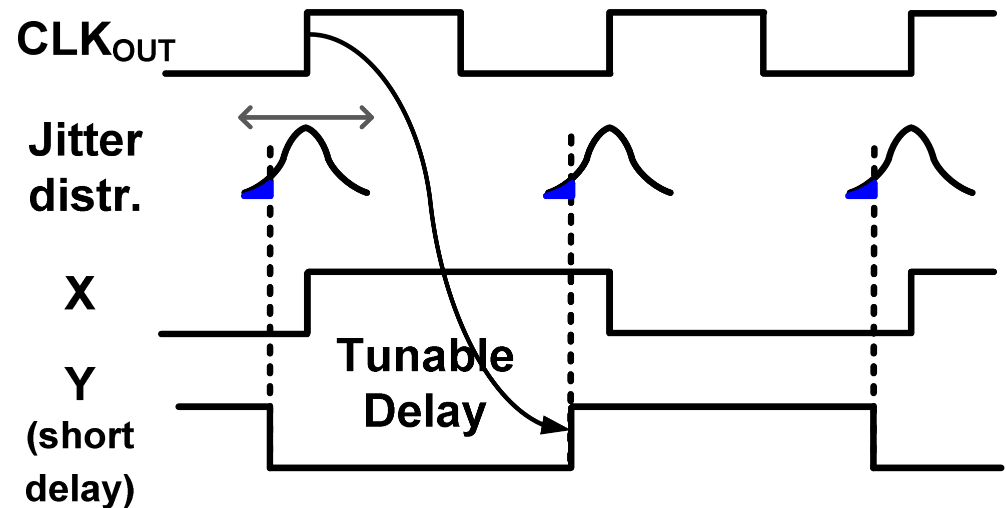
Phase Window Monitor



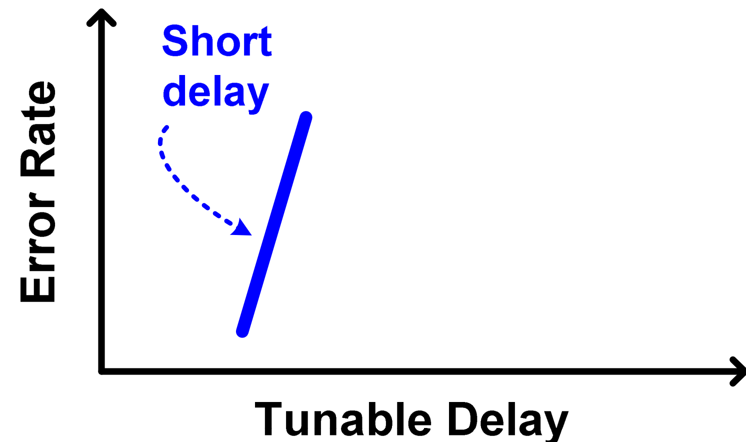
- Clock period (including jitter) compared with tunable delay
- Indirectly measure phase noise by sweeping tunable delay

Phase Window Measurement

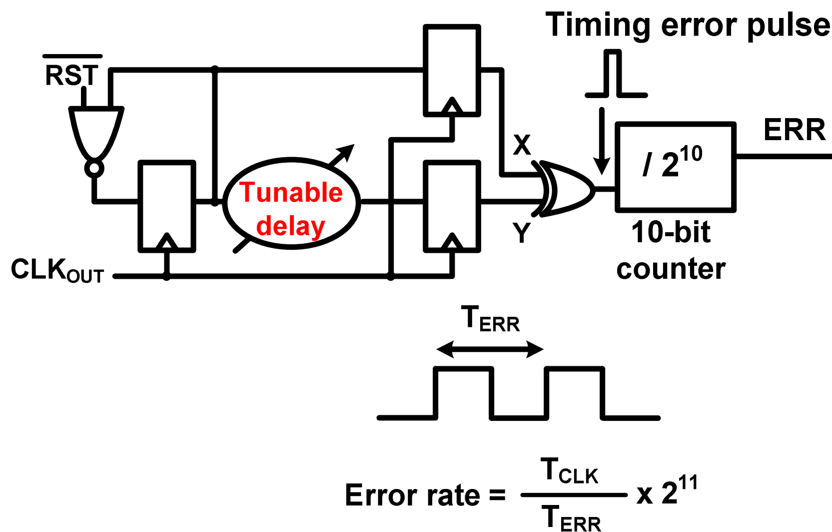




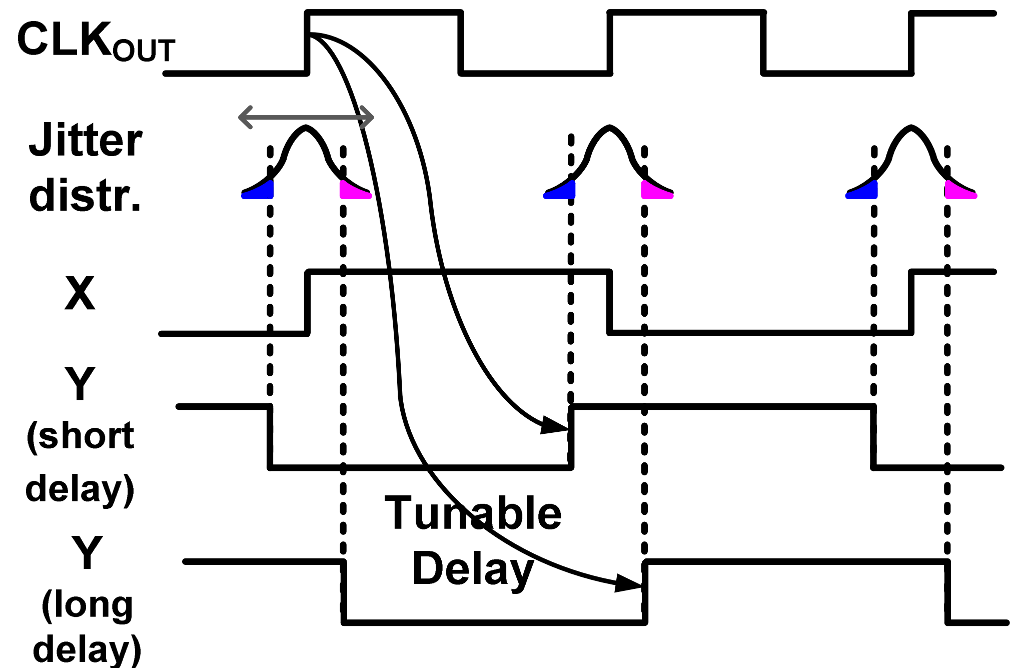
- As tunable delay approaches the clock period, error rate increases

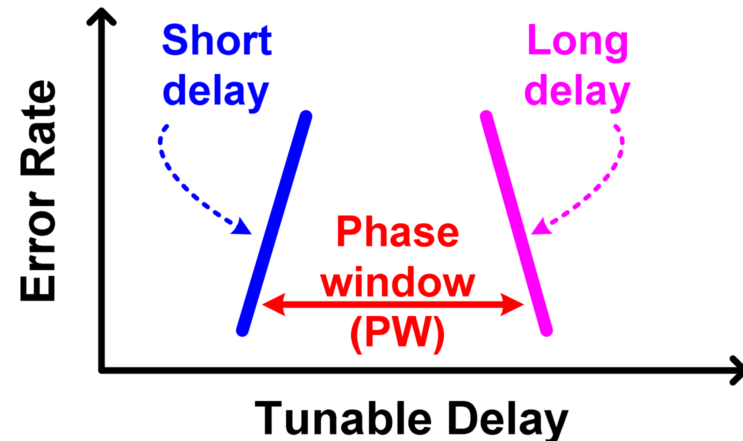


Phase Window Measurement



- As tunable delay increases beyond the clock period, error rate decreases
- Phase window in right figure = a measure of phase noise





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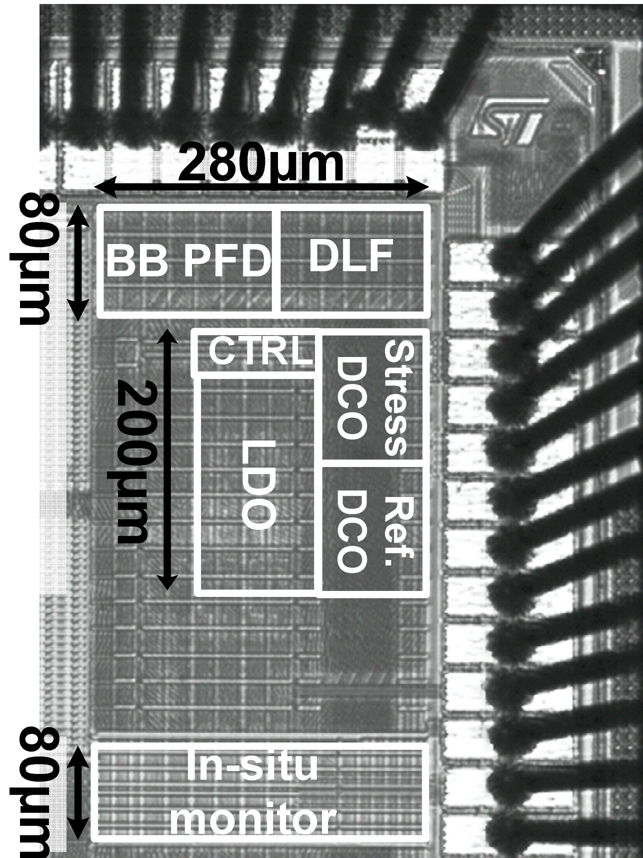
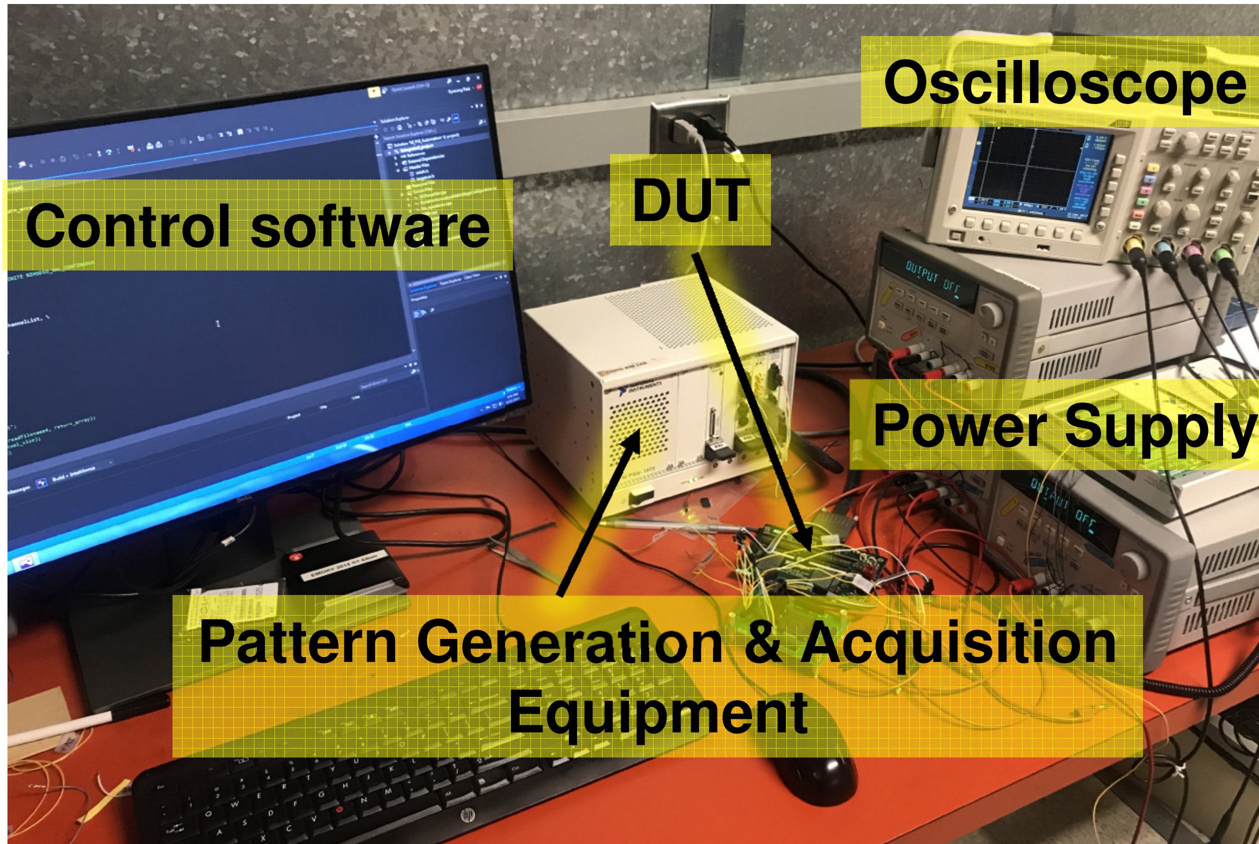
Die Photo and Chip Description



Process	65nm CMOS
System	All-Digital PLL
Nominal supply	1.2V
Stress supply	2.4V
Annealing temp.	110°C, 240°C
DCO frequency (free running)	720MHz @1.2V 1.54GHz @2.4V
Circuit area	0.08mm^2

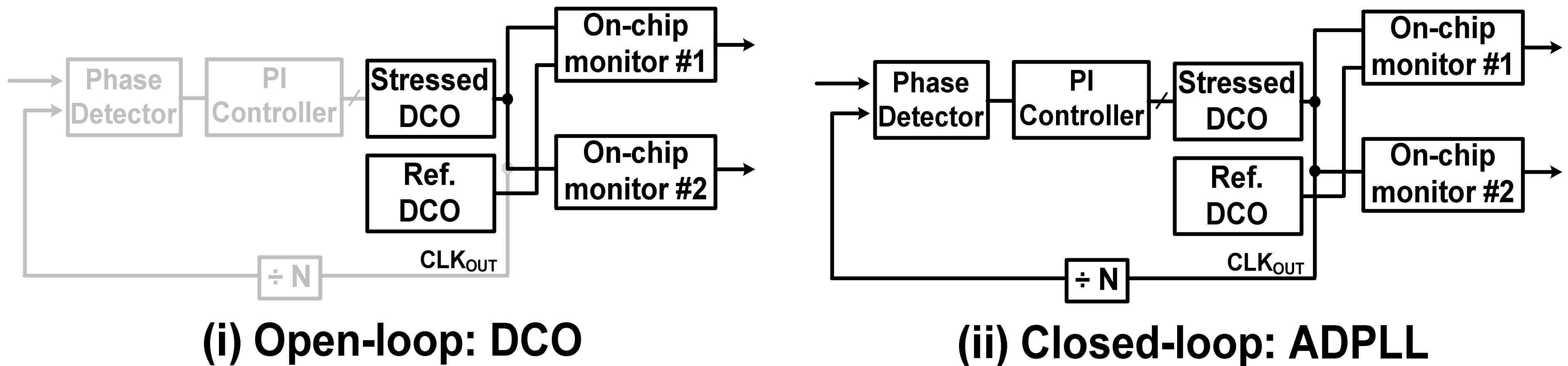
Measurement Setup



Hot Plate

No power
@ 110°C, 240°C

Open-loop and Closed-loop Configurations



(i) Open-loop: DCO

(ii) Closed-loop: ADPLL

- Stress mode: Stress supply (2.4V) for stressed DCO, 0V for reference DCO
- Measurement mode: Nominal supply (1.2V) for both stressed and reference DCOs

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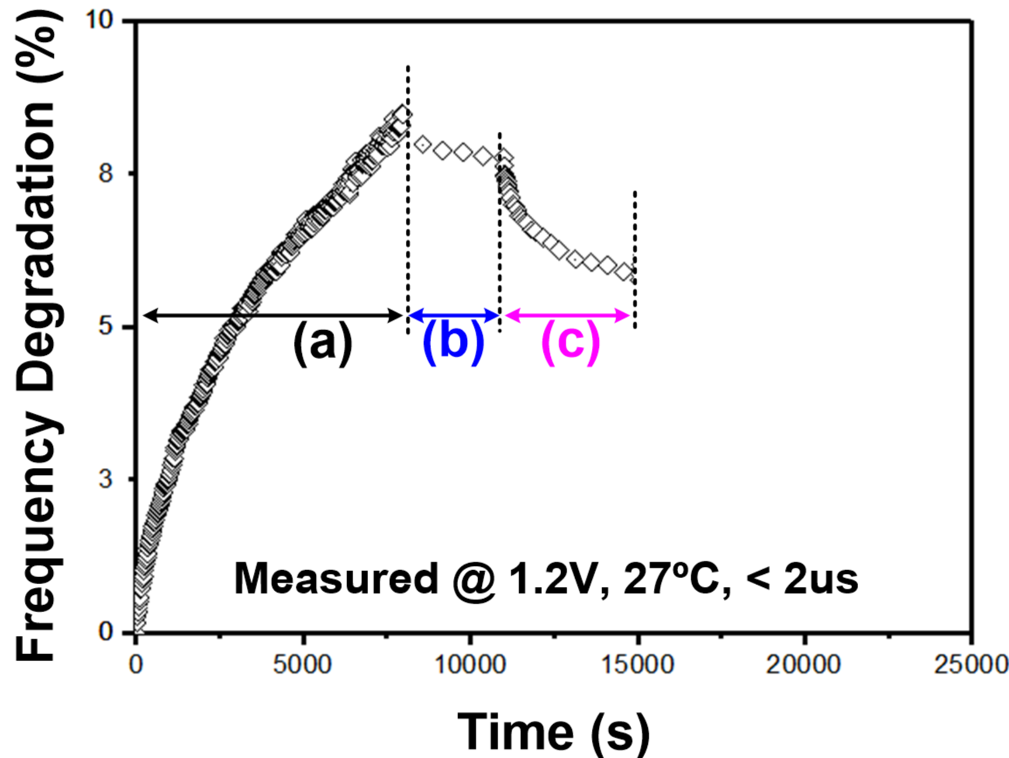
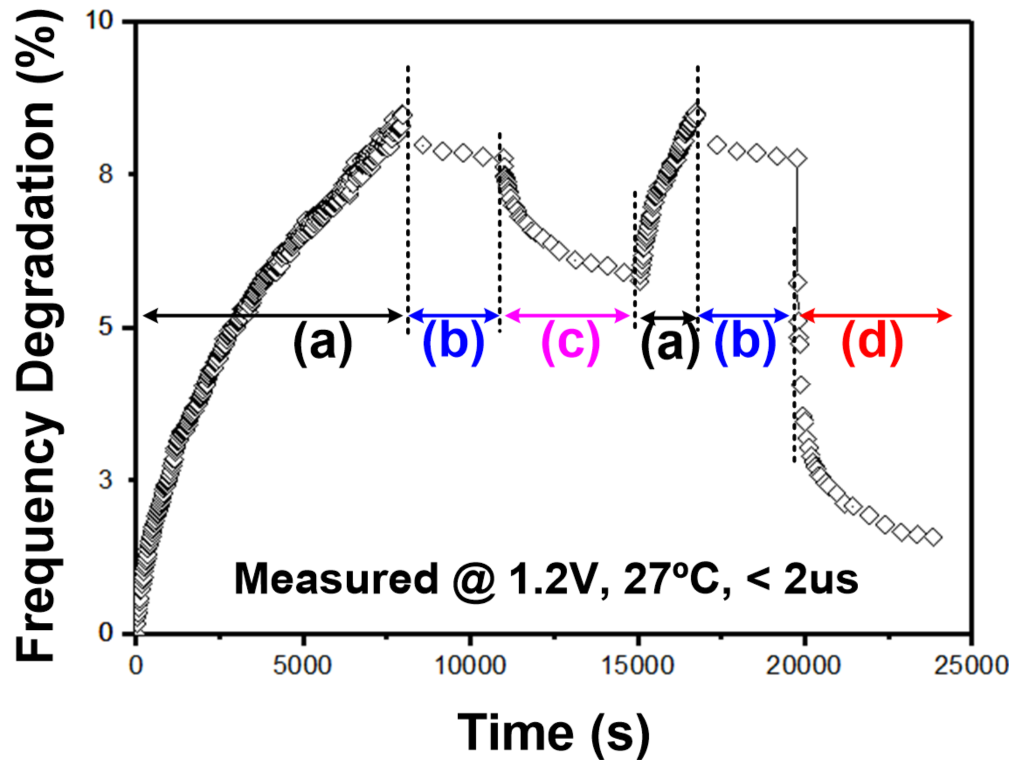
Open-Loop Results: Frequency



(a) Stressed @ 27°C, 2.4V, 1.54GHz
(b) Natural recovery @ 27°C, 0V
(c) Annealing @ 110°C, 0V
(d) Annealing @ 240°C, 0V

- Stress → BTI, HCI → frequency degradation
- Natural recovery and annealing
- Cool down the chip after annealing → remove any residual heat

Open-Loop Results: Frequency



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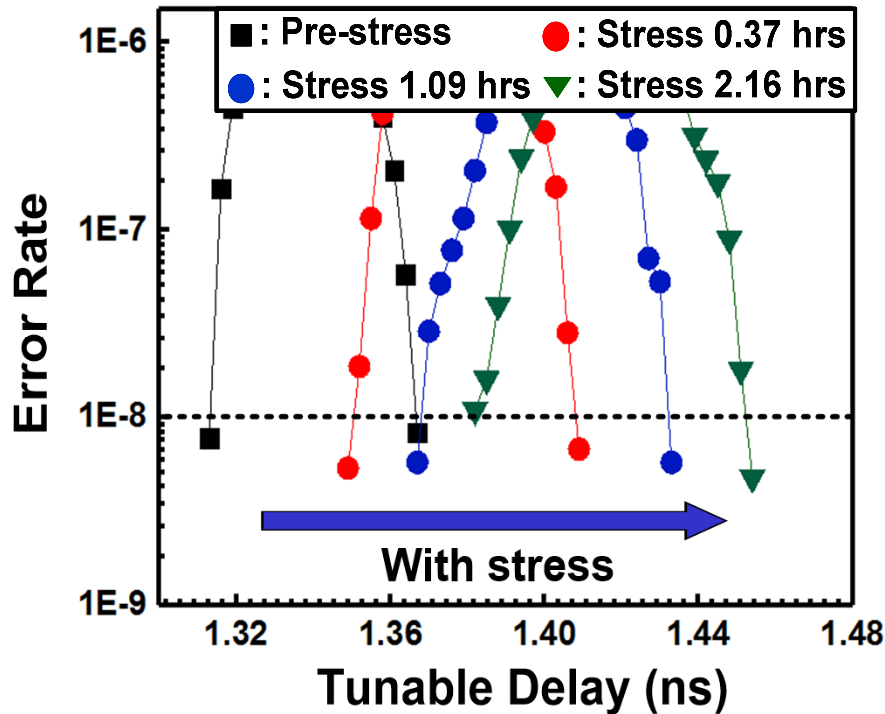
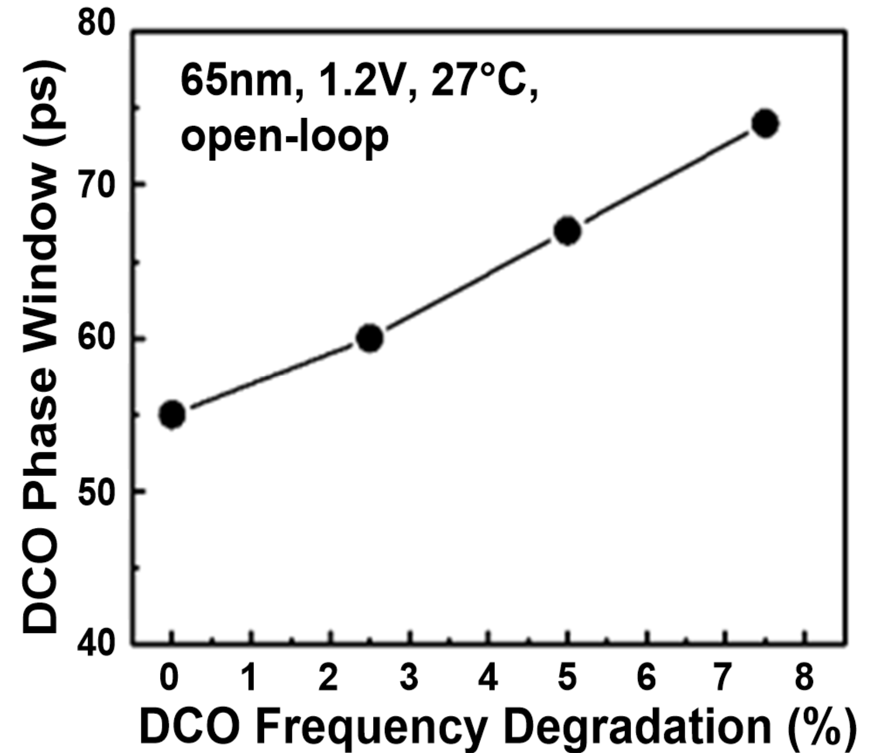
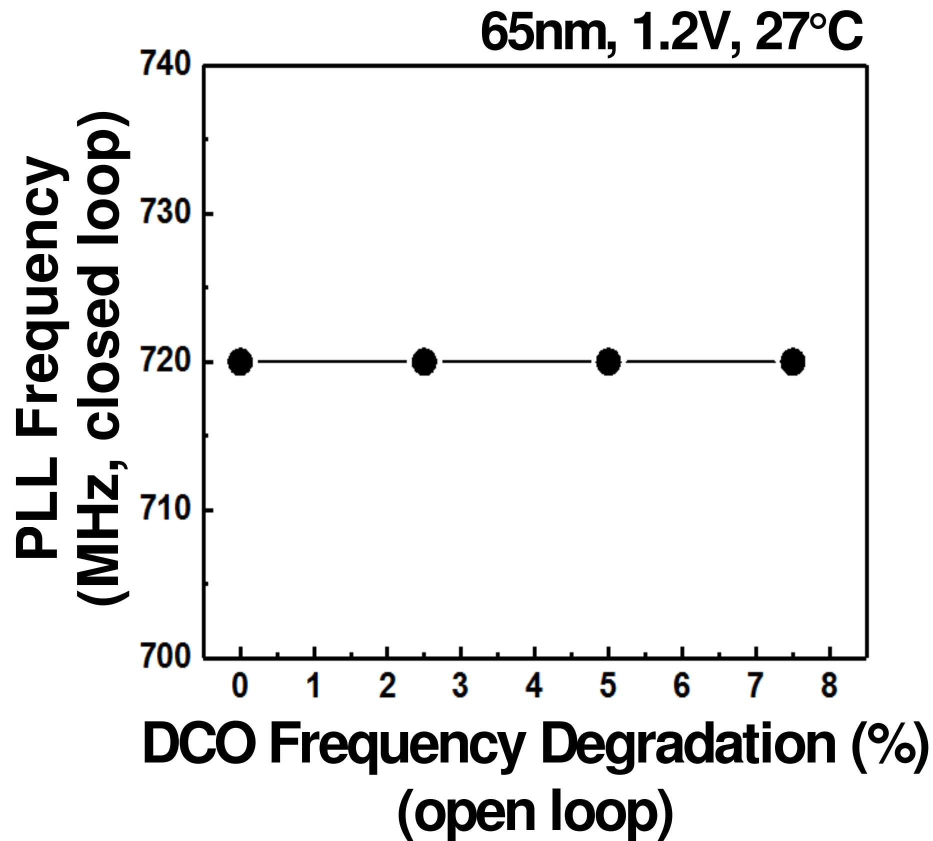
Open-Loop Results: Phase Window





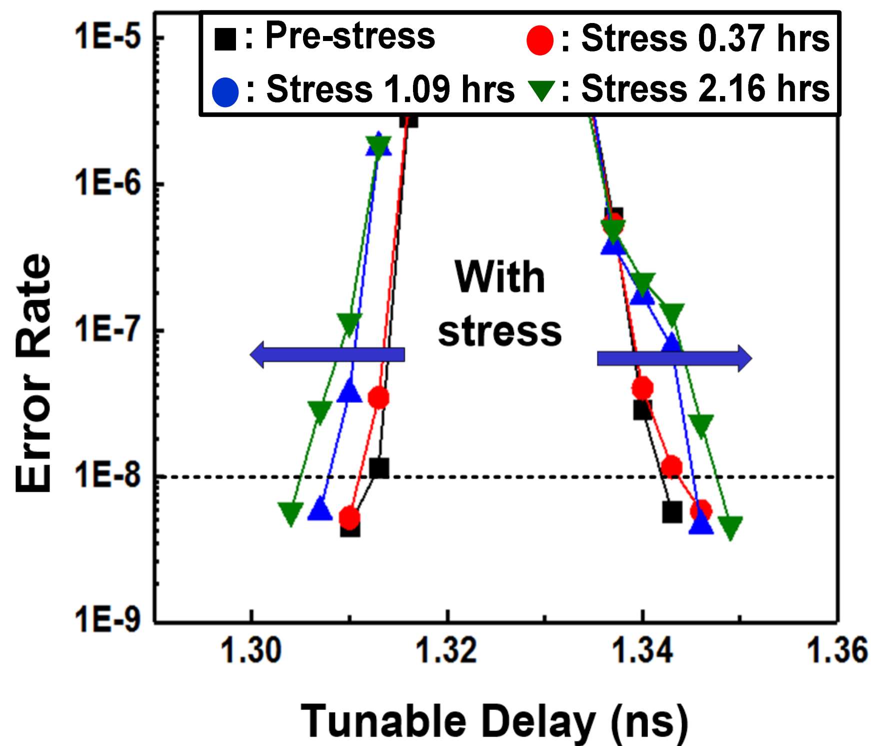
- Phase window @ error rate = 1E-8
- More degradation → larger phase window

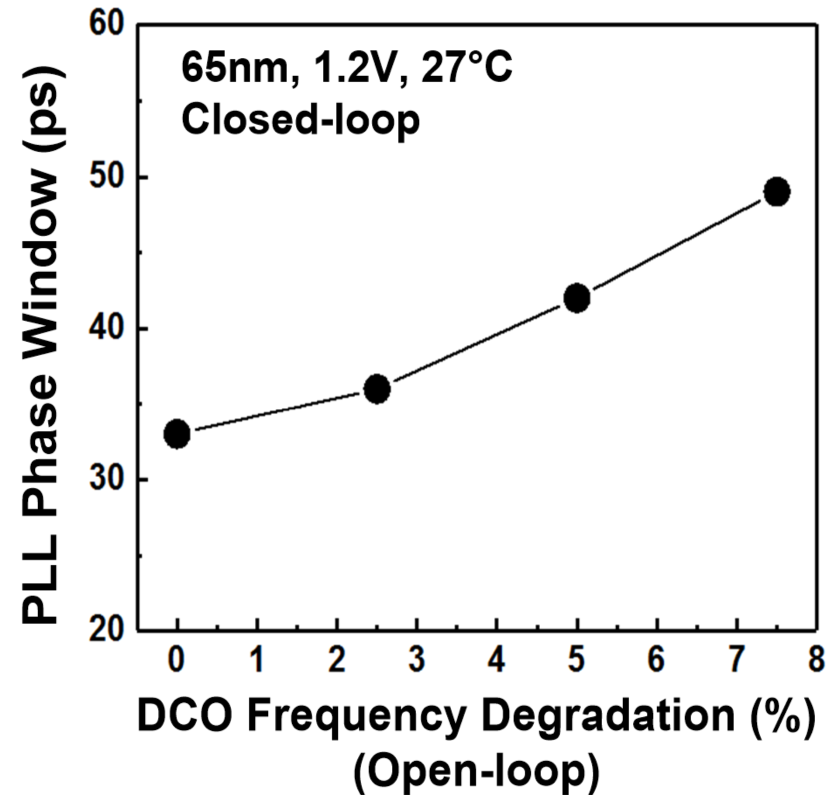
Closed-Loop Results: Frequency



- **Feedback loop ensures that output frequency is constant**

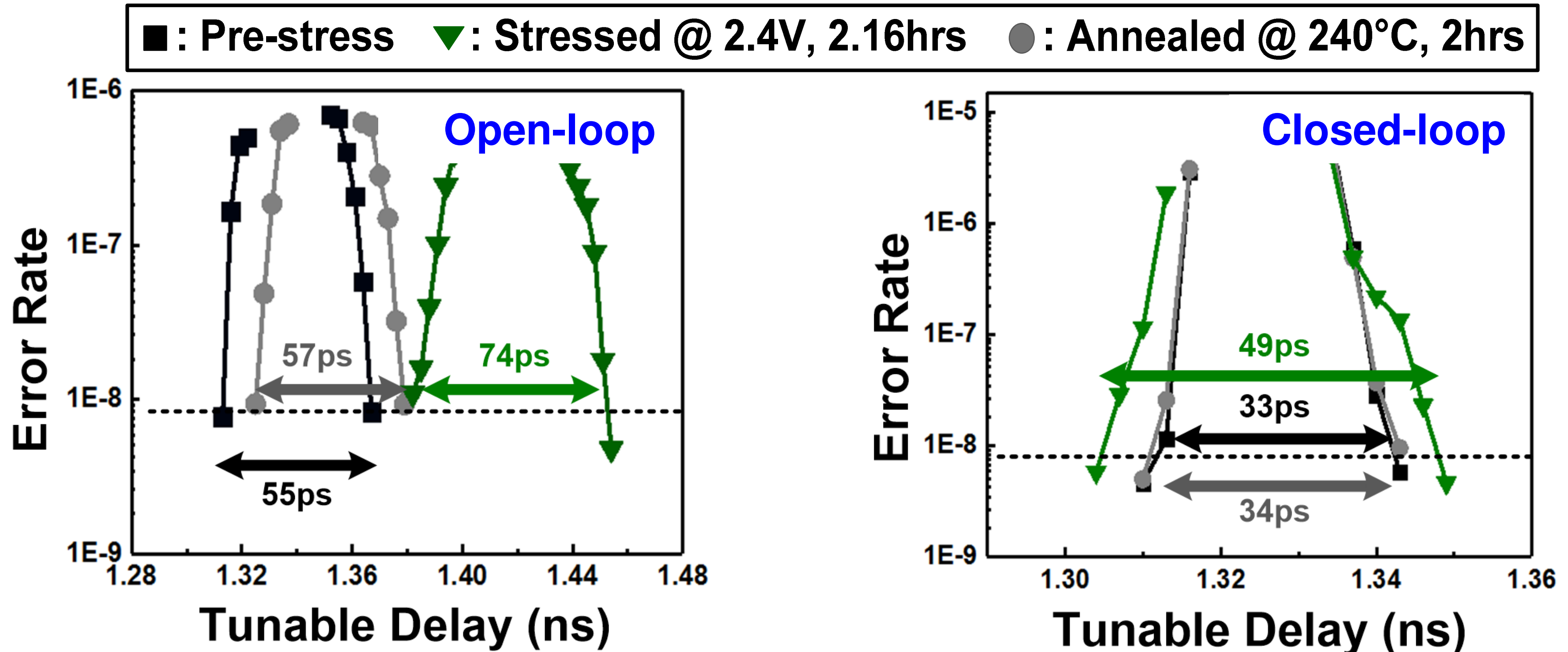
Closed-Loop Results: Phase Window





- Error rate curves all centered around same frequency due to feedback loop
- Longer stress → larger phase window

Phase Window Recovery



- **Phase window almost fully recovered after annealing @ 240°C**

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Conclusions

- ADPLL frequency and phase noise characterized for the first time using on-chip monitors
- Phase noise increases with stress for both open-loop and closed-loop configurations
- High temperature annealing can be used to recover most of the degradation
- Post-stress phase noise measurements critical for reliability assurance