All-Digital PLL Frequency and Phase Noise Degradation Measurements Using Simple On-Chip Monitoring Circuits

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***Abstract*— Using simple on-chip monitoring circuits, we precisely characterized the impact of hot carrier injection and bias temperature instability on frequency and phase noise degradation of a 65nm all-digital PLL circuit. Experimental data shows that PLL phase noise degrades with aging even though the output frequency is maintained constant due to the PLL feedback operation. Results show that applying high temperature annealing can recover most of the phase noise degradation.**

Keywords –Bias temperature instability (BTI); hot carrier injection (HCI); thermal recovery; phase-locked loop (PLL); phase noise

I. INTRODUCTION

While the effects of aging and recovery on devices and digital gates have been well studied, aging-induced shifts in mixed-signal circuits have not be widely reported due to the complexity of the circuit and the difficulty in measuring subtle performance shifts. Recent design trends toward digital intensive mixed-signal implementations (e.g, all digital PLL (ADPLL) [1] [2], time-based ADC [3] [4], digitally-controlled voltage regulators [5] [6]), warrant further investigation of aging issues in critical mixed-signal building blocks. To this end, this paper presents frequency and phase noise degradation data measured from a standard ADPLL circuit fabricated in a 65nm process, using simple on-chip monitoring circuits. Our study shows that precise measurement of aging-induced timing shifts in ADPLLs is possible using digital circuits such as counters, flip-flops, and a variable delay line. The proposed approach does not require an extensive test setup and allows automated testing using a simple serial interface. Detailed frequency and phase noise window data under various stress, recovery, and annealing conditions are presented.

II. TEST STRUCTURE AND EXPERIMENT FLOW

A. DCO and PLL Test Structure

The ADPLL test chip with on-chip monitors for measuring the frequency and phase noise degradation is shown in Fig. 1. The PLL itself contains a digitally controlled oscillator (DCO) with capacitor banks, a bang-bang phase frequency detector (BB PFD), a digital loop filter, and a

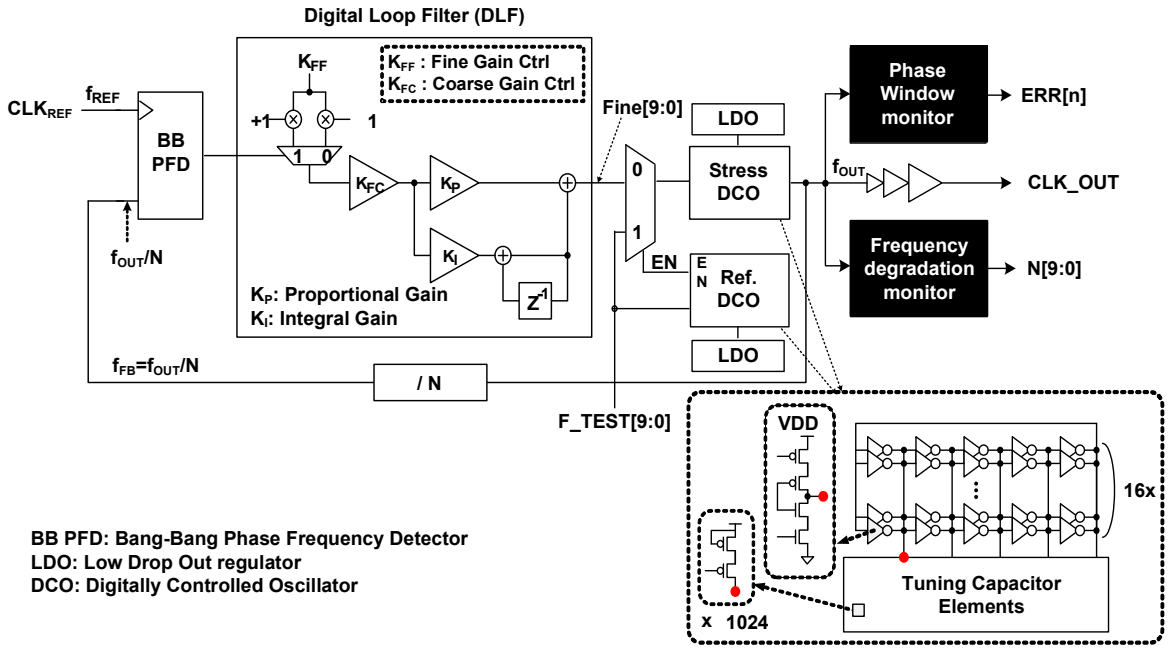


Fig. 1. All-digital PLL with on-chip frequency and phase noise measurements circuits.

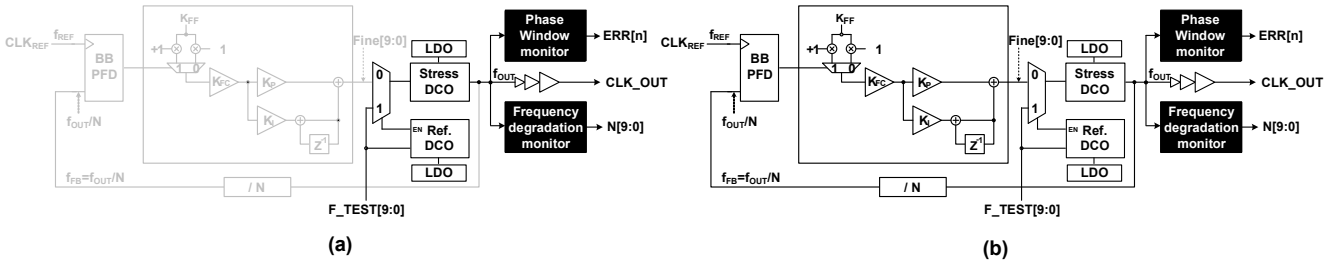


Fig. 2. (a) Open-loop test configuration. DCO's open loop frequency is measured. (b) Closed-loop test configuration. Locked ADPLL frequency is measured.

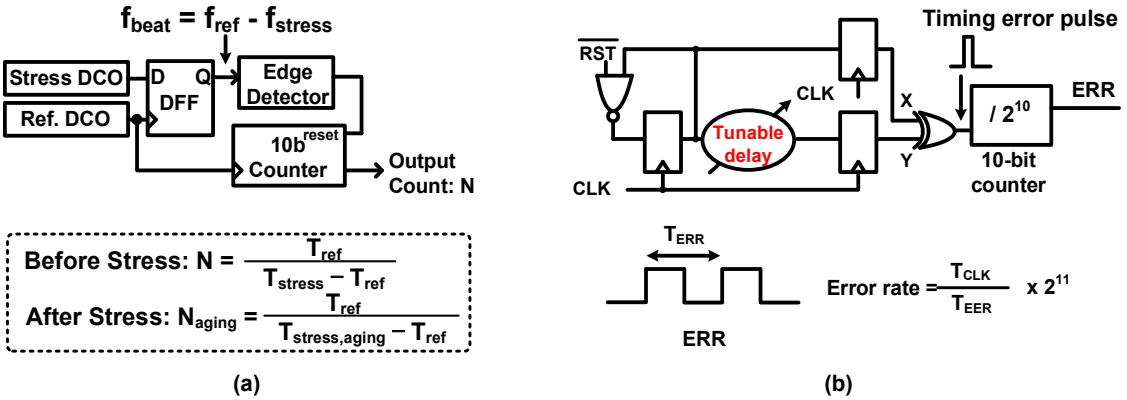


Fig. 3. (a) Frequency degradation monitor based on "silicon odometer" beat frequency detection scheme. (b) Phase window monitor based on a tunable delay.

frequency divider. During stress mode, a supply of 2.4V is applied to the stress DCO while the fresh reference DCO is powered off. The stressed DCO oscillates at its natural oscillation frequency inducing HCI and BTI. In measurement mode, the supply voltages of both DCOs are switched to the nominal voltage of 1.2V. On-chip LDOs are implemented for fast power supply transition between stress and measurement modes. We also employed on-chip monitor circuits to measure subtle frequency and phase noise shifts induced by device aging.

B. Experiment Flow

We measured the frequency and phase noise degradation (indirectly) which are critical performance parameters of a PLL system. To fully understand the aging implications on these parameters, we tested the ADPLL in both open loop and closed loop configurations. By simply turning off the feedback loop of ADPLL as shown in Fig. 2(a), we can measure the open-loop characteristics. High voltage stress was applied to study frequency and phase noise. We also measured recovery effect under different annealing temperatures. Fig. 2 (b) shows the standard ADPLL configuration for testing closed-loop characteristics.

C. Frequency and Phase Noise Window Monitors

Fig. 3(a) shows one of the on-chip monitors, which is the proven-and-tested beat frequency (BF) detection circuit for measuring the frequency shift of the stressed DCO [7]-[11]. The output signal of the D-flip-flop exhibits the beat frequency, $f_{beat} = f_{ref} - f_{stress}$. The beat frequency is measured by counting the number of reference DCO periods that can fit within one period of the phase comparator output signal. Using the digital output code N[9:0], we can compute the frequency shift in the stressed DCO with picosecond accuracy. The BF monitor can measure frequency shifts as small as 0.01% within a few microseconds. The short interrupt time prevents unwanted BTI recovery from corrupting the aging data.

Phase noise is typically characterized by measuring the PLL output clock signal using a high-speed sampling oscilloscope or spectrum analyzer. In this work, we implemented an on-chip phase window (PW) monitor circuit which can indirectly measure the phase noise amplitude.

The circuit shown in Fig. 3(b) consists of a tunable delay line, an XOR gate, sampling flops, and a 10-bit counter. Basically, the ADPLL clock period is compared with the tunable delay by measuring the error rate. Let us assume that initially the tunable delay is much shorter than the ADPLL clock period. Then, there will be no error and thus the counter value will be zero. As the tunable delay is gradually increased, errors will start to occur which can be detected by the XOR gate and tallied by the 10-bit counter. That is, any time there's an error in signal Y due to timing failure, the XOR gate generates an error pulse which increments the 10 bit counter. By measuring the average period of the counter output signal ERR and the period of the stressed DCO, error rate (or 1-error rate) can be calculated as shown in [12] [13]. This is how the left boundary of the phase window denoted as "short delay" in Fig. 4 is measured. As we continue to increase the tunable delay, the error will continue to rise, eventually reaching 100%. The actual error rate can be deduced based on the error count

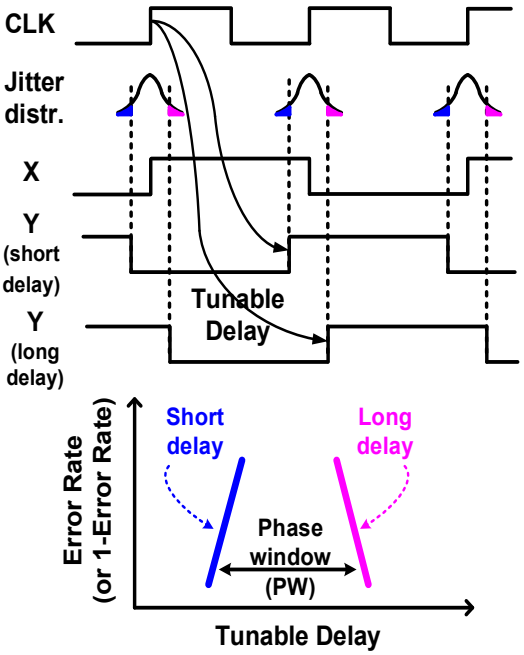


Fig. 4. Phase noise degradation can be indirectly measured by sweeping the tunable delay.

and the total number of cycles. The right side boundary in Fig. 4 is measured in this way. Phase noise in the ADPLL output will affect the error rate which can be indirectly monitoring using the proposal circuit. The phase window for a specific error rate can be obtained by measuring the tunable delay as shown in Fig. 4.

III. Experiment Results

A. Open-loop Stress and Recovery Experiments

We measured the open-loop DCO frequency using the BF monitor circuit in Fig. 5, while applying a 1.2V nominal voltage and a 2.4V stress voltage at 27°C. The stress frequency was the natural oscillation frequency of the DCO at 2.4V, which is 1.56 GHz. The beat frequency was measured at a nominal supply of 1.2V at 27°C, while the measurement interrupt time was 2µs. A combination of BTI and HCI caused a frequency shift of 8.49% after 2.22 hours of stress.

Fig. 6 shows the DCO phase window measured using the on-chip PW monitor. Since phase window measurements take a long time (minutes), for consistency, the frequency was measured after sufficient recovery. The phase window is defined as the range of tunable delay where error rate is higher than 1E-8. Fig. 6 (lower) shows the open-loop phase window versus DCO frequency degradation. The phase window becomes larger with more degradation in the DCO frequency.

Frequency recovery under different temperatures is shown in Fig. 7. Upon removing the 2.4V stress voltage, natural recovery at 27˚C induced a 0.76 % frequency recovery (Fig. 7, upper, (b)). Then we place the package on a hot plate for annealing experiments. After a 20 second annealing period where the package temperature is raised to 110˚C, we let the package cool down to room temperature before taking

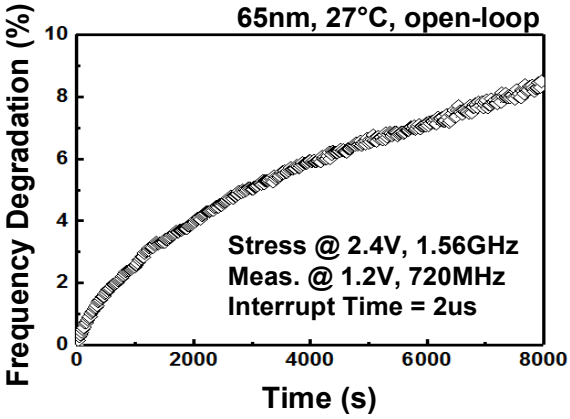


Fig. 5. Measured frequency degradation of open-loop DCO using beat frequency detection circuit.

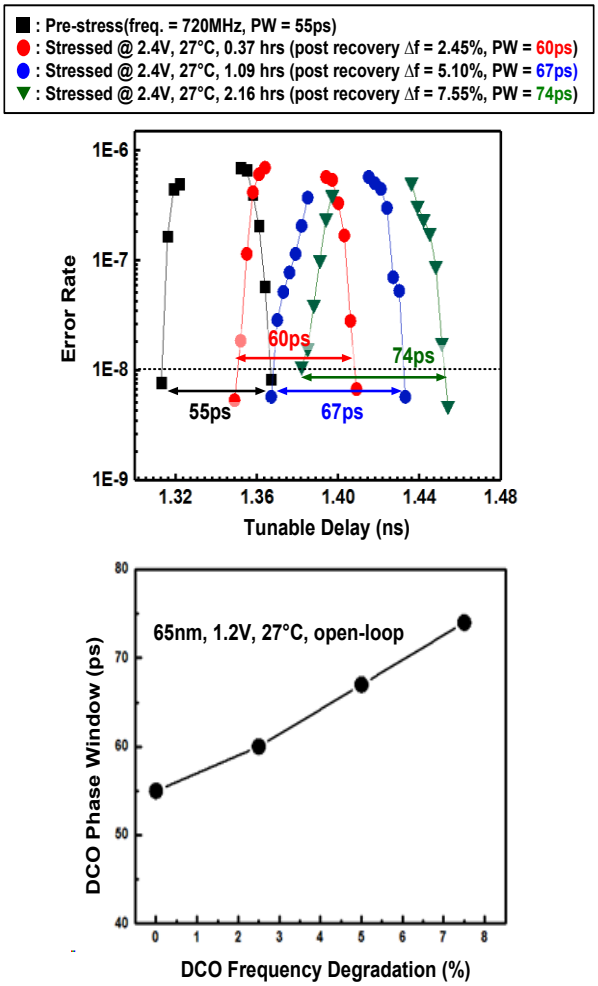
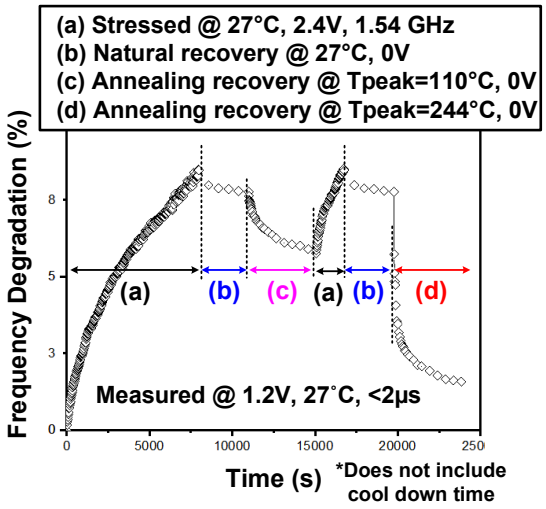


Fig. 6. (Upper) Measured open-loop DCO phase window before and after stress. (Lower) Measured open-loop phase window versus open-loop DCO frequency degradation.

frequency measurements. Fig. 7 (lower) shows the measured temperature profile for a single annealing cycle. We repeat this cycle while measuring the frequency between each annealing period. Annealing the chip repeatedly at 110°C resulted in a 1.9% frequency recovery. We reapplied the 2.4V stress voltage to bring the chip back to the state after the natural



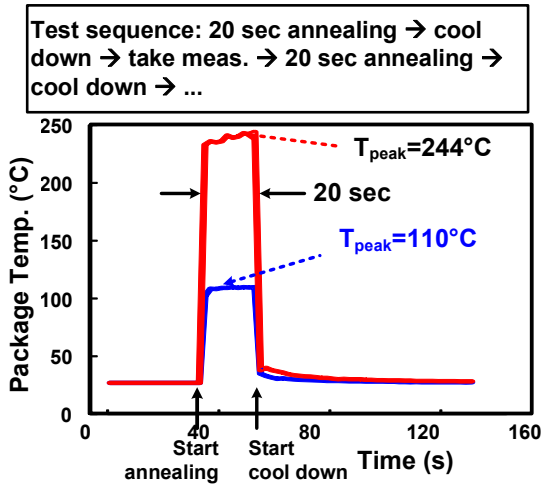


Fig. 7. (Upper) Measured frequency shift under different stress and recovery conditions. (Lower) Annealing test sequence. The package is cooled down after each 20 second annealing period to ensure accurate frequency measurements.

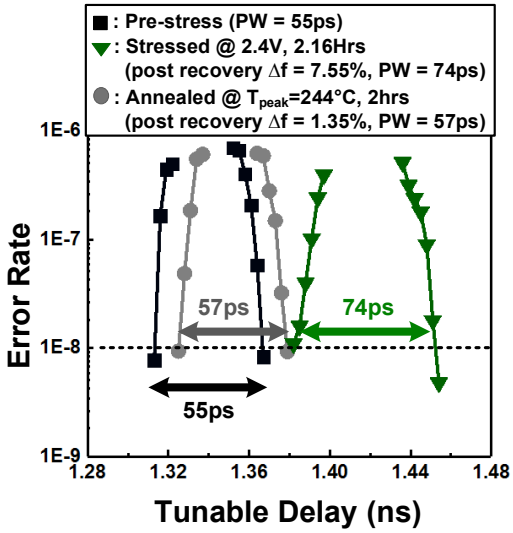


Fig. 8. Measured open-loop phase window curves for pre-stress, stressed, and annealed DCOs.

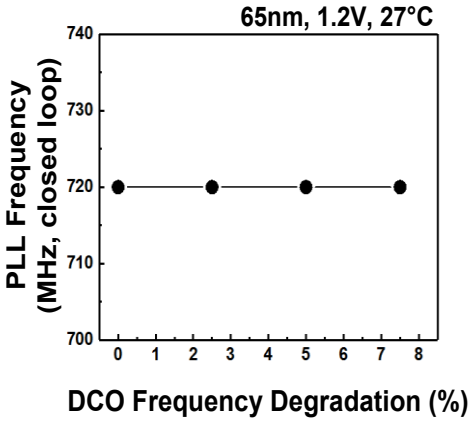


Fig. 9. Closed-loop PLL frequency remains constant despite DCO frequency degradation.

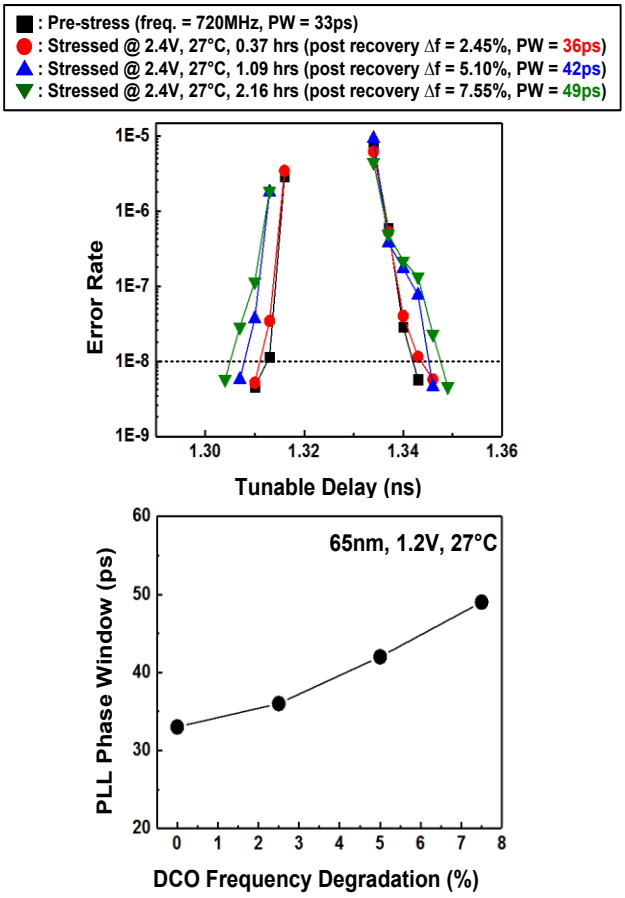


Fig. 10. Measured PLL phase window before and after stress.

recovery, and repeated the annealing test at 110°C and 244°C. Annealing at higher temperature results in stronger recovery. We suspect annealing cures HCI degradation while BTI is mostly recovered by natural recovery. Fig. 8 shows the phase window recovery after annealing at 244°C for 2 hours.

B. Closed-loop Stress and Recovery Experiments

Fig. 9 shows the closed-loop ADPLL frequency versus open-loop frequency degradation of DCO. The open-loop

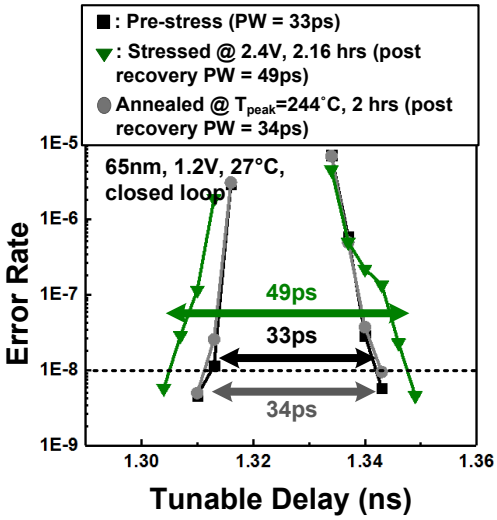


Fig. 11. Measured closed-loop phase window curves for pre-stress, stressed, and annealed DCOs.

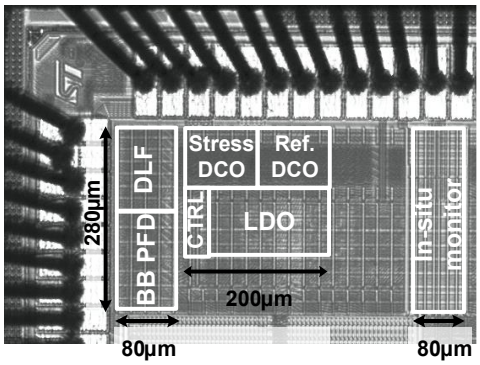


Fig. 12. 65nm all-digital PLL test chip die photo

DCO is degraded under same stress condition as that described in previous section, stress voltage 2.4V and 27˚C. And, after the stress, the frequency of closed-loop PLL was measured in nominal condition, 1.2V and 27˚C. Even though the DCO frequency is degraded, the feedback loop of the ADPLL ensures that the output frequency is constant. Fig. 10 shows the phase window of the ADPLL versus the DCO frequency degradation. Unlike the open-loop results, the error rate curves are all centered around the same output frequency, however, the phase noise window degrades with longer stress times. For instance, a 7.55% degradation in DCO frequency caused the phase window to increase by 16ps. Fig. 11 shows the phase window recovery of the closed-loop configuration after natural recovery and annealing at 244°C for 2 hours. The phase noise window is reduced from 49ps (before annealing) to 34ps (after annealing). The ADPLL test chip was fabricated in a 65nm CMOS process, and the die microphotograph is shown in Fig. 12.

IV. Conclusion

Using simple on-chip monitoring circuits, we have experimentally shown that PLL phase noise degrades with aging even though the output frequency is maintained constant due to the PLL feedback operation. This has implications on ADPLL qualifications. Natural recovery alone was not enough to fully recover the phase noise due to permanent HCI and BTI damage. The proposed test structure was implemented in a 65nm CMOS process and tested under different annealing temperatures. In certain high-reliability applications where parts cannot be easily replaced and a long lifetime must be ensured (e.g. space electronics) [14] [15], annealing using an on-chip heat source may be a viable option.

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