A 0.0094mm^2/Channel Time-Based Beat Frequency ADC in 65nm CMOS for Intra-Electrode Neural Recording

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***Abstract*- A digital-intensive, low-area, time-based ADC optimized for in-situ neural recording is fabricated in a 65nm test chip and validated with *in-vivo* data. The intrinsic inversely proportional gain of a beat frequency based quantizer allows recording of sub-millivolt neural signals without any sophisticated amplifiers or filters. A low-area analog-front-end (AFE) is implemented with a standard digital logic inverter transimpedance amplifier and tunable low pass and high pass filters. The test chip achieves 20.9dB SNDR for a 1mVpp input at 416Hz with a bandwidth of 4.2 kHz and consumes 52µW at 0.8V. *In-vivo* evoked potentials and spontaneous activity were measured directly from a mouse cerebellum without any external components, validating the efficacy of the aggressive tradeoffs. These results are achieved in an area of 0.0094mm^2/channel, including on-chip AC coupling and filter passives, which makes this an attractive architecture for complete integration in ultra-high channel count neural recording systems.**

I. Introduction

In-vivo recordings from microelectronic electrode arrays are becoming clinically useful due to their promise of providing the capability to record from hundreds of neurons simultaneously [1-3]. This capability can provide neuroscientists and clinicians with the essential tools to study neurodegenerative disorders such as Alzheimer's disease. Since neural signal voltages are inherently small compared to full swing-inputs required by conventional ADCs, this poses challenging design constraints from the circuit designer's perspective. These challenges include; low input referred noise, ability to block DC offsets from the electrode-tissue interface, large dynamic range, tunable filters to identify clinically relevant signals, draw minimal power, and consume as little area as possible [1]. All of these constraints incur trade-offs between area, power, and recording quality. In the leading edge neural recording systems, silicon shank electrodes are outfitted with an astonishing 1356 channels [3]. Illustrated in Fig. 1 (above), each channel necessitates a custom pixel amplifier, providing small gain to the neural signals, and multiplexers which send the analog voltages through the shank to a series of high gain amplifiers in the base before it is digitized. While this is an impressive effort, it fundamentally suffers from transmitting analog voltages through the shank. Even though they reduce the aliasing due to the lack of low pass filters at the pixel by using an integrator, the in-band noise is still increased. Crosstalk between channels also degrades the performance. In addition, longer shanks require larger driving strength which reduces the available area in the shank for recording sites [4]. Moreover, high performance ADCs are designed to be optimal for a given

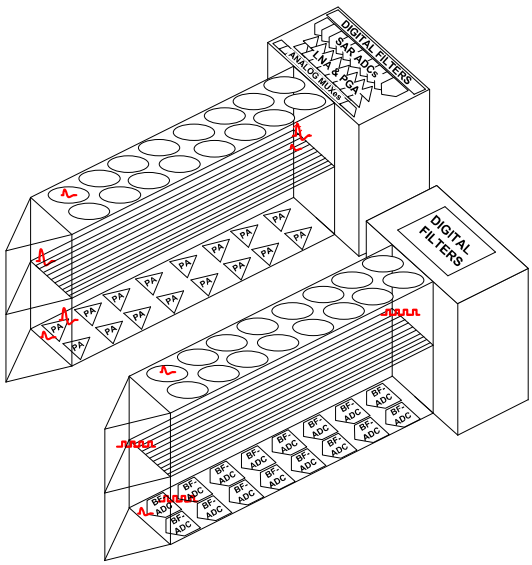


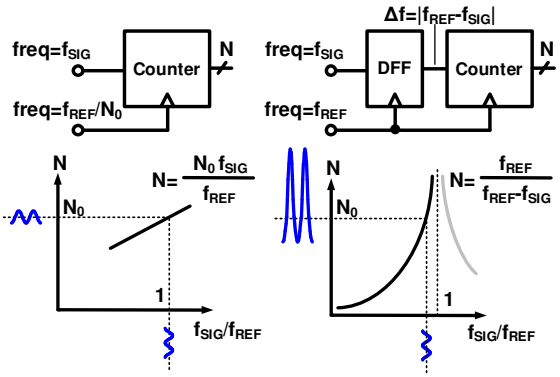
Fig. 1. (Above) Conventional neural recording system [3]. (Below) Envisioned application of the BFADC as digitizer at the recording site with minimal or no AFE overhead for achieving ultra-high channel count and high signal integrity.

sampling frequency in time multiplexed applications and incorporating additional channels requires a redesign [4]. If the signals could be digitized at the source in Fig. 1 (below), this would solve the issues caused by analog voltage transmission, enable full use of the electrodes in the shank, and enable the shank base to perform more complicated digital filtering.

The Beat Frequency Analog-to-Digital Converter (BFADC) is optimized explicitly for ultra-high density neural recording and can sense changes in signals down to 0.01% [5]. The basic principle of BFADC is to measure the frequency difference, or beat frequency, between two identical oscillator circuits, driven by a differential signal pair. By making the two oscillating frequencies similar to each other using trimming circuits, we can obtain an extremely high built-in amplification gain that is inversely proportional to the beat frequency. Furthermore, this digital-intensive approach is amenable to technology scaling and low voltage operation, unlike conventional approaches based on sophisticated analog amplifiers containing large passive devices. The 65nm test chip presented in this paper requires a petite 0.0094mm^2/channel for AC coupling, low-gain analog amplification, filtering, and digitization. By focusing on low-area, low-power, digital-intensive circuits, the BFADC could digitize neural signals directly at the electrode source without increasing the footprint of the electrode shank [2, 6]. In

this paper, the BFADC concept is described along with the test chip implementation and *in-vivo* physiological recordings from a mouse cerebellum.

II. BEAT FREQUENCY ADC WITH BUILT-IN AMPLIFICATION



N_0	Linear Quantizer	BF Quantizer (This work)	
	Gain*	Gain*	f_{SIG}/f_{REF}
50	50	49^2 = 2401	0.980
100	100	99^2 = 9801	0.990
200	200	199^2 = 39601	0.995

*Gain=slope=dN/d(f_{SIG}/f_{REF}))

Fig. 2. Comparison between linear VCO based quantizer and proposed BF quantizer. The frequency-to-count gain of the linear quantizer is proportional to the nominal count N_0 while that of the BF quantizer is proportional to $(N_0-1)^2$. The slope for several N_0 values are listed in the table. The high built-in gain of the BF quantizer allows neural signals to be measured with a modest AFE circuit.

Fig. 2 compares the schematic and gain characteristics of the conventional linear VCO based quantizer and the proposed BF based quantizer. The voltage input from external and reference electrodes drive two identical VCOs which generate clock frequencies f_{SIG} and f_{REF} that are linearly proportional to the electrode voltages.

$$f_{SIG} = K_{VCO}V_{SIG} \quad (1)$$
$$f_{REF} = K_{VCO}V_{REF} \quad (2)$$

In linear VCO based ADC, the number of cycles N in a fixed sampling period N_0/f_{REF} is counted. Here, N_0 is the nominal count which is chosen based on the target sampling frequency of the ADC. This gain corresponds to the slope of the straight line in Fig. 2 (left, middle). Since the slope is proportional to the nominal count N_0, the only way to increase the sensitivity to f_{SIG} is by counting for a longer sampling period which degrades ADC performance. Detection of sub-mV neural signals in this scheme necessitates a sophisticated high-gain low-noise AFE [5]. In contrast, the BF quantizer compares f_{SIG} to a reference that has a similar f_{REF} frequency. A standard D-flip-flop circuit is used to generate a beat frequency clock with a frequency of $\Delta f=|f_{REF}-f_{SIG}|$ [7]. The beat frequency is then converted to a digital count N by measuring the number of f_{REF} cycles that fits in a single beat frequency period. The BF count N can be expressed as:

$$N = \left\lfloor \frac{f_{REF}}{f_{REF}-f_{SIG}} \right\rfloor \quad (3)$$

To illustrate the BF quantizer operation further, let us consider the case where f_{SIG} is lower than f_{REF} by 1%. That is, $f_{SIG}=0.99f_{REF}$. This can be easily achieved in a real chip using trimming capacitors. The BF count N in this case will be 100 since it takes 100 cycles for the faster f_{REF} clock to overtake the f_{SIG} clock. If the count drops to 99, then this corresponds to a frequency difference of 1.010101...% between f_{REF} and f_{SIG} (i.e. $f_{SIG}=0.98989\ldots f_{REF}$) which translates into an f_{SIG} change of only ~0.01%. The same change in the output count (i.e. 100→99) would have required a 1% frequency change for the linear VCO scheme. Our analysis indicates that the sensitivity of the BF quantizer is about 100 times higher than that of a linear VCO quantizer for a nominal count of 100. In other words, the beat frequency operation effectively amplifies small voltage differences by the built-in non-linear relationship in (3). It's worth noting that the quantization error and sampling time of BFADC depend on the beat frequency. For instance, a smaller frequency difference between f_{REF} and f_{SIG} increases the quantizer gain and thereby reduces the quantization error, at the expense of a longer sampling period. The irregular sampling period can be circumvented by enabling the oscillators with a fixed frequency clock. This ensures that BF counts are generated at a fixed interval. The lower quantization error is the reason why BFADC achieves an extremely high gain for the dynamic range of interest.

Conventional designs rely on sophisticated amplifiers combined with a large-dynamic-range ADC to prevent the output signal from being saturated due to common-mode noise in the signal and reference voltages. This approach however incurs a large area overhead and requires significant design effort. Interestingly, the non-linear relationship of BF quantizer inherently suppresses common-mode noise effects. This is because the neural signal component in f_{REF}-f_{SIG} is amplified by the inverse relationship in (3) while common-mode noise contained in f_{SIG} or f_{REF} is not amplified. This unique property allows the BFADC to extract neural signals as small as 100μV from a noisy environment.

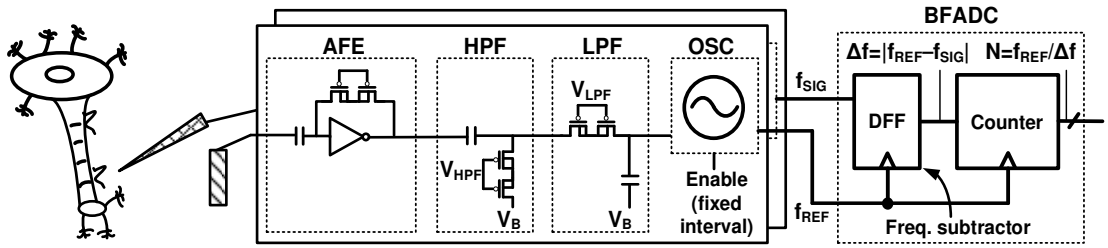


Fig. 3. Schematic representation of the implemented neural recording BFADC test chip. Each signal channel has an AFE, BPF, oscillator, and BFADC. The generated reference frequency can be shared across many channels.

III. TEST CHIP ORGANIZATION

The simplified schematic of the proposed neural recording IC consisting of a simple AFE (TIA gain of 5), passive filters, oscillator, and BFADC is shown in Fig. 3. The test chip was implemented in 65nm LP CMOS to validate the proposed low-area, all-digital neural recording system. The first stage of the AFE is an AC-coupled digital-inverter based TIA. By applying resistive junction feedback to the inverter, the operating point is fixed at the trip point and any perturbation on the input will be amplified at the output due to the steep slope. The feedback resistor is implemented as a pseudo-resistor by shorting the drains and connecting the body and gate to V_{DD} which puts the devices in cut-off to give the channel a large resistance. The primary drawback of using this configuration is the static current. However, this can be reduced to an acceptably low level by decreasing the supply voltage. In addition, simulation results have shown that very aggressive gate widths near minimum size still give good amplification performance. The trade off with using a smaller device is that the device noise is proportional to the g_m of the device which favors using larger devices. Since the BFADC has such high intrinsic gain, the extremely low area, and fully-digital implementation makes the junction feedback amplifier a pragmatic choice. The output of the amplifier is AC coupled by the first stage of the band pass filter (BPF) which prevents the DC offset of the TIA from setting the bias of the VCO. The pseudo-resistors are controlled by a gate bias, which enables tuning the pass band to physiologically relevant signals [1]. The HPF also sets the operating point for the VCO which is DC coupled through a pseudo-resistor. In this implementation, the VCO bias voltages are shared to further reduce the implementation overhead. The frequency tuning to set the operating point for the BFADC is controlled through digital tuning bits. A major improvement in this design over previous works [5, 7] is that the VCO is implemented as a current controlled oscillator (CCO). This replaces the need for a large unity gain buffer to drive the VCO. Instead, we implement a digital-intensive current control circuit which helps drive the entire channel area down making this configuration attractive for high channel count neural recordings.

IV. TEST CHIP MEASUREMENTS

Test chip measurements were performed in three scenarios: bench testing, *in-vitro* saline tank simulation, and *in-vivo* mouse electrophysiology. Power was supplied from a 9V battery and regulated with discrete voltage regulator ICs. In the controlled bench test, input signals were supplied from an Agilent 33520A function generator. An input of $1mV_{pp}$ at 416.6Hz was applied in which the full ADC chain provided a SNDR of 20.9dB at supply voltage of 0.8V. This is slightly less than previously reported BFADC designs [5, 7] due to the new buffer-less CCO having lower K_{VCO}. Additionally, previous works required two references to reconstruct the input signal where we employ a single reference. In this design the goal was to aggressively cut area while retaining enough performance to remain functional. Fig. 4 (above) shows the measured SNDR as a function of the input voltage. All measurements were recorded at a given

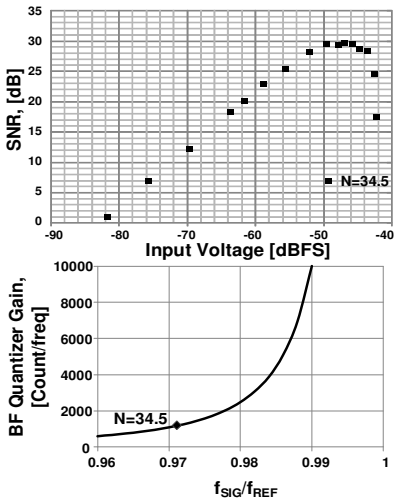


Fig. 4. (Above) Measured SNDR vs. input amplitude at a given BFADC operating point for a 416.6Hz signal sampled at 41.6kHz, dBFS=$1.2V_{pp}$. (Below) BF quantizer gain for the operating point above. For a typical BF count of ~100, the frequency to count gain is ~10,000, which is roughly two orders of magnitude higher than that of a linear counter.

TABLE I: PERFORMANCE COMPARISON

Parameters	This Work	[11]JSSC'17	[12]JSSC'16	[13]CICC'15	[5]CICC'15	[14]TCAS-I'15
ADC Type	Beat Freq.	VCO	CT-$\Delta\Sigma$	VCO-$\Delta\Sigma$	1-Step BF	Incr.-$\Delta\Sigma$
Process/Supply	65nm/0.8V	40nm/1.2V	130nm/1.2V	130nm/1.2v	65nm/1.2V	180nm/1.2V
Bandwidth	4.5kHz	200Hz	15MHz	1.7MHz	1.2KHz	4kHz
Sampling Rate	50kHz	3kHz	500MHz	250MHz	50kHz	8kHz
In_{0db} [dBFS]*	-84	-75	-80	-75	-86	-85
$SNDR_{1mVpp}$ [dB]**	20.9	35	20	14	22	22
$ENOB_{1mVpp}$ [b]**	3.17	5.52	3.03	2.03	3.36	3.36
Power	52uW	7uW	20mW	910uW	34uW	34.8uW
FoM @ F_{in} [pJ/Conv]***	683 @ 900Hz	380 @ 3Hz	81.4 @ 4.15MHz	66.6 @ 500kHz	1252 @ 300Hz	424 @ 175Hz
Chip Area [mm^2]	0.046	2.16	1.3	0.04	0.096	0.0564
Area/Ch [mm^2] (Relative)	0.0094 (1x)	0.135 (14.5x)	1.3 (138x)	0.04 (4.3x)	0.078 (8.3x)	0.0564 (5.9x)
Experiment	*In-vivo*	*In-vitro*	-	-	-	-

**Input Amplitude at SNDR=0dB, 0dBFS=1.2V* ***Reported at V_{in}=1mV_{pp}* ****FoM =Power/(2*BW*2^{ENOB})*

operating point with no tuning between inputs to simulate an actual use case. Fig. 4 (below) shows the analytical relationship between the BF quantizer gain and the default count. The power consumption of the total system (excluding scan and pad I/O power) at 0.8V is 52µW. The input referred noise of our entire recording chain is calculated to be 5.3µVrms by the histogram method given in [8]. The area required for a single channel to be digitized includes the AC coupling capacitor, AFE, BPF, CCO, and BFADC is $0.0094mm^2$ as seen in Fig. 5. The reference electrode AFE area can be amortized over many channels and does not require its own quantizer. *In-vitro* recordings were performed in a saline solution with a shielded beaker to reduce external noise [9]. The saline environment simulates the charge transfer mechanism that occurs in the brain. Measured SNDR for a $1mV_{pp}$ sine wave at 800Hz was 4.5dB *in-vitro*. Table 1 compares this work to state of the art time-domain ADCs. The Walden FOM is the same used in [5, 12]. Our reported FOM is higher than [12, 13] due to their larger bandwidth, but otherwise in line with or outperforms state of the art. [11] reported higher SNDR but it has 22.5x lower bandwidth which could be due to the long required sample period since it is a linear multi-phase VCO. This restricts the efficacy to only local field potentials (LFPs), whereas with the BFADC can record LFPs and spikes.

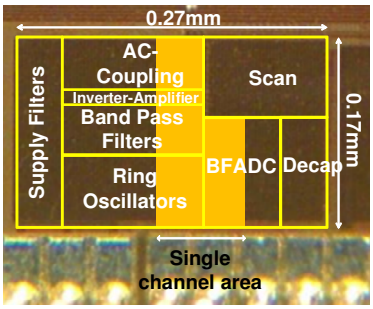


Fig. 5. Die photo of the test chip in 65nm LP CMOS. Box highlighted in orange represents the area of a single channel.

V. *IN-VIVO* RECORDING RESULTS

All animal handling procedures were approved by the Institutional Animal Care and Use Committee of the University of Minnesota. Electrophysiology was performed using the neural recording BFADC in an anesthetized (WT)/FVB mouse for recording from the Purkinje fibers (PF) in the cerebellum shown in Fig. 6a. Fig. 6b shows the microscope image placement of the stimulating Tungsten microelectrode and glass micropipette recording electrode. Activity-dependent optical imaging was used to determine the location of the PF, indicated by the arrow, using flavoprotein autofluorescence in Fig. 6c [10]. PF can have two sets of pre-synaptic and post-synaptic activations from stimulation, manifested here as positive (depolarization) and negative (hyperpolarization) signal swings. Fig. 6d (top) shows one section of the experiment recorded with the BFADC. Stimulation was applied at 1Hz and evoked potentials were observed and overlaid in the middle plot. PF have two sets of activations corresponding to the notch and the main peak seen in the traces. No digital filtering or off-line processing was applied to the data other than (3) in Fig. 6d (bottom). The BFADC gives a relative measurement, so extracellular potentials were estimated by applying a $1mV_{pp}$ input, applying (3), and then scaling to match a $1mV_{pp}$ digitized output. A benefit of the non-linear quantization is the BFADC does not saturate during stimulation artifacts manifested as the large hyperpolarization. The difference in the relative magnitudes of the peaks in the middle and bottom plots highlights the non-linear quantization in the BF counts. The plots confirm the ability of the BFADC to record both sets of PF activations.

VI. CONCLUSION

In this paper, we have described the implementation of a fully-digital, low area neural recording system based on the BFADC. It was able to achieve 20.9dB SNDR for a 1mVpp signal while occupying a meager $0.0094mm^2$. The high sensitivity to small signal changes reduced the need for sophisticated high gain amplifiers and massive filter circuits which makes the BFADC architecture well suited for neural recording as evidenced by the *in-vivo* experiment.

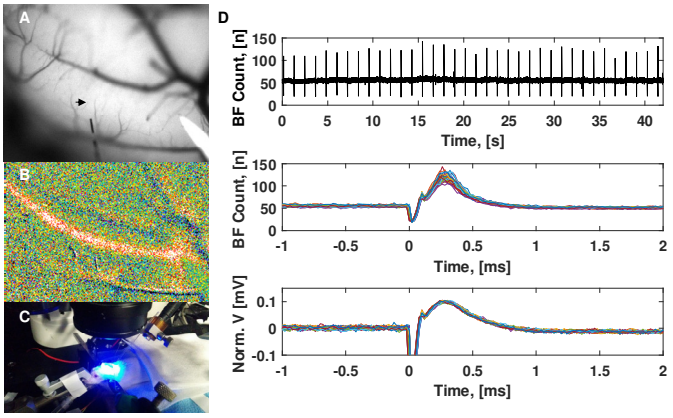


Fig. 6. Results from the *in-vivo* recording experiment.

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