A 2.1 pJ/bit, 8 Gb/s Ultra-Low Power In-Package Serial Link Featuring a Time-based Front-end and a Digital Equalizer

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Outline

- Motivation
- Proposed Time-Based Receiver
- Proposed Delay Line Based Time Amplifier
- 65 nm Test Chip Measurement results
- Conclusion
• **System-in-Package**
  - Multi-chip integrated in a single package
  - Enables small form factor
RX Equalization Technique

- Continuous Time Linear Equalizer (CTLE)
- Decision Feedback Equalizer (DFE)
RX Equalization Technique

- ADC-based receiver enables digital equalization
- Take advantage of CMOS scaling
RX Equalization Technique

- Voltage-to-Time Converter (VTC)
- Time Amplifier (TA)
- Time-to-Digital Converter (TDC)
- Digital-intensive time-based front-end
- Signal amplifier is performed in the time domain while equalization is performed by DSP circuits
# Time-Based Receiver

<table>
<thead>
<tr>
<th>Receiver Type</th>
<th>Digital</th>
<th>Analog</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Frontend</td>
<td></td>
<td></td>
<td>Fully-Analog</td>
</tr>
<tr>
<td>Analog DFE</td>
<td></td>
<td></td>
<td>Voltage based</td>
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<tr>
<td>Analog Frontend</td>
<td></td>
<td></td>
<td>Analog FE, Digital Equalizer</td>
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<td></td>
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<td><strong>Time based</strong></td>
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<tr>
<td>Proposed Time-based Frontend</td>
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<td></td>
<td></td>
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<tr>
<td>Digital FE, Digital Equalizer</td>
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Voltage-to-Time Converter

- Time delay is determined by input signal
- Voltage signal is converted to time delay

Related Time Amplifier

- NAND gate based Ring-oscillator design
- Speed is limited by oscillator frequency

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Proposed Time Amplifier

- Open loop delay line for short range application
- Inverter based design
Proposed Time Amplifier

![Diagram of Proposed Time Amplifier]

STARTi ——> 1x ——> 1x ——> 1x ——> STARTo

NX ——> NX ——> NX

STOPi ——> 1x ——> 1x ——> 1x ——> STOPo

NX ——> NX ——> NX

EN
Proposed Time Amplifier

- STARTi driving by N+1 inverter \( \Delta t \) longer than STOPi

\[ \Delta t \]

AND gate delay > \( \Delta t \)
Proposed Time Amplifier
Time Amplifier Simulation Results

- High linearity between input and output delay @ 2GHz operation

![Graph showing high linearity between input and output delay](image)
• Conventional 4-bit Vernier line TDC
• Total TDC delay should smaller than 1 UI
Digital DFE

- 4-bit digital comparator
- TDC output compared with predetermined weights
Proposed Transceiver for SiP

- Transmitter: PRBS, FFE and clock
- Receiver: 4-lane time-based receiver, digital equalization and BER monitor
• TX and RX chip are integrated in same package
In-situ BER Eye-Diagram Monitor


- X-axis: Phase delay in red box
- Y-axis: Time offset in blue box
Measured BER Bathtub

- Eye width = 0.12UI @BER < 10^{-12}
Measured BER Eye Diagram

- Y-axis: time offset code corresponds to voltage offset
## Performance Summary

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</thead>
<tbody>
<tr>
<td>RX Architecture</td>
<td>Off Chip</td>
<td>4x Flash ADC</td>
<td>4x Flash ADC</td>
<td>32x SAR ADC</td>
<td>4x TDC</td>
</tr>
<tr>
<td>Front-end Type</td>
<td>Voltage-Based (CTLE +VGA)</td>
<td>Voltage-Based (VGA)</td>
<td>Voltage-Based (VGA)</td>
<td>Voltage-Based (Analog FFE)</td>
<td>Time-Based (VTC+TA)</td>
</tr>
<tr>
<td>Data Rate</td>
<td>10 Gb/s</td>
<td>10.3125 Gb/s</td>
<td>8.5-11.5 Gb/s</td>
<td>10 Gb/s</td>
<td>8 Gb/s</td>
</tr>
<tr>
<td>Technology</td>
<td>65nm</td>
<td>40nm</td>
<td>40nm</td>
<td>65nm</td>
<td>65nm</td>
</tr>
<tr>
<td>Voltage</td>
<td>1.1V</td>
<td>0.9V</td>
<td>1V</td>
<td>1V</td>
<td>1V</td>
</tr>
<tr>
<td>Resolution</td>
<td>4 bit</td>
<td>6 bit</td>
<td>6 bit</td>
<td>6 bit</td>
<td>4 bit</td>
</tr>
<tr>
<td>BER</td>
<td>&lt;1E-9</td>
<td>&lt;1E-12</td>
<td>&lt;1E-12</td>
<td>&lt;1E-10</td>
<td>&lt;1E-12</td>
</tr>
<tr>
<td>RX Area (w/o DSP)</td>
<td>0.288 mm²</td>
<td>0.27 mm²</td>
<td>0.82 mm²</td>
<td>0.38 mm²</td>
<td>0.0192 mm²</td>
</tr>
<tr>
<td>Power Efficiency (pJ/b)</td>
<td>8.1 (RX only)</td>
<td>15.1 (RX only)</td>
<td>18.9 (RX, includes Clock)</td>
<td>7.9 (RX only)</td>
<td>2.1 (TX+RX, includes DSP power)</td>
</tr>
</tbody>
</table>
Conclusion

- Digital-intensive time-based front-end receiver is proposed for SiP application

- The proposed time-based receiver achieves an energy-efficiency of 2.1 pJ/b while the area is 0.0192mm²

- The proposed VTC and TA based implementation significantly reduces circuit complexity and has favorable scaling properties