Statistical Characterization of Radiation-Induced Pulse Waveforms and Flip-Flop Soft Errors in 14nm Tri-Gate CMOS Using a Back-Sampling Chain (BSC) Technique

Saurabh Kumar\textsuperscript{1}, M. Cho\textsuperscript{2}, L. Everson\textsuperscript{1}, H. Kim\textsuperscript{1}, Q. Tang\textsuperscript{1}, P. Mazanec\textsuperscript{1}, P. Meinerzhagen\textsuperscript{2}, A. Malavasi\textsuperscript{2}, D. Lake\textsuperscript{2}, C. Tokunaga\textsuperscript{2}, H. Quinn\textsuperscript{3}, M. Khellah\textsuperscript{2}, J. Tschanz\textsuperscript{2}, S. Borkar\textsuperscript{2}, V. De\textsuperscript{2} and C. H. Kim\textsuperscript{1}

\textsuperscript{1} University of Minnesota, Minneapolis, MN
\textsuperscript{2} Intel Corporation, Hillsboro, OR
\textsuperscript{3} Los Alamos National Laboratory, Los Alamos, NM

kumar175@umn.edu

This research was, in part, funded by the U.S. government. The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the U.S. government
Outline

- Motivation
- Back-sampling chain (BSC) technique
- 14nm test-chip and board design
- Neutron irradiation test results
- Strike pulse re-construction results
- Conclusion
Device level soft error rate has been decreasing with scaling.
Scaling Impact on SER in Tri-Gate

- Lower SER with tri-gate scaling
  - Taller/narrower fins, higher resistance
  - Smaller cross-section
Scaling Impact on SER in Tri-Gate

- Lower per-transistor SER 😊
- Higher transistor count, lower VDD → increased chip-level SER 😞
- Challenge: Collecting statistically significant amount of data in limited beam time
Logic SET vs. Sequential SEU/MBU

Combinational logic path

Flop storage node

VDD

V_node

Time

Trip point of next stage

Flipping threshold
• For higher SER sensitivity:
  - $I_{\text{restore}}$ : High $V_T$, smaller size ($N_1$)
  - $I_{\text{strike}}$ : High flux/LET (radiation parameter)
  - $C_{\text{node}}$ : Small fan-out, device size
  - $V_{\text{sw}}$ : High $V_T$, smaller device ($P_2$)
Technique #1: Current Starved Buffers

• Starved buffer chain: High sensitivity
**Technique #1: Current Starved Buffers**

- **Alternate starving:**
  - Lower $I_{\text{restore}}$, lower $V_{\text{sw}}$
- **Analog bias knobs:**
  - Tunable resolution and sensitivity
Technique #2: Back-Sampling Chain

- Later stage rising edge back-samples previous stage falling edge
Example: Short vs. Long Strike Pulse

<table>
<thead>
<tr>
<th>Time</th>
<th>Stage Output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>'1'</td>
</tr>
<tr>
<td></td>
<td>'1'</td>
</tr>
<tr>
<td></td>
<td>'1'</td>
</tr>
<tr>
<td></td>
<td>'1'</td>
</tr>
<tr>
<td>'0'</td>
<td>'0'</td>
</tr>
<tr>
<td>'0'</td>
<td>'0'</td>
</tr>
<tr>
<td>'0'</td>
<td>'0'</td>
</tr>
<tr>
<td>'0'</td>
<td>'0'</td>
</tr>
<tr>
<td>'0'</td>
<td>'0'</td>
</tr>
<tr>
<td>'0'</td>
<td>'0'</td>
</tr>
<tr>
<td>'0'</td>
<td>'0'</td>
</tr>
<tr>
<td>'1'</td>
<td>'1'</td>
</tr>
<tr>
<td>'1'</td>
<td>'1'</td>
</tr>
<tr>
<td>'1'</td>
<td>'1'</td>
</tr>
</tbody>
</table>

Unsampled original bits

<table>
<thead>
<tr>
<th>Time</th>
<th>Stage Output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>'1'</td>
</tr>
<tr>
<td></td>
<td>'1'</td>
</tr>
<tr>
<td></td>
<td>'1'</td>
</tr>
<tr>
<td></td>
<td>'1'</td>
</tr>
<tr>
<td>'0'</td>
<td>'0'</td>
</tr>
<tr>
<td>'0'</td>
<td>'0'</td>
</tr>
<tr>
<td>'0'</td>
<td>'0'</td>
</tr>
<tr>
<td>'0'</td>
<td>'0'</td>
</tr>
<tr>
<td>'0'</td>
<td>'0'</td>
</tr>
<tr>
<td>'0'</td>
<td>'0'</td>
</tr>
<tr>
<td>'1'</td>
<td>'1'</td>
</tr>
<tr>
<td>'1'</td>
<td>'1'</td>
</tr>
<tr>
<td>'1'</td>
<td>'1'</td>
</tr>
</tbody>
</table>

Short trail of 0's
Tunable Resolution and Sensitivity

- Allows multiple resolution-sensitivity sweeps
- Facilitates strike pulse re-construction
Back-Sampling Chain (BSC) Array

**Unit Cell**

- Buff In
- Scan Out
- Scan In
- Buff Out

**BSC Arrays**

<table>
<thead>
<tr>
<th>Technology</th>
<th>14nm, 9-metal layer, tri-gate HKMG CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die area</td>
<td>3.7mm x 2.2mm</td>
</tr>
<tr>
<td>Core voltage</td>
<td>&lt;0.7V</td>
</tr>
<tr>
<td>Scan voltage</td>
<td>1.1V</td>
</tr>
<tr>
<td>Array dimension</td>
<td>250x500x12 = 1.7 million BSC stages</td>
</tr>
</tbody>
</table>
• Beam diameter = 3 inches
• 3x3 SER test-chips fit within beam area
• FPGA: JTAG support for automated control
• 15.3 million BSC stages per board
LANL Neutron Irradiation Test

- 10 stacked boards with 90 test-chips in parallel irradiated under neutron beam at Los Alamos National Laboratory (LANL)
• Neutron beam specs
  • Avg. energy spectrum range: 1.38 – 750 MeV
  • Avg. neutron flux: ~ 4.2x10^4 neutrons/cm^2/s
A strike on buffer node induces SET

FF Data = '0'
FF Data = '1'

560 rows
250 columns
Neutron Test Data: SEU/ MBU

A strike on flop storage node induces SEU/ MBU

FF Data = '0'
FF Data = '1'

560 rows
250 columns
• With lower VDD, sampling cut-off drops and wider SET pulses are sampled
• $Q_{\text{crit}}$ decreases with lower VDD, increasing SER
• With stronger starving (lower $V_{GS}$), sensitivity increases and sampling threshold drops, sampling wider SET pulses
SET Pulse Re-construction
SET Pulse Re-construction

Circuit simulator/ Matlab model

Double-exponential model

JDD-bias sweeps allow to vary sampling cut-off

Sampling Cut-offs

Pulse width (ns)

Time

Voltage

Pulse count

0.4V VDD, 0.30V VGS
0.5V VDD, 0.30V VGS
0.6V VDD, 0.30V VGS

Slide 21
SET Pulse Re-construction

Circuit simulator
Matlab model

SET Pulse Re-construction

VDD: 0.5V
FWHM$_{AVG}$: 218ps
Amplitude$_{AVG}$: 0.42

FWHM: Full width at half maximum
SET Pulse Re-construction

- Higher amplitude = shorter pulse width (lower FWHM)
- To our knowledge, this is the first time individual strike pulses are reconstructed
SET Pulse Re-construction

VDD=0.5V

- FWHM_{AVG}: 218ps
- Amplitude_{AVG}: 0.42

VDD=0.4V

- FWHM_{AVG}: 222 ps
- Amplitude_{AVG}: 0.45

- Lower VDD: pulse amplitude ↑, pulse width ↑
## Comparison with Prior Art

<table>
<thead>
<tr>
<th></th>
<th>TDC based circuit [1]</th>
<th>Pulse shrinking [2]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Unit cell layout</strong></td>
<td>Irregular, not easily scalable</td>
<td>Regular, scalable</td>
<td>Regular, scalable</td>
</tr>
<tr>
<td><strong>Sensitivity tuning</strong></td>
<td>Fixed by design</td>
<td>Fixed by design</td>
<td>Variable using bias knobs</td>
</tr>
<tr>
<td><strong>Resolution</strong></td>
<td>&gt; 30ps</td>
<td>&gt; 1ps</td>
<td>&gt; 1.3ps</td>
</tr>
<tr>
<td><strong>$Q_{\text{crit}}$ sensitivity</strong></td>
<td>1x</td>
<td>0.6x</td>
<td>9x</td>
</tr>
</tbody>
</table>

* Results reproduced in 14nm process

---

Flip-Flop SEU/MBU

- SER exponentially increases with lower VDD
- At lower VDDs, MBU become more dominant

### Failure In Time (normalized)

- FIT: # of SER per flop per billion hours

### Cross-section (normalized)

- 5-bit
- 4-bit
- 3-bit
- 2-bit
- 1-bit

![Graph showing FIT and Cross-section vs. VDD](image-url)
Conclusion

- BSC chain technique proposed with 9x lower $Q_{\text{crit}}$ and picosecond range resolution
- BSC circuit detects SET, SEU, and MBU
- 14nm test-chip irradiated under neutron beam
- Individual strike pulses re-constructed based on neutron irradiation data
- Next step: SER model framework development