Statistical Characterization of Radiation-Induced Pulse Waveforms and Flip-Flop Soft Errors in 14nm Tri-Gate CMOS Using a Back-Sampling Chain (BSC) Technique

Saurabh Kumar, Minki Cho[±], Luke Everson, Hoonki Kim, Qianying Tang, Paul Mazanec, Pascal Meinerzhagen[±], Andres Malavasi[±], Dan Lake[±], Carlos Tokunaga[±], Heather Quinn[*], Muhammad Khellah[±], James Tschanz[±], Shekhar Borkar[±], Vivek De[±], Chris H. Kim

[±]Intel Corporation, Hillsboro, OR 97124, USA; [*]Los Alamos National Laboratory, Los Alamos, NM 87545, USA;
Dept. of ECE, University of Minnesota, 200 Union Street SE, Minneapolis, MN 55455, USA (Email: kumar175@umn.edu)

Abstract

A novel BSC circuit with tunable current starved buffers demonstrates higher sensitivity, scalability & accurate statistical characterization of radiation-induced SET pulse waveforms & flip-flop SER in 14nm tri-gate CMOS, thus enabling improved SER estimation & analysis for a range of supply voltages including NTV.

Introduction

Radiation-induced soft errors (SER) in logic circuits, flip-flops and memory arrays in scaled CMOS process can pose significant reliability challenges for mission critical applications. Although FinFET and tri-gate technologies can improve SER immunity to some extent [1, 2], single event upset (SEU) and multi-bit upset (MBU) error rates increase exponentially at low voltages, especially in the near-threshold voltage (NTV) operating regime. SER and critical charge (Q_{Crit}) modeling & analysis for different logic circuits require accurate statistical characterizations of the radiation-induced single event transient (SET) pulse waveforms (Fig. 1) across a range of operating voltages including NTV. The measured distribution of pulse widths and amplitudes can be used for estimating SEU and MBU failure-in-time (FIT) rates for different designs.

SET pulse width measurements have been reported previously using (1) multiple logic chains connected to a time-to-digital converter through an OR-gates network [3], or (2) a pulse shrinking chain of skewed inverters with local sampling flip-flops that measure the number of stages it takes for the SET pulse to disappear [4]. In this paper, we use a novel back-sampling chain (BSC) circuit with tunable current starved buffers implemented as large arrays in 14nm tri-gate CMOS to directly measure SET pulse width & amplitude statistics, as well as SEU/MBU FIT rates of the embedded flip-flops, for a large number of chips under neutron beam irradiation across a range of voltages including NTV. We demonstrate improved sensitivity to radiation strikes, as well as better pulse width distortion effects and unit cell layout regularity, leading to more robust accurate measurement statistics. The detection threshold and pulse width measurement resolution are adjusted using tuning voltages to enabling accurate reconstruction of the original strike waveforms.

Back-Sampling Chain (BSC) Circuit

The proposed BSC circuit (Fig. 2) allows the detection of very low amplitude transients, thus enabling capture of many more radiation-induced SET events. Current starved inverters are used to limit the restore current and thereby enhance sensitivity to radiation strikes. Since radiation-induced SET events are relatively infrequent even for accelerated high intensity irradiation testing, the improved sensitivity helps produce a statistically meaningful number of SET pulse measurements within a limited duration of irradiation. Symmetrical bias voltages at the PMOS & NMOS gate inputs in alternating inverter stages are used for buffer starving which is utilized for tuning measurement sensitivity and detection threshold.

The pulse width expands as it propagates through the chain, the expansion rate being governed by the degree of buffer starving. To measure the original pulse width, each buffer output is sampled by a D flip-flop which is clocked by the rising edge of a later stage signal. The sampled data containing the pulse width information is periodically read out using the scan chain embedded in the BSC array. The original voltage waveform is reconstructed using the measured pulse width and the detection threshold as determined by simulations in conjunction with post-silicon calibration of the buffer circuit. The number of stages between the clock node and data input node of the flip-flop is fixed by design (2 full rows or 250x2=500 stages), and it determines the maximum pulse width that can be measured. Post-silicon calibration results show that at nominal supply voltage, a maximum pulse width of 10ns can be measured. This is sufficient for capturing most of the significant SET pulses.

Thus, the main advantages of the BSC circuit (Fig. 4) are: (i) large arrays can be implemented without compromising measurement accuracy due to the regular unit cell layout structure (Fig. 3); (ii) sensitivity to radiation strikes is 9X higher while resolution & sensitivity can be tuned post-silicon (Fig. 4); (iii) non-ideal pulse width distortion effects can be eliminated by local sampling; and (iv) SEU & MBU FIT rates of the BSC flip-flops can be readily measured using the scan-out chain.

SET Pulse & Flip-Flop SER Measurements on Testchips

A testchip containing 12 identical 250X560 BSC arrays is implemented in 14nm tri-gate CMOS (Fig. 4). A JTAG control unit on the chip with 6 ports (Fig. 5) controls the BSC arrays. A chip configurator module is used to support 3 modes: calibration, irradiation and scan-out. All peripheral modules (IOs, JTAG & chip configurator) operate at a higher VDD of 1.1V to ensure minimal or no strikes during scan-out. The BSC arrays are tied to a separate VDD rail to enable SET/SEU/MBU measurements at different supply voltages. During the one-time post-silicon calibration, pulse expansion rates are measured for different buffer starving voltages. In the irradiation mode, the chip is exposed to neutron beam for SET/SEU/MBU measurements.

Neutron irradiation tests were performed at Weapons Neutron Research (WNR) facility at Los Alamos National Laboratory with 54 chips, containing more than 180 million current starved inverters total, exposed to a spallation neutron beam. The average beam flux was 4.1×10^4 neutrons/cm^2/s. 6 boards, each consisting of 9 chips and an FPGA, were tested to obtain sufficient amount of statistically meaningful data (Fig. 5).

Isolated random flips indicate SEU/MBU in the flop storage nodes, while long trails of flips signify SET strikes in the buffer chain (Fig. 5). Pulse width is measured from the number of consecutive bit flips in the array. Measured SET pulse width distributions for different buffer starving and supply voltage values (Fig. 7) show that wider pulses are detected at higher sensitivity due to the double-exponential pulse waveform shape. The pulse width distributions change with supply voltage as well, as expected.

The original SET pulse waveforms as well as the joint distributions of pulse amplitude & full width half max (FWHM) are reconstructed for different supply voltages from the pulse width measurements for a range of detection thresholds (buffer starving voltages) at each supply voltage (Fig. 6). Measured SEU/MBU cross-section versus supply voltage results for the flip-flops embedded in the BSC array scan chain, as shown in Fig. 6, confirm the inverse dependence of SER on supply voltage. These measured SET pulse distributions can be used in conjunction with the measured SEU/MBU cross-section results to calibrate and validate accuracies of predictive SER & Q_{Crit} models for different circuits across a range of voltages including NTV, thus paving the way for full chip level SER estimation and analysis.

Acknowledgements The authors thank R. Corkran, C. Roberts and N. Seifert for their help. This research was, in part, funded by the U.S. government. The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the U.S. government.

References [1] N. Seifert, TNS, 2015 [2] S. Lee, IRPS, 2015 [3] T. D. Loveless, IEEE TNS, 2012 [4] J. Furuta, IRPS, 2011.

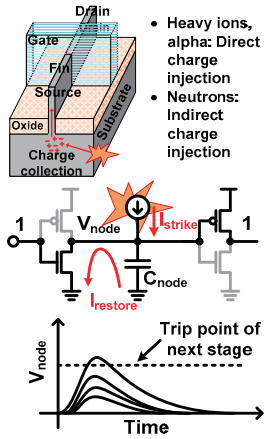


Fig.1: Particle strike and voltage pulse in logic circuit.

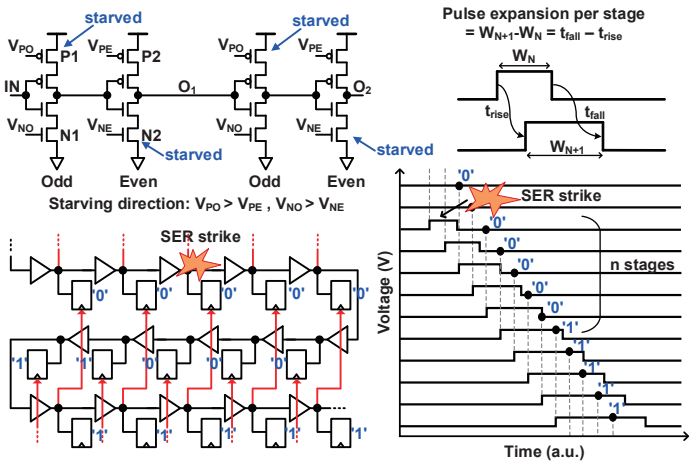


Fig.2: Current starved buffers and back-sampling circuit for accurate strike waveform characterization

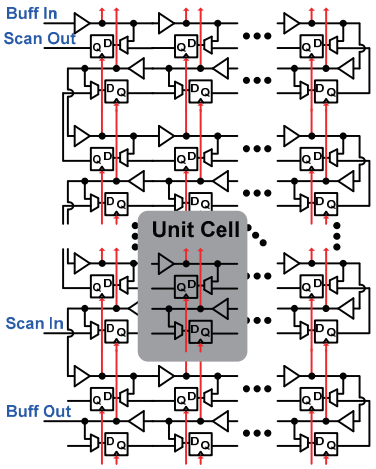
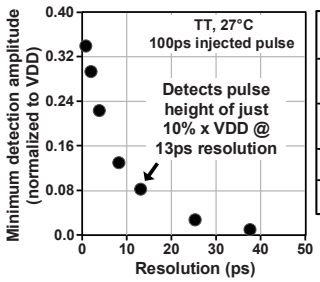
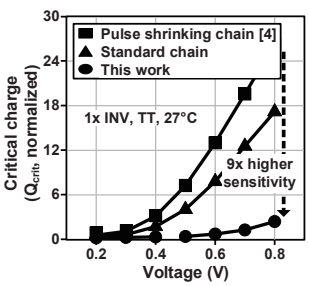
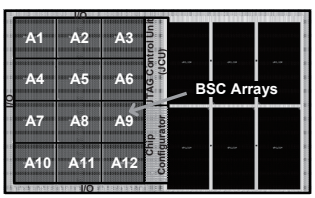


Fig.3: Back-sampling chain (BSC) implemented as a 250x560 array with 12 such arrays in each test-chip.



	TDC based circuit [3]	Pulse shrinking [4]	This work
Unit cell layout	Irregular, not easily scalable	Regular, scalable	Regular, scalable
Sensitivity tuning	Fixed by design	Fixed by design	Variable using bias knobs
Maximum resolution	> 30ps	> 1ps	> 1.3ps
SER sensitivity	1x	0.6x	9x





Technology	14nm, 9-metal layer, tri-gate HKMG CMOS
Test-chip die area	7.7mm x 3.7mm
Core + test area	3.7mm x 2.2mm
Core voltage	<0.7V
Scan voltage	1.1V

Fig.4: (clockwise from top-left) Min. detection amplitude vs pulse width measurement resolution; Comparison summary of proposed and previous work; 14nm BSC testchip layout and summary table; Q_{crit} sensitivity comparison between proposed and prior work

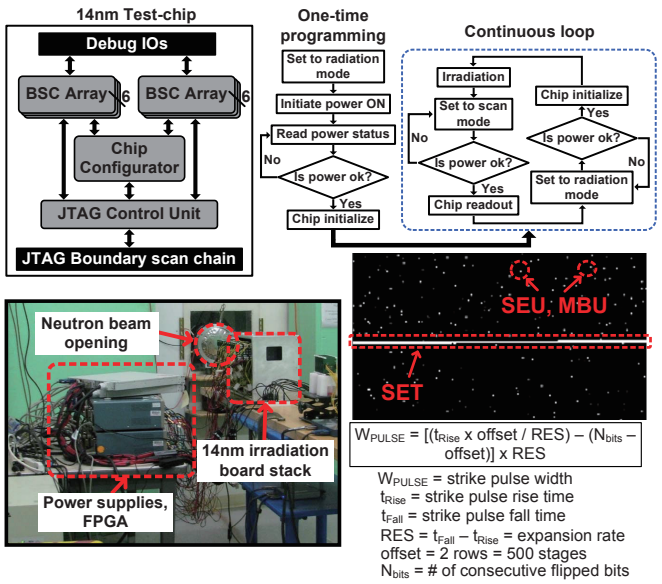


Fig.5: (clockwise from top-left) Top level 14nm SET testchip architecture; Neutron irradiation test-flow implemented in FPGA board; Portion of irradiated BSC array showing SET, SEU and MBU errors. Strike pulse with calculation method; Measurement setup at Los Alamos National Laboratory

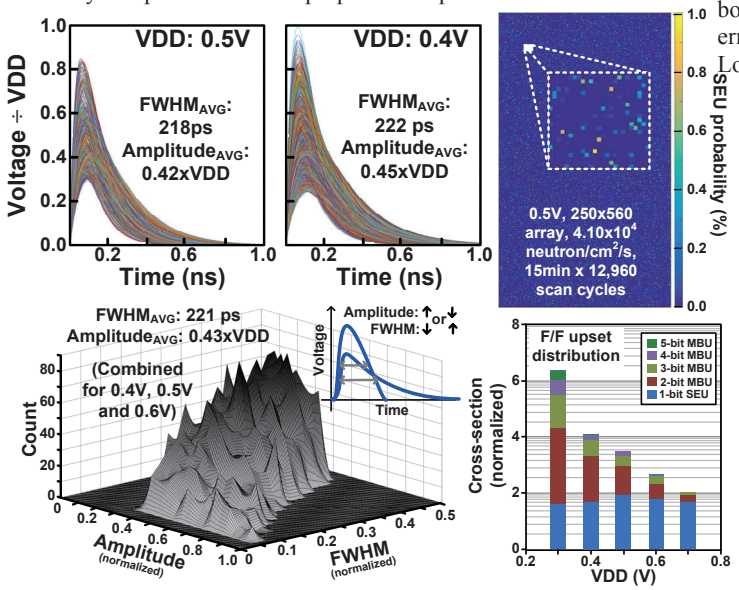


Fig.6: (clockwise from top-left) Re-constructed strike pulse waveforms based on measured pulse width data at 0.5V and 0.4V; SEU probability distribution map; Measured MBU cross-section vs VDD; Joint distribution of amplitude and FWHM of re-constructed pulses

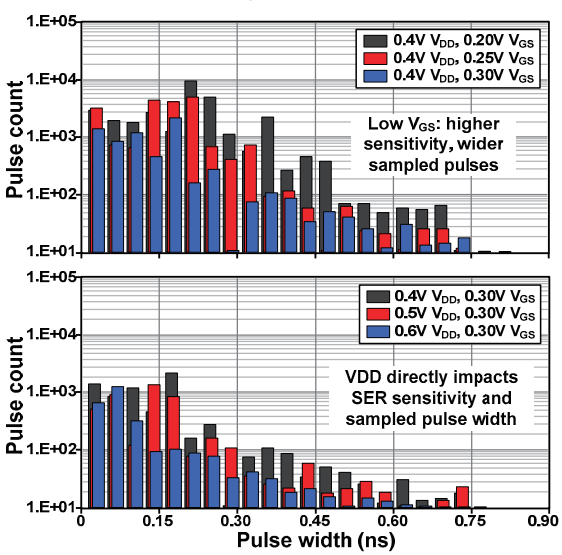


Fig.7: Measured strike pulse width distributions for different starving and VDD conditions.