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A Circuit based Approach for Characterizing High Frequency Electromigration Effects

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***Abstract*—A test chip for studying electromigration (EM) effects under various DC and AC stress conditions was implemented in a 32 nm High-k Metal Gate (HKMG) process. The stress current, which can be either DC, pulsed DC, square AC or real AC, was generated on-chip and applied to 60 devices-under-test (DUTs) in parallel. An on-chip voltage-controlled-oscillator was designed to generate a stress frequency higher 1 GHz while on-chip metal gate heaters were used to raise the DUT temperature to >300 °C for accelerated testing. Both abrupt and progressive failures were observed under DC and pulsed DC stress modes. The abrupt failures could be further divided into two categories based on the final resistance value. Although no AC stress induced failures were observed during our extensive stress experiments, AC stress did have an impact on the subsequent DC EM lifetime. Two possible scenarios are given to explain the high frequency EM results.**

***Index Terms*—Electromigration, high frequency, AC stress, metal gate heater, circuit based characterization.**

I. Introduction

WHEN wires are subject to a high current stress for extended periods, their resistance values can shift due to the formation and growth of voids within the metal structure. This phenomenon, referred to as electromigration (EM), manifests as an abrupt or gradual increase [1] in the wire resistance depending on the location of the void. EM is the primary back-end-of-line reliability mechanism affecting modern integrated circuits: EM failures occurring in the power grid can result in increased IR drop, while EM failures in signal wires can result in increased interconnect delay. EM lifetime depends on several parameters such as stress current, temperature, mechanical stress profiles, and vacancy distribution. Wires in power girds are normally exposed to a DC or pulsed DC current which have been studied extensively in previous works [2] [3]. In contrast, EM effects in signal wires are subject to a bidirectional AC stress current which has been overlooked in the past due to (i) the minimal impact it has on EM lifetime and (ii) the difficulty in applying a high frequency stress current/voltage [4]. However, the increased current density coupled with higher joule heating in advanced technologies such as FinFET has led to renewed interest in AC EM, especially at high stress frequencies [5]. The main challenge with studying high frequency AC EM effects is that wires must be stressed at-speed using a gigahertz clock. Unfortunately, the highest off-chip generated stress frequency reported for EM studies is just 5 MHz [3] due to I/O bandwidth limitations.

In this work, we have fabricated a test chip in a 32 nm high-k metal-gate technology specifically to study high frequency EM effects. Unlike previous efforts where stress current was provided by off-chip equipment, an internally generated high frequency clock was used to stress the devices-under-test (DUTs). Stress current was applied to an array of DUTs in parallel, thereby enhancing the test efficiency by N times, where N is the number of wires in the test structure that can be stressed simultaneously. Four stress modes are supported in our test chip: pure DC, pulsed DC, square AC and real AC. We used on-chip metal gate heaters to raise the die temperature to above 300 °C for accelerated testing. On-chip heaters have been used in the past for reliability studies [6]. However, to our knowledge, none of them were designed for temperatures as high as 325 °C. In our experiments, both abrupt and progressive failures were observed. Even though there were no apparent changes in the wire resistance under AC stress, we were able to study the effect of AC stress by measuring the DC EM lifetime after applying a pre AC stress current. A detailed analysis on the measured EM data are provided in this paper.

II. Proposed Circuit Based Electromigration Test Structure

A. DUT with Stress and Measurement Circuits

Fig. 1 (above) shows the EM test DUT implemented in the 32 nm test chip. The wire structure was built on M1 metal layer and has a dimension of L = 200 µm and W = 50 nm. 60 wires were implemented in a single test chip. Each wire is connected to a wide M2 plate through a single via at both ends to form a standard M2-M1-M2 downstream/upstream DUT structure. Each wire is connected to individual tri-state driver circuits capable of switching at giga-hertz frequencies. The different stress modes can be configured using the input and enable signals of the drivers.

Fig. 1 (below) illustrates the four stress modes supported in our chip: DC, pulsed DC, square AC and real AC. DC stress mode can be applied by driving the left and right ends of the wire to opposite values as shown in the table. Stress current flows continuously in one direction which pushes the metal atoms in one direction, resulting in the shortest time

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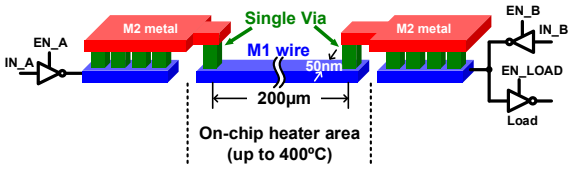


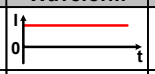
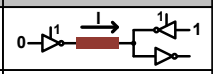
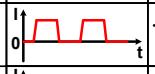
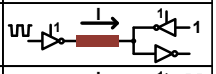
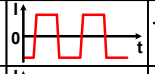
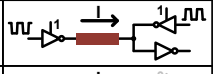
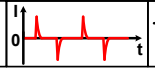
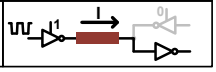
Stress Mode	Current Waveform	Driver Operation
DC		
Pulsed DC		
Square AC		
Real AC		

Fig. 1. DUT structure and different stress modes supported in the 32 nm test chip.

to failure. DC stress mode mimics the current waveform in a power grid. For pulsed DC stress mode, the stress current is turned on and off by toggling one of the drivers while leaving the other driver on. The current behavior is similar to that of a power grid that is periodically activated. Square AC stress mode has a bidirectional (i.e. positive and negative) stress current. In our experiment, we applied a balanced square AC current, meaning that the duty cycle is 50%. Although square AC is not a realistic scenario occurring in a real chip, it is helpful in studying the EM healing behavior when a reverse direction current is applied. Real AC represents the current waveform occurring in signal wires. It includes both forward and backward currents charging and discharging a capacitive load. This stress mode was not studied in previous works because the real AC current can only be generated using on-chip driver circuits.

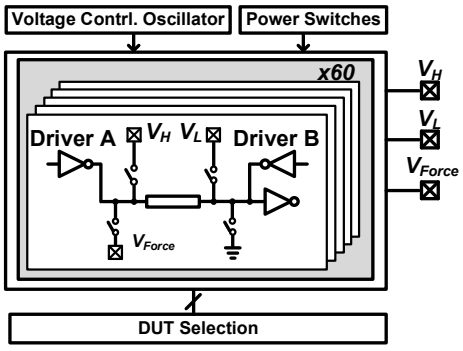


Fig. 2. EM test array with 60 DUT wires.

Fig. 2 shows the simplified diagram of the overall test chip. An on-chip voltage controlled oscillator generates a high frequency gigahertz stress clock. A power switch block is used to switch the VDD between a 1.5 V stress voltage and the 0.9 V nominal voltage. We used the 4-terminal Kelvin method to measure the individual DUT wire resistance through shared I/O pads. A small current is applied to the pad denoted V_{Force}, and then the voltage difference between V_H and V_L was measured. The resistance value is the ratio between the voltage difference and the sourced current. All 60 DUTs share the same V_{Force}, V_H and V_L pads. Wires can be individually accessed using transmission gate based selection switches configured by a scan chain.

B. Heater Design and Temperature Control

For accelerated EM testing, the DUT temperature and current density must be increased. According to Black's equation [7], EM lifetime is an exponential function of temperature and a weaker function of current density. Therefore, in addition to applying a higher voltage during stress mode, we included on-chip metal gate heaters shown in Fig. 3. The heaters are located underneath the DUTs and can raise the DUT temperature to a high temperature. After several trial and errors, 325 °C was found to be a safe temperature that would allow accelerated testing without damaging the chip package. Off-chip heaters cannot be used in our experiment because: 1) the peripheral circuits cannot withstand a temperature as high as 325 °C, and 2) the packaged chips attached to the PCB can easily melt and deform when an external heat source is used. With a local heater, the high temperature is only contained to the DUT region which can alleviate both issues.

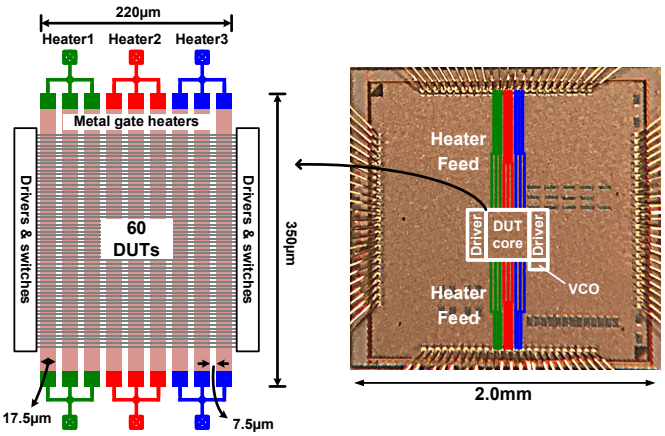


Fig. 3. (Left) Vertical metal gate heaters placed underneath 60 horizontal EM wires. (Right) Die photo of the 32nm EM test chip.

The heating area was 220 µm by 350 µm and contains 9 metal-gate heater strips. Each of them is 17.5 µm wide and the heater-to-heater spacing is 7.5 µm. To reduce the number of I/O pads, we group the 9 heater strips into 3 heater groups. Each group can be controlled individually to ensure uniform temperature across the heating box. To avoid EM in the metal-gate heaters themselves, we periodically switched the direction of the heater current, which provides the same heating power but without any EM failures in the heaters.

For accurate testing, the DUT temperature must be continuously monitored and regulated. Thermal diode based temperature sensors could not be used since the target temperature is higher than the safe operating temperature of the sensor circuitry. So instead, we opted to use the heater resistance itself as the temperature monitor. The heater resistance value will increase linearly with temperature so by measuring the temperature coefficient of resistance (TCR) at known temperatures,

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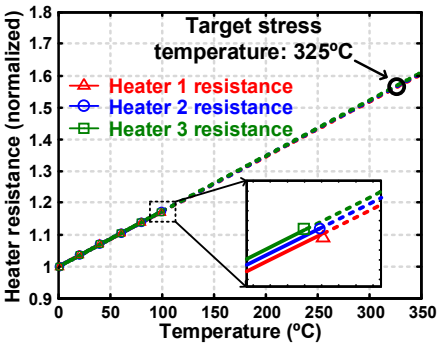

Fig. 4. Temperature Coefficient of Resistance (TCR) measurements from 3 heater leads and temperature extrapolation method.

we can deduce the chip temperature. This was done by placing the chip in a temperature chamber and measuring the TCR while varying the temperature from 0 °C to 100 °C. Excellent linearity between temperature and resistance was verified as shown in Fig. 4. Based on the TCR value, we can indirectly measure the DUT temperature using the extrapolation method described in Fig. 4. For instance, a 56% increase in resistance compared to 0 °C corresponds to the target temperature of 325 °C.

Another issue we experienced during actual measurements was the excessive leakage current in the selection switches at high DUT temperatures. The excess leakage current corrupted the resistance data. To alleviate this issue, we lowered the DUT temperature to 100 °C during measurements as shown in Fig. 5. Each stress interval was 10 minutes. The temperature ramp up and ramp down each takes about 15 seconds and measuring the resistance of all 60 DUTs takes about 1 minute. Note that it was not practical to wait for the DUT temperature to stabilize to room temperature due to the long settling time. The on-chip heater allowed fast temperature transition which in turn reduced the test time.

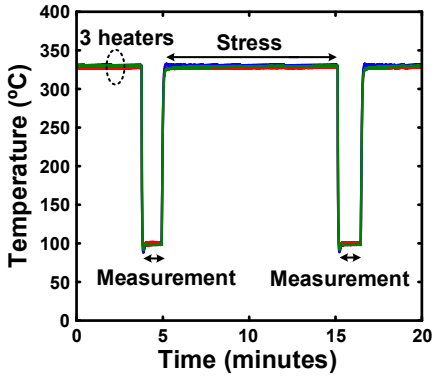

Fig. 5. Temperature cycling for stress and measurement modes. The DUT temperature was lowered from 325 °C to 100 °C during resistance measurements to suppress leakage current in the selection switches.

The test chip measurement setup is shown in Fig. 6, and an automated script was developed for efficient long term testing (Fig. 7). The program consists of two control loops: stress/measurement control loop and temperature control loop. After measuring the TCR and configuring the stress mode, the

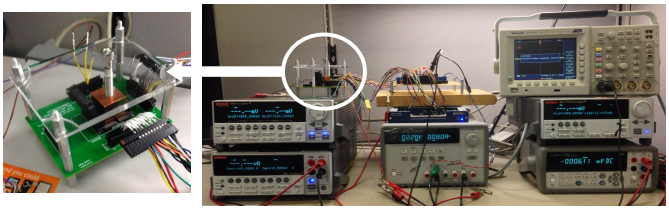

Fig. 6. 32 nm EM test chip measurement setup.

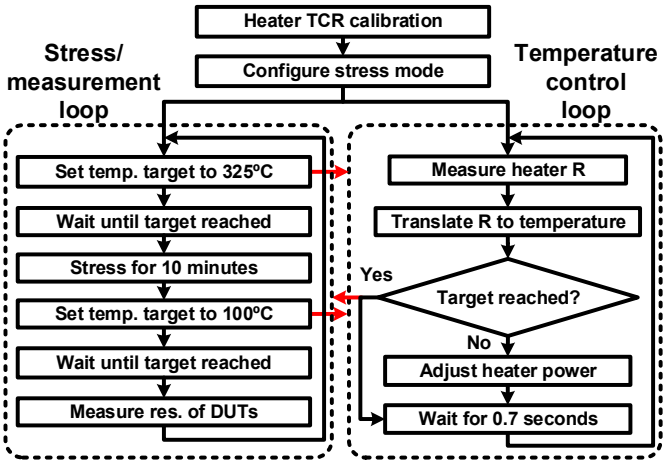

Fig. 7. Script based automated test flow. Two control loops (stress/measurement and temperature control) were implemented.

stress/measurement loop requests the target temperature to the temperature control loop. The temperature control loop adjusts the three heater voltages until the target temperature is reached. Once the target temperature is reached, the stress/measurement loop takes over.

C. Suggested Design Improvements and Test Procedure Guidelines

- Transistor aging may degrade the stress current with time, and hence may need to be avoided or limited in order to obtain pure EM results. Large devices should be considered, which can generate a large stress current without an excessively boosted supply voltage. New circuit topologies that can cancel out transistor aging effects may need to be developed.
- The temperature of the measurement circuit should be kept low. This can be achieved by increasing the distance between the heating area and measurement circuit area, and attaching a heat sink to the test chip.
- Temperature across the chip could be made more uniform by employing more heater stripes, in both horizontal and vertical directions.
- In our test chip, all DUTs share the same stress mode and stress frequency. So only one stress condition can be applied to each chip. This may inadvertently introduce some chip-to-chip variation effects. In future work, the test chip should be designed in a way that different stress conditions (e.g. DC, pulsed DC, real AC, and square AC)

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can be applied to different parts of the same chip during a single experiment.

- We were unable to monitor the stress current of each DUT as all DUTs share the same power supply. In future design, if the stress can be enabled or disabled individually for each DUT, we will be able to monitor the stress current of each individual DUT.
- To improve the stability of test setup, we suggest soldering the test chip to the test PCB, instead of using a test socket.
- To prevent EM failures in the heaters themselves, wide metal layers and a large number of vias should be used in heater feeds. In addition, the heater current direction can be switched periodically.
- To suppress the leakage current which may corrupt the Kelvin resistance measurements at high temperatures, IO devices may be used in the measurement circuits.

III. RESISTANCE MEASUREMENT RESULTS

We first recorded the fresh wire resistance values. The average resistance of the 60 DUTs measured from 7 chips at 100 °C were 955.6, 936.5, 896.1, 984.6, 953.5, 887.0 and 934.4 Ω. The standard deviations were 4.7, 4.7, 7.9, 10.7, 7.4, 7.8 and 6.9 Ω, respectively. Next, we apply the various stress modes and measure the resistance of each DUT every 10 minutes. The resistance traces were used to analyze various EM behaviors. The criteria for EM failure used in this work is when the resistance increases by 10% compared to its fresh value. Next, we provide a detailed analysis of the measured EM data.

A. DC and Pulsed DC Stress Results

Fig. 8 shows resistance traces under a DC stress current. Two failure types can be seen: 1) abrupt failure, where the wire resistance instantaneously jumps to a large value; and 2) progressive failure, where the resistance increases gradually. Upon further examination, we found that the abrupt failures can be divided into two sub-types based on the final resistance value. Type 1 abrupt failure is when the final resistance value is above 100 KΩ, while type 2 abrupt failure is when it is between 3 KΩ and 10 KΩ. In addition, we observed temporary healing in type 1 abrupt failures, which was also reported in a previous work [8]. Temporary healing lasted for up to 40 minutes before the wires were broken again. Fig. 9 shows sample resistance traces under DC stress mode and 200 MHz pulsed DC stress mode, showing type 1 and type 2 abrupt failures as well as progressive failures. Some type 1 abrupt failures switched to type 2 abrupt failures.

The different failure types can be explained by the location of the void [9] [10] as illustration in Fig. 10. When current flows through a wire, metal atoms are pushed away from their originally locations resulting in a void. If the void is located underneath the via and completely blocks the connection between the upper metal barrier layer and the bottom metal, then an open-circuit failure occurs, which was defined as type 1 abrupt failure. However, if the void doesn't completely block the connection and leaves a weak connection between the

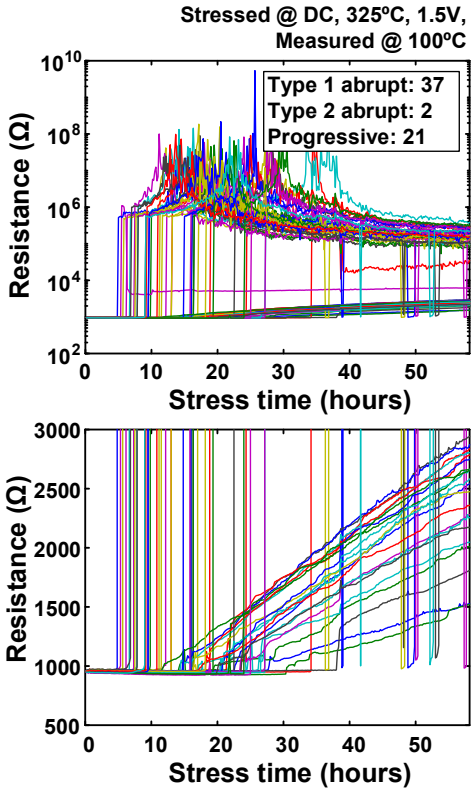

Fig. 8. Resistance traces under DC stress.

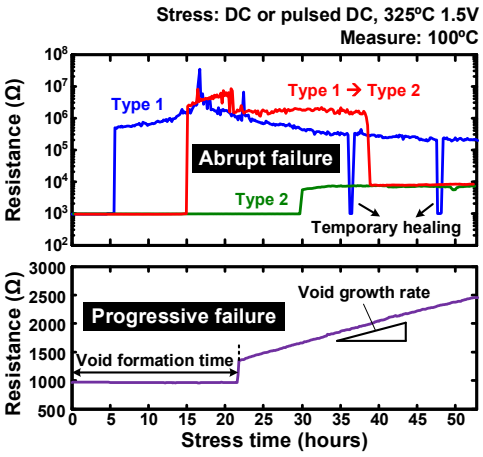

Fig. 9. Resistance trace samples showing abrupt and progressive failures.

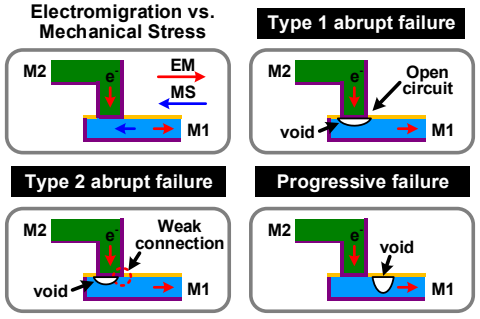

Fig. 10. Void location of different failure types.

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barrier layer and bottom metal, the resistance ends up being moderate, which was defined as type 2 abrupt failure. Fig. 8 (above) also shows that after the initial resistance jump, the wire resistance continues to increase before it peaks. This can be attributed to two reasons: (i) some weak EM persisting after the abrupt failure, or (ii) the reduced leakage current caused by transistor aging. The mechanical backstress causes recovery in the wire resistance resulting in a resistance peak. As for progressive failure, the void is formed inside the wire. Since stress current still flows after the initial resistance increase, the void continues to grow and therefore the resistance continues to increase [11].

Temporary healing occurred in a small number of test wires. If healing is a repeatable process, then it could be explained by the reasons suggested by A. W. Hunts [8]. Although the work was performed decades ago in an aluminum metallization process, their explanation could still be valid in analyzing our test results. The reasons outlined in [8] are discussed next: (a) The first possible reason is the thermal contraction/expansion cycle. The sharp temperature cycling (325 °C for stress and 100 °C for measurement) enabled by the on-chip heater could induce excessive thermal contraction/expansion in the test wire, causing the broken wire segments to reconnect. Once the stress current is restored, electromigration will resume and induce a failure again. (b) The second possible reason could be annealing effects at high temperatures. The metal atom diffusion rate could be very high during stress mode which may cause new metal islands to form inside the electromigration void and develop into larger metal grains that may restore the connection. (c) Mechanical back stress, albeit small in a long wire, could be the third reason for the healing process. The metal atom movement induced by EM results in compressive stress at the anode. The mismatch in material stress results in mechanical stress which counter balances the electrical stress, and hence pushes back the atoms towards their original locations. Initially, electrical stress is stronger than mechanical stress, so EM failure occurs. When abrupt failure occurs, electrical stress no longer exists due to the absence of stress current, while mechanical stress persists, causing the voids to recover.

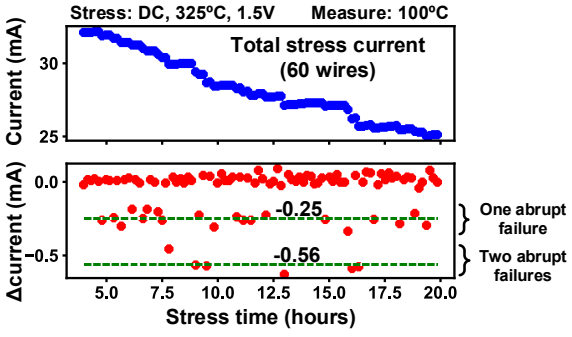

Fig. 11. (Above) Total stress current versus stress time. (Below) The change in the stress current in each 10 minutes stress interval indicating the number of EM failures and the stress current of each DUT.

Fig. 11 describes the method we used to measure the DC stress current of an individual DUT. During stress, all peripheral circuits including the scan chain, stress clock generator, and local stress drivers are powered on. Since the stress current and leakage current share the same I/O pad, it is not possible to measure the stress current portion only. However, when monitoring the total stress current, we can clearly see the sudden current drops shown in Fig. 11 (below). These drops indicate the number of abrupt failures occurring in each stress interval (= 0, 1, or 2) as well as the stress current in each broken wire. We did not observe more than two wires break in a 10 minute stress interval. During the short 10 minutes stress interval, the stress current change due to progressive failure can be ignored. So we can measure the stress current of each wire by measuring the current drop in each stress interval. Based on the data, we found that the average stress current through a single DUT is 0.25 mA for a 1.5 V, 325 °C DC stress condition.

B. Square and Real AC Stress Results

Although the on-chip voltage controlled oscillator can generate a stress frequency much higher than 1 GHz, the stress drivers may not be able to switch wire signals at such high frequencies due to RC parasitics. To ensure that our EM results are representative, we first determined the highest stress frequency at which the wire signals will switch reliably. Since the dynamic power of a circuit is proportional to $C*VDD^2*f$, the power consumption is expected to increase with frequency. However, as shown in Fig. 12, the current started to drop beyond 900 MHz. This can be attributed to the reduced signal swing at such high frequencies. That is, the wire signal is no longer a square wave but becomes a sinusoidal wave. Based on this simple experiment, we chose 900 MHz as the maximum stress frequency.

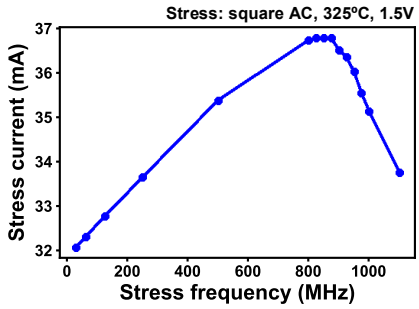

Fig. 12. Total stress current versus stress frequency for square AC stress. Stress current decreases beyond 900 MHz due to signal swing degradation so we chose 900 MHz as the maximum stress frequency.

AC stress is known to have minimal impact on EM. This is because any atom movement caused by the forward current will be cancelled out by the backward current. However, previous results were based on low stress frequencies, so further studies are needed to fully understand EM effects at high frequencies. Fig. 13 shows resistance traces of 60 wires subject to square AC and real AC stress at 900 MHz. No appreciable resistance shift was measured over the 52.7 hours stress period. Although the resistance didn't change under AC stress current, other underlying characteristics such as the metal grain structure, vacancy density and mechanical

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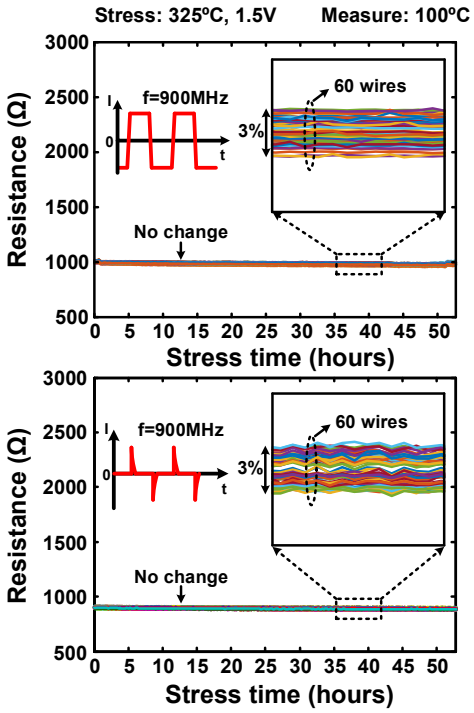

Fig. 13. Resistance traces under square AC and real AC stress modes at 900 MHz.

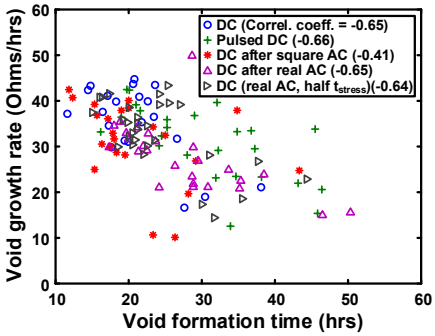

Fig. 14. Correlation between void formation time and void growth rate for progressive failures.

stress distribution may have been affected, which cannot be picked up by simple resistance measurements. To uncover subtle effects of AC stress, we measured the DC stress lifetime after a AC pre-stress and compare the results with DC stress on fresh wires [2]. The test chip was placed under AC stress mode for 52.7 hours and then switched to DC stress mode. Wires were subject to either a square AC current or a real AC current. If the AC pre-stress had any effect on the underlying wire structure, it should show up as difference in the DC EM lifetime. Five specific AC pre-stress conditions were used in our experiment: 52.7 hours 200 MHz square AC, 52.7 hours 900 MHz square AC, 52.7 hours 200 MHz real AC, 52.7 hours 900 MHz real AC and 26.4 hours 900 MHz real AC.

C. Pre AC + DC Stress Results: Failure Types

The three failure types occurred in all stress modes, but with different ratios as denoted in Fig. 16. The number of progressive failures under different stress mode are more or less similar, ranging from 21 to 31, meaning that progressive failure is not strongly influenced by AC stress. However, significantly more type 2 abrupt failures occurred under pulsed DC and square AC + DC stress modes, compared to DC and real AC + DC modes. For 200 MHz pulsed DC, 200 MHz square AC + DC, and 900 MHz square AC + DC stress modes, the number of type 2 abrupt failures were 20, 6, and 17, respectively. While for DC, 200 MHz real AC + DC, 900 MHz real AC + DC and 900 MHz real AC (half pre-AC stress time) + DC, the numbers were 2, 1, 2, and 4. These results suggest that pulsed DC stress and square AC + DC stress modes may have altered some aspects of the wire structure, such as metal grain, vacancy density and mechanical stress, thereby turning some type 1 abrupt failures into type 2 abrupt failures.

D. Pre AC + DC Stress Results: Progressive Failure

As illustrated earlier in Fig. 9 (below), for progressive failures, there are two parameters of interest: void formation time and void growth rate. Fig. 14 shows the correlation between void formation time and void growth rate for different AC and DC stress modes. The pulsed DC void formation time is scaled by 0.5 for a more meaningful comparison. The figure shows a negative correlation between void formation time and void growth rate. That is, a wire with a longer void formation time tends to have a slower void growth rate, and vice versa. The correlation coefficients of each stress mode ranges from –0.66 to –0.41.

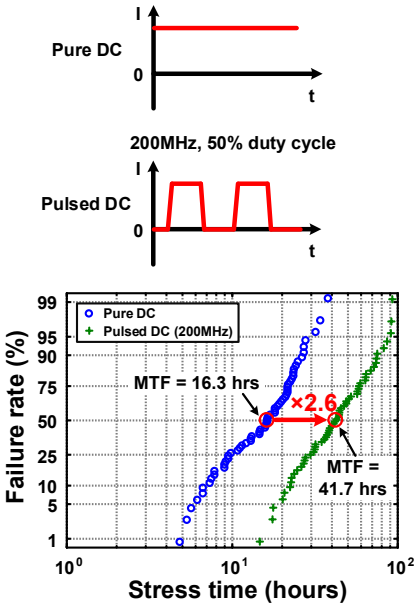

Fig. 15. Failure time comparison between DC and pulsed DC.

IV. TIME TO FAILURE DISTRIBUTION RESULTS

In this section, we compare the failure time distributions measured under different stress modes.

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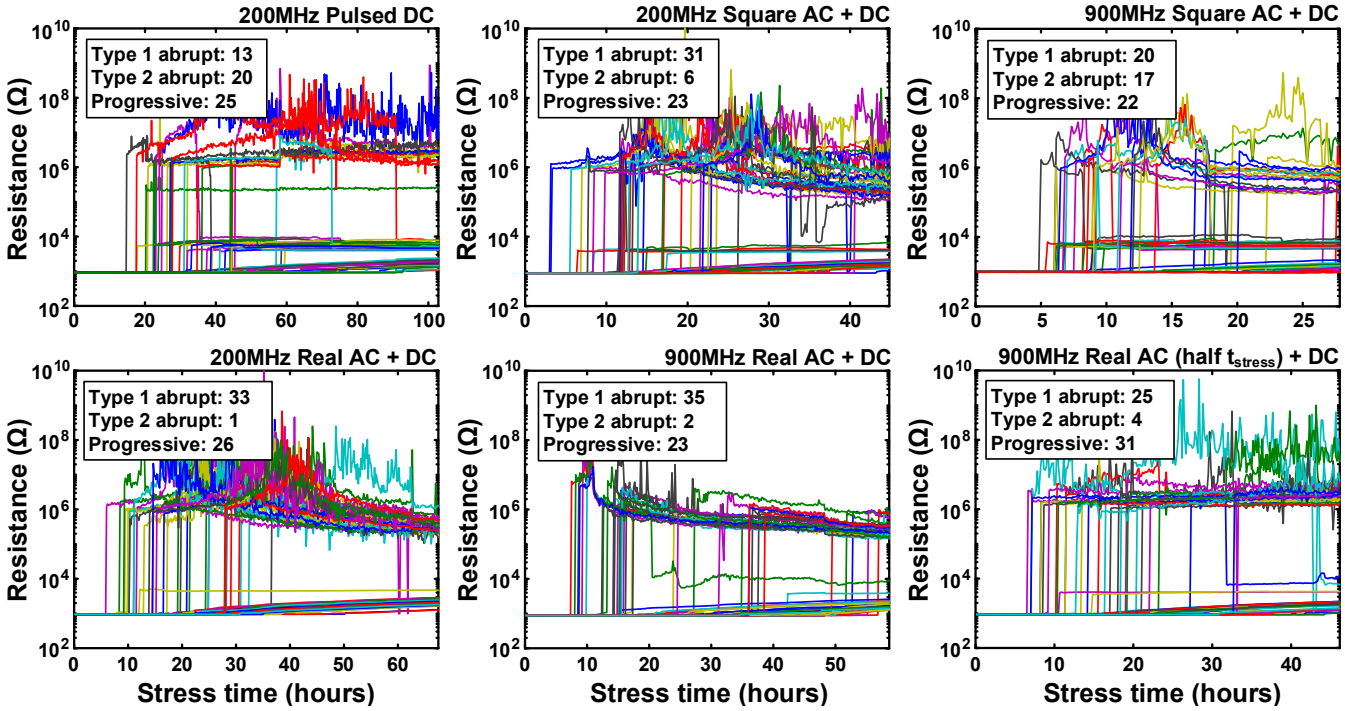

Fig. 16. Resistance traces and failure type ratios under various stress modes.

A. Comparison between Different Stress Modes

Fig. 15 shows the comparison between pure DC and pulsed DC results. Originally, we were expecting the pulsed DC to have a mean time-to-failure (MTF) close to 2 times that of pure DC owing to the 50% duty cycle. However, measured data shows an MTF ratio of 2.6. We suspect the higher than expected ratio is due to the lower Joule heating and/or mechanical backstress exerted during current off periods.

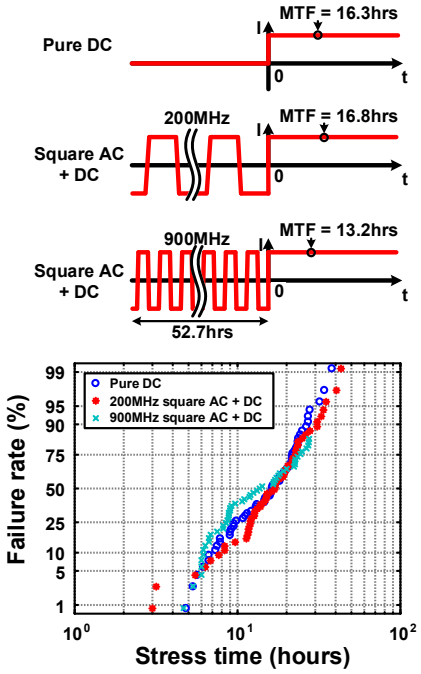

Fig. 17. Failure time comparison between DC and square AC + DC.

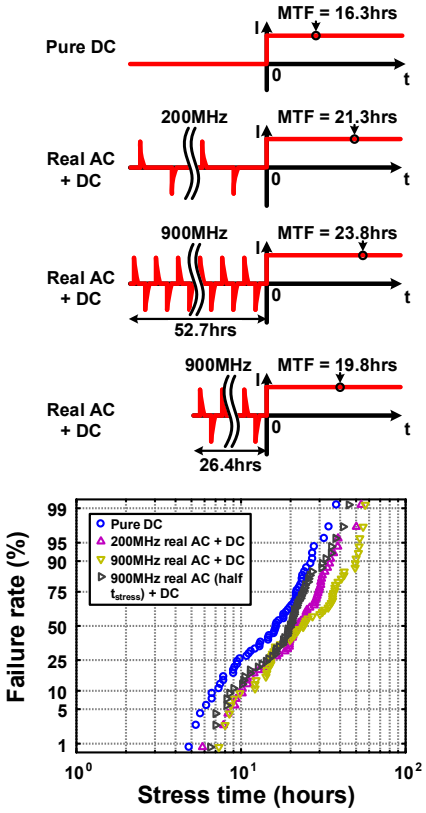

Fig. 18. Failure time comparison between DC and real AC + DC.

Fig. 17 compares pure DC versus DC after square AC. Two chips were pre-stressed at 200 MHz and 900 MHz, respectively, for 52.7 hours. As seen in the figure, we did not observe any noticeable difference in their failure time distributions

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which suggests that square AC has minimal impact on the failure time characteristics.

Fig. 18 shows pure DC versus three real AC pre-stress results: 52.7 hours 200 MHz, 52.7 hours 900 MHz and 26.4 hours 900 MHz. The MTFs were 16.3 hours, 21.3 hours, 23.8 hours and 19.8 hours, respectively. To our surprise, EM lifetime consistently improved for the DUTs exposed to real AC stress before pure DC stress. A longer AC stress time improved the lifetime further, while changing the stress frequency did not have much impact on the failure time distribution. Two possible reasons for this counter-intuitive behavior are given in the next section.

B. Two Possible Reasons for Lifetime Improvement after Real AC Stress

Possible reason #1: The unexpected lifetime improvement after real AC stress can be attributed to unbalanced current peaks, as explained in Fig. 19. The forward charging and backward discharging current peaks could be different even with careful sizing. If the discharging current peak is higher than the charging one, then the DUT wire undergoes stress in the opposite direction before DC stress is applied. This scenario will result in longer lifetime as the DC stress will first have to "undo" the stress occurred during the real AC stress period. Square AC on the other hand doesn't have any systematic difference in the forward and backward current peaks as one PMOS and one NMOS (in opposite ends of the wire) are activated irrespective of the current direction. Although process variation could introduce forward and backward currents mismatch in square AC current, its effect should be small due to two reasons: (a) the driver transistor size is 10 times of the minimum size, resulting relatively less mismatch; (b) we report the shift in average time-to-failure so process variation effects are averaged out.

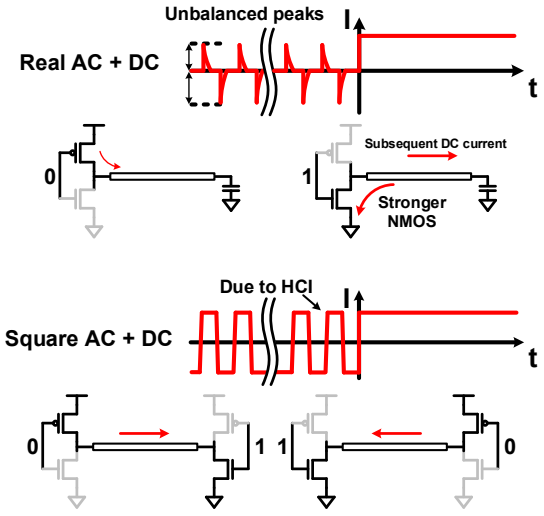

Fig. 19. Mismatch in forward and backward peak currents during real AC stress may result in a longer lifetime in subsequent DC stress.

Possible reason #2: Transistor aging might be responsible for the unexpected lifetime improvement. For our circuit based EM test structure, transistor aging will affect the EM lifetime as the stress current may degrade with time. That is, threshold voltage of the stress drivers may degrade during AC pre-stress, resulting in a lower stress current after the real AC pre-stress period, as illustrated in Fig. 20. Note that we only observed a longer lifetime for the real AC pre-stress, and not for the square AC pre-stress. This can be explained by the difference in Bias Temperature Instability (BTI) induced degradation and Hot Carrier Injection (HCI) induced degradation between the two modes. As depicted in Fig. 20, BTI aging is more dominant in real AC than in square AC because the driver transistors see a larger voltage across the gate-to-source and gate-to-drain terminals in that stress mode. In this case, the stress current will degrade more after a real AC stress than after a square AC stress, resulting in an improved lifetime for the former. HCI is believed to be less significant in the 32 nm technology used in this study which suggests that transistors do not degrade appreciably during square AC stress. This explains why the distributions didn't shift after square AC stress in Fig. 17. It's worth pointing out that circuit based EM test structures capture the interplay between EM degradation and transistor degradation, which can provide a more realistic picture of the overall EM lifetime characteristics compared to traditional probing based methods.

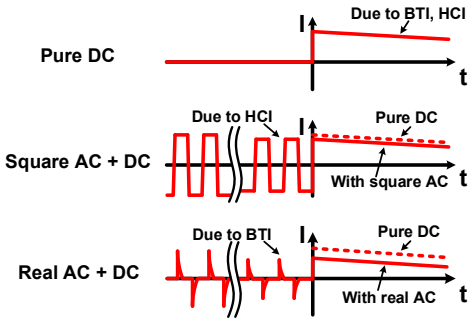

Fig. 20. Transistor aging during pre-stress may reduce the stress current in subsequent DC stress.

C. Time-to-Failure versus DUT location

Fig. 21 shows the MTF versus DUT location for various stress modes. MTF for pulsed DC is scaled by 0.5 for easier

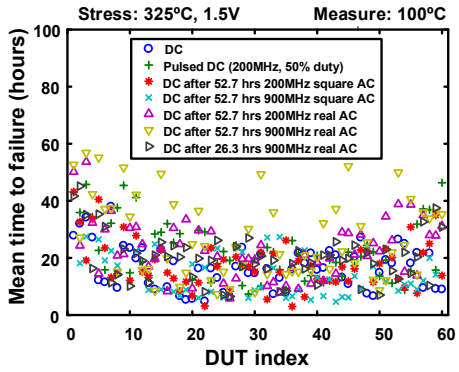

Fig. 21. MTF versus DUT location. DUTs located in the center of the heating area show a marginally shorter MFT. This can be attributed to a subtle temperature gradient within the heating area.

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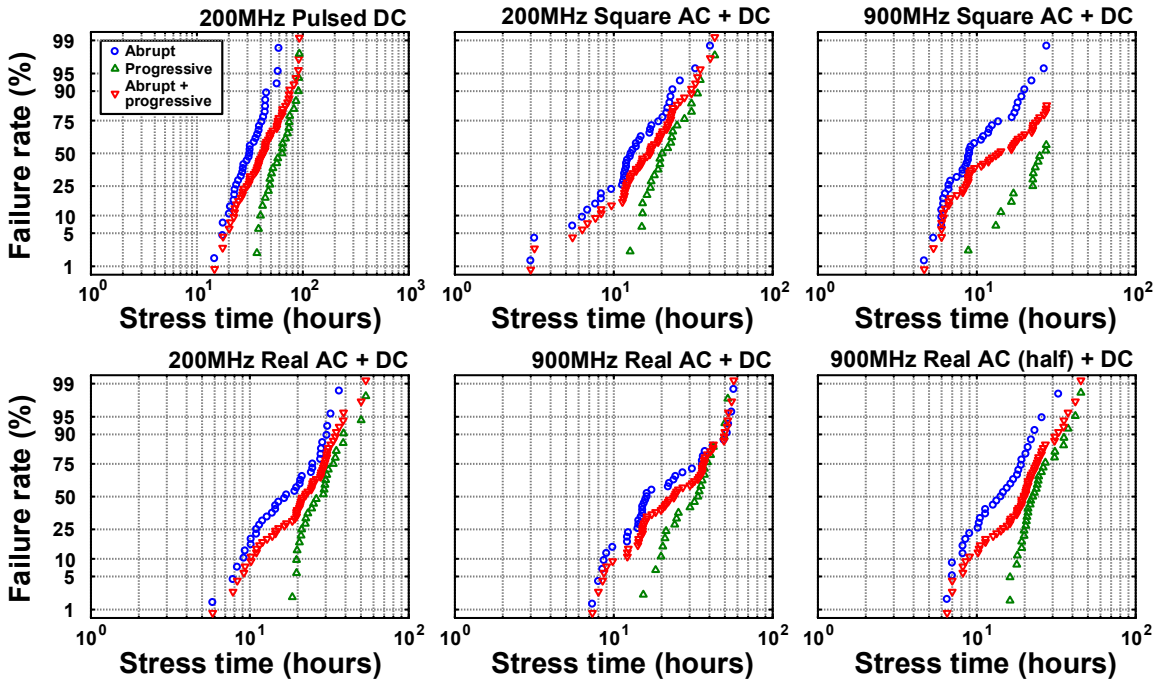

Fig. 22. Abrupt, progressive, and total failure distributions under various stress modes.

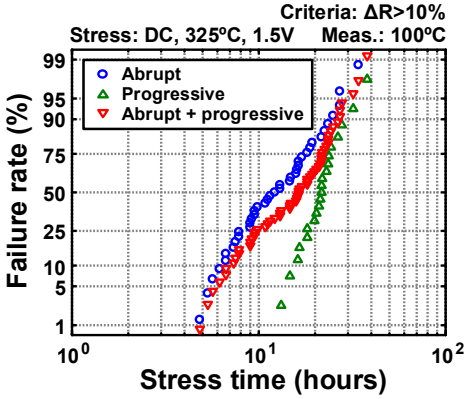

Fig. 23. Abrupt failure and progressive failure distributions for DC stress, along with the combined distribution. The individual distributions follow a lognormal distribution.

comparison. The data indicates that MTF is relatively uniform throughout the DUT array except for perhaps a few DUTs located on both sides of the array. This suggests that the DUT temperature is slightly lower towards the edge of the heating area. However, for the majority of DUTs, MTF was independent of the location. It's worth noting that the small temperature gradient on both sides cannot be avoided as the heat has to eventually travel from the heat source to the ambient.

D. Failure Time Distribution for Abrupt and Progressive Failures

In this section, we show the abrupt and progressive failure time distributions separately. Fig. 23 shows the distributions of abrupt, progressive, and total failures under normal DC stress. The individual distributions follow a lognormal distribution, resulting in a bimodal lognormal distribution for the combined failure distribution. Compared to progressive failures, abrupt failures occur earlier and have a smaller mean and larger sigma value. Since the chip lifetime is typically determined by the time-to-first failure, abrupt failures will ultimately limit the chip EM lifetime. Fig. 22 shows the abrupt failures and progressive failures for 6 different stress modes.

V. Conclusion

In this paper, we presented detailed AC and DC electromigration data from a 32 nm test chip. On-chip metal gate heaters were employed for temperature accelerated testing. Local stress drivers can stress 60 EM wires in parallel which enhances the test efficiency. Wire resistance was measured under various AC and DC stress modes with stress frequencies up to 900 MHz. Abrupt and progressive failures were observed, each following a lognormal distribution. DC EM data shows temporary revhealing and two distinct abrupt failure types. These behaviors can be explained by considering both electrical stress and mechanical stress profiles. Although AC stress alone did not cause any noticeable resistance change, data suggests that AC stress affects the wire's underlying EM characteristics. This was confirmed by measuring the DC EM lifetime with and without applying an AC pre-stress. Counter-intuitively, the lifetime improved after applying a real AC stress. This can be explained by two hypotheses: transistor aging and unbalanced forward and backward peak currents.

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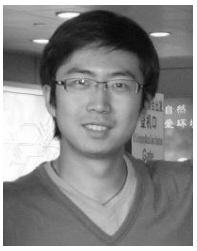

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