A Multi-phase VCO Quantizer based Adaptive Digital LDO in 65nm CMOS Technology

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Presentation Outline

• Analog vs. digital Low DropOut (LDO) regulators
• Digital LDO examples
• Proposed VCO-based digital LDO
• Stability analysis
• 65nm simulation results
• Conclusion
Integrated Voltage Regulators

- On-chip distributed voltage regulators
- Wide operating conditions with fast transients

22nm Intel Haswell processor
N. Kurd, et al., ISSCC, 2014

22nm IBM POWER8 processor
Z. Toprak-Deniz, et al., ISSCC, 2014

<1% area overhead
Analog vs. Digital LDO

- Digital LDOs:
  - Good scalability with technology
  - Low voltage operation
  - Loop parameters can be controlled digitally

*Ref: S. Gangopadhyay, JSSC’14*
Digital LDO Examples

1-bit ADC

- Simple design
- Requires many clock cycles to settle
- Slow response

Y. Okuma, CICC’10

Multi-bit ADC

- Complex design
- Requires fewer clock cycles
- Fast response

T-J Oh, TVLSI’14
Digital LDO Examples

- Multi-bit ADC based distributed digital LDO
- Shared voltage regulator controller (VREGC) and distributed micro-regulators (UREGs)
- VREGC utilizes a 3-bit flash ADC
Motivation of This Work

• Trade-off between response time and efficiency
  o Higher sampling clock provides faster settling
  o Lower sampling clock improves efficiency

  Adaptive sampling clock frequency

• High resolution ADC solutions
  o Higher ADC resolution provides settling in fewer clock cycles
  o Increasing ADC resolution requires more power and area

  VCO based digital intensive ADC
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Proposed VCO-based Digital LDO

- VCO based quantizer provides multi bit resolution
- Droop/overshoot detector generates adaptive sampling clock ($C_{K_s}$)

![Diagram of Proposed VCO-based Digital LDO]

- $V_{REF}$
- Multi-ph Time Quant.
- $V_{IN}$
- $V_{OUT}$
- $I_{LOAD}$
- $C_L$
Multi-phase VCO-based Quantizer

- Multiple VCO phases are utilized to increase resolution
- VCO phase quantization provides 1\textsuperscript{st} order quantization noise shaping
Adaptive Sampling Clock Generator

- Droop/overshoot detector detects sudden change in load current by observing $V_{OUT}$
- VCO high frequency mode is activated to reduce ripple and faster recovery
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Discrete-time Small Signal Model

• Two poles in the system due to digital integrator and output load

Ref: S. B. Nasir, TPE, 2016
Root Locus and Stability

- Higher sampling clock frequency, lighter load moves $z_{p2}$ towards unity circle
- Proposed LDO is stable for $I_{\text{LOAD}} > 3.2\text{mA}$

Ref: S. B. Nasir, TPE, 2016
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Transient Step Response

\[ C_L = 40 \text{pF}, \ V_{\text{IN}} = 1, \ V_{\text{OUT}} = 0.9 \text{V}, \ 65\text{nm CMOS} \]
Baseline Digital LDO

- Single phase VCO quantizer with fixed sampling frequency
- Baseline design is used for performance comparison
**Transient Step Response**

\[ C_L=40\text{pF}, \ V_{\text{IN}}=1, \ V_{\text{OUT}}=0.9\text{V}, \ 65\text{nm CMOS} \]

- Multi-phase VCO quantization error during steady state is only 0.5mV
Adaptive sampling reduces voltage droop by 40 – 60% and 3.5 – 6.5 times faster settling.
• **Maximum current efficiency 99.3% and power efficiency 92.8%**

• **Total quiescent current:** 660µA (VCOs: 530µA, Switching: 110µA and droop/overshoot detector: 20µA)

• **Overhead of droop/overshoot detector is negligible**
## Performance Comparison

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<thead>
<tr>
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<tbody>
<tr>
<td><strong>Technology</strong></td>
<td>65nm</td>
<td>180nm</td>
<td>130nm</td>
<td>110nm</td>
</tr>
<tr>
<td><strong>ADC type</strong></td>
<td>Multi-bit VCO</td>
<td>Multi-bit SAR</td>
<td>1-bit Comp.</td>
<td>Multi-bit VTC+TDC</td>
</tr>
<tr>
<td><strong>$V_{IN}$ range (V)</strong></td>
<td>0.6 – 1.2</td>
<td>0.9 – 1.8</td>
<td>0.5 – 1.2</td>
<td>0.6 – 1.2</td>
</tr>
<tr>
<td><strong>$V_{OUT}$ range (V)</strong></td>
<td>0.5 – 1.15</td>
<td>0.8 – 1.5</td>
<td>0.45 – 1.14</td>
<td>0.5 – 0.9</td>
</tr>
<tr>
<td><strong>$I_{LOAD}$ (mA)</strong></td>
<td>10 – 100*</td>
<td>1 – 200</td>
<td>0.5 – 4.6</td>
<td>80</td>
</tr>
<tr>
<td><strong>$I_{Q}$ (µA)</strong></td>
<td>660*</td>
<td>750</td>
<td>78</td>
<td>32</td>
</tr>
<tr>
<td><strong>Max. Current Efficiency (%)</strong></td>
<td>99.3*</td>
<td>99.6</td>
<td>98.3</td>
<td>99.98</td>
</tr>
<tr>
<td><strong>$C_{L}$ (nF)</strong></td>
<td>0.04</td>
<td>1000</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td><strong>Steady-state $f_s$ (MHz)</strong></td>
<td>8.4*</td>
<td>5</td>
<td>25</td>
<td>1</td>
</tr>
<tr>
<td><strong>$\Delta V_{OUT}$ (mV)</strong></td>
<td>50**</td>
<td>70</td>
<td>40</td>
<td>53</td>
</tr>
<tr>
<td><strong>Settling Time (µs)</strong></td>
<td>0.7**</td>
<td>2</td>
<td>1.1</td>
<td>38</td>
</tr>
<tr>
<td><strong>FOM&lt;sup&gt;#&lt;/sup&gt; (ps)</strong></td>
<td>0.53**</td>
<td>5250</td>
<td>76.5</td>
<td>0.26</td>
</tr>
</tbody>
</table>

<sup>€</sup>Schematic Simulation results

<sup>*</sup>At $V_{IN}$=1V and $V_{OUT}$=0.9V

<sup>**</sup>$I_{LOAD}$ step from 30-80mA in 1µs
Conclusion

- Multi-phase VCO quantizer based ADC operating over wide range of load current and input/output voltage in 65nm CMOS technology

- Dynamically adaptive sampling clock depending on the load transients reduces the output voltage ripple and provides faster settling

- Schematic simulations show a maximum current efficiency of 99.3% and an FOM of 0.53ps