A Multi-phase VCO Quantizer based Adaptive Digital LDO in 65nm CMOS Technology

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***Abstract*—A digital low-dropout (DLDO) voltage regulator circuit is proposed utilizing a multi-phase VCO based time quantizer. This high-resolution quantizer requires much lower sampling clock frequency compared to the previously proposed 1-bit comparator based architectures and thereby ensures stability over a wide operating condition, while reducing the dynamic power consumption at the same time. The DLDO operates at an input voltage range of 0.6V to 1.2V and delivers a maximum 115mA current with a 50mV dropout, simulated in a 65nm LP CMOS technology. A dynamically adaptive sampling clock can reduce the output voltage droop by 40 – 60% and provides 3.5 – 6.5 times faster settling compared to a baseline DLDO design that uses a fixed sampling clock frequency. The FOM calculated at 0.9V output is 0.53ps. The maximum current efficiency is 99.3%.**

Keywords—digital low dropout regulator; adaptive sampling; voltage-controlled oscillator; time-based quantizer;

I. INTRODUCTION

Modern multi-core systems and system-on-chips require multiple voltage domains to improve the energy efficiency by spatially adjusting the supply voltage. The efficiency is further optimized by the technique known as dynamic voltage and frequency scaling (DVFS) that controls the supply voltage of each domain depending on its workload. However, all these power delivery constraints impose several challenges in the design of integrated voltage regulators. Switching regulators have high power efficiency, but suffer from the overhead associated with their design, such as, low quality factor and large area of the on-chip inductor based implementation and low power density of switched capacitor based implementation [1]. On the contrary, the linear low dropout (LDO) regulators are simpler to design, although efficiency degrades with increasing dropout voltage. Traditional analog LDO achieves fast transient response and good ripple immunity, but the performance severely degrades at lower input voltages, which is essential for power optimization. This makes the design of the error amplifier in the analog LDO very difficult while ensuring loop stability and high bandwidth at the same time over a wide variation in the load current. As a result, the implementation of digital LDO (DLDO) [2] – [6] is drawing significant attention for its process scalability, immunity to PVT variations and flexibility to adjust the loop parameters for design optimization. A DLDO, as shown in Fig. 1, replaces the error amplifier with an analog-to-digital converter (ADC) followed by a digital accumulator that adjusts the number of switches to be turned on in the output stage for a desired output

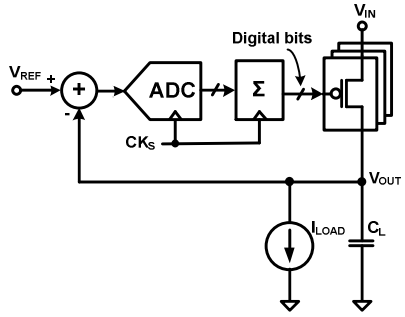

Fig.1. Simplified block diagram of a DLDO.

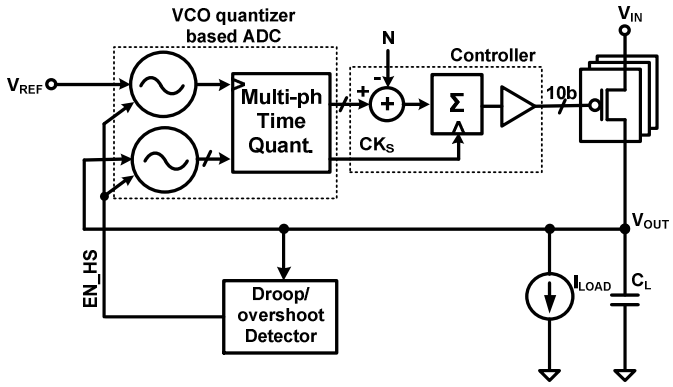

Fig.2. Proposed multi-phase VCO quantizer based DLDO block diagram.

voltage (V_{OUT}) and load current (I_{LOAD}). The frequency (f_S) of the sampling clock (CK_S) decides the loop transient response. Although higher f_S is good for faster response, but at the cost of higher dynamic power consumption and lower stability range. Section III discusses the stability issue in details. An architecture based on a simple comparator that acts as a 1-bit ADC and a shift register is widely used [2] – [4], due to its low quiesc ent current (I_Q). But binary comparison takes several clock cycles to track the reference (V_{REF}), as the loop value is updated by a small fixed step at every clock. Increasing f_S is the only solution for faster transient response. However, the maximum value of f_S is directly dependent on the frequency of the output pole for system stability [3]. Furthermore, higher f_S increases the dynamic power consumption. As a result, DLDO design using multi-bit ADC is proposed in [5] and [6] for faster loop response through the direct measurement of the error voltage (i.e. $V_{OUT} - V_{REF}$). [5] uses a SAR type ADC and DAC to drive a single power transistor in the output stage. This increases the circuit complexity and I_Q. [6] relies on a half-rate saw-tooth generation circuits for voltage-to-time conversion

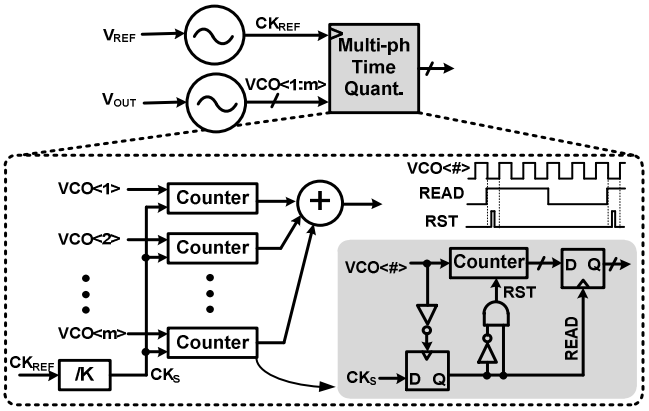

Fig.3. Multi-phase VCO based quantizer schematic.

(VTC) which is sensitive to circuit parasites and leakage. Both [5] and [6] have used many analog components and therefore, are not able to fully utilize the benefits of digital circuits.

In this paper, a digital intensive VCO quantizer based ADC is utilized to achieve high resolution quantization without relying on analog components. A pair of ring oscillator generates clock frequencies proportional to the input voltages and a digital counter performs quantization. Multiple phases of the ring oscillator improve the resolution further. Moreover, a detection circuit is incorporated to reduce the voltage ripples and settling time upon droop or overshoot occurrence, by increasing the ring oscillator frequency momentarily.

II. PROPOSED DLDO

Fig. 2 shows the block diagram of the proposed DLDO. A pair of ring oscillator converts the voltage inputs V_{REF} and V_{OUT} to equivalent clock signals of frequency f_{REF} and f_{OUT} respectively. Then they are quantized by the multi-phase quantizer that generates output count, $N_{OUT}=Nf_{OUT}/f_{REF}$. N is the quantizer output when $f_{OUT}=f_{REF}$ and can be controlled externally. The difference (i.e. N_{OUT} - N) is accumulated by a digital integrator to generate a 10-bit binary output that decides the number of PMOS (each 4µm/0.1µm) switch arrays to be turned on. Infinite dc gain of the integrator makes $V_{OUT}=V_{REF}$ in steady-state condition. The gain of the integrator (K_I) is easily adjusted for optimum performance. A droop/overshoot detector continuously monitors V_{OUT} and increases the loop operating speed for faster recovery when V_{OUT} crosses a given thresold limit above and below V_{REF}.

A. Multi-phase VCO Quantizer

The design of the multi-phase VCO based quantizer is illustrated in Fig. 3. The quantizer utilizes multiple phases of the VCO output (VCO<1:m>) to improve the resolution. Each VCO phase goes to a counter and all counter outputs are then added. Moreover, unlike conventional designs where the count values in two consecutive sampling periods are subtracted, in this design a short pulse (RST) resets the counter after reading the count (READ) in every sampling period. As the VCO is operating continuously, the quantization error generated in one sampling period is carried forward to the next period, providing 1st order noise shaping [7]. This technique eliminates the requirement of a register that stores the pervious count value and the subtractor. The sampling clock (CK_S) is generated by dividing the output of the reference clock (CK_{REF})

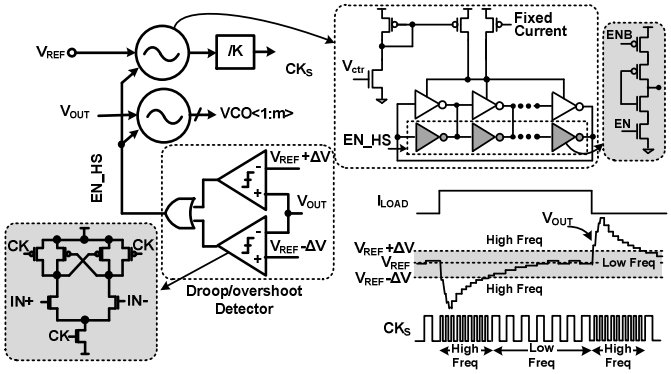

Fig.4. Droop and overshoot detection circuit for a dynamically adaptive sampling clock generation.

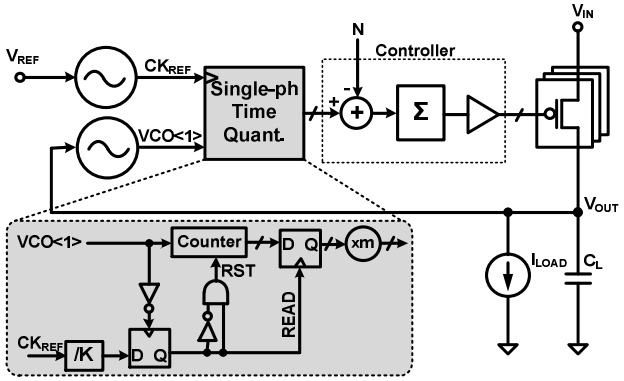

Fig.5 Baseline DLDO schematic.

that uses an identical VCO to make the quantizer insensitive to PVT variations. The frequency division factor (K) must be equal to N/m. Since the counter operates at the rising edges of the VCO, the READ and the RST operation occur at the falling edges to avoid meta-stability. This is achieved by resampling CK_S with the VCO falling edge. However, the RST operation must finish before the next VCO rising edge.

B. Dynamically Adaptive Sampling Clock Generation

A lower f_S saves dynamic power and improves the stability of the DLDO for a wide operating condition. However, it increases the output voltage ripple and settling time during load transients. In order to address this, a droop and overshoot detection circuit is introduced [3]. It compares V_{OUT} against a threshold (Δ) above and below V_{REF} to identify droop or overshoot occurrence and enables high frequency operation mode (i.e. EN_HS=1) of the VCOs when V_{OUT} goes above $V_{REF}+\Delta$ or falls below $V_{REF}-\Delta$. Since the quantizer generates code proportional to the ratio of f_{OUT} to f_{REF}, increasing both by the same factor doesn't alter the quantizer output. But the loop is updated at a much faster rate for quick recovery. When V_{OUT} reaches within the threshold, VCOs again go back to low frequency mode for better efficiency and stability. The operation is explained with a timing diagram in Fig. 4. The selection of Δ depends on the comparator input offset voltage.

C. Baseline DLDO

A baseline DLDO, as illustrated in Fig. 5, is designed to compare the benefits of the proposed techniques. The design uses a single-phase quantizer and the output is multiplied by the factor m to keep the loop dynamics identical to the proposed multi-phase design. Also, the droop/overshoot

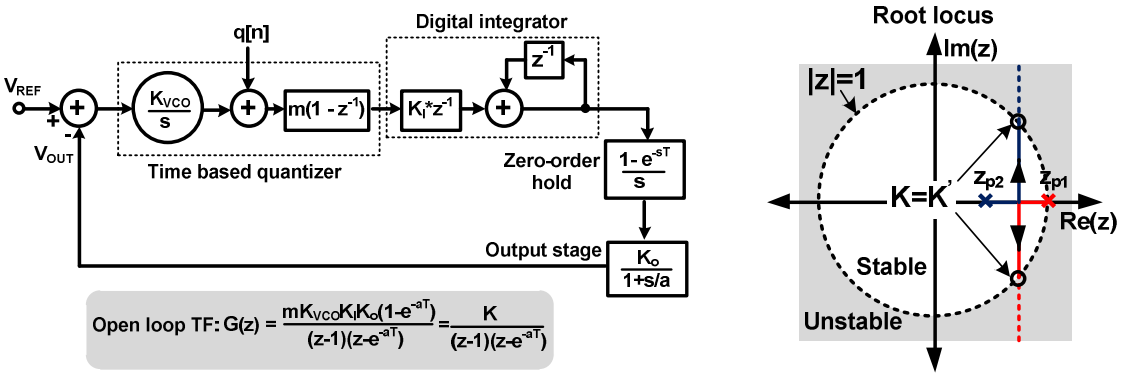

Fig.6. Small signal model of the DLDO and root locus plot for stability analysis.

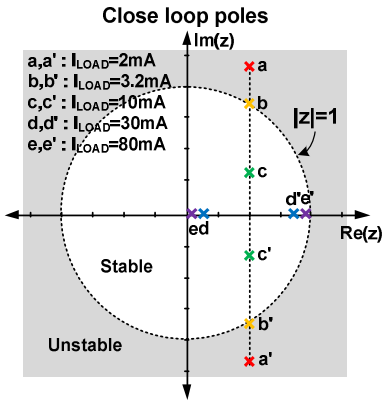

Fig.7. Close loop poles of the DLDO model for different load current. DLDO is stable for load current larger than 3.2mA.

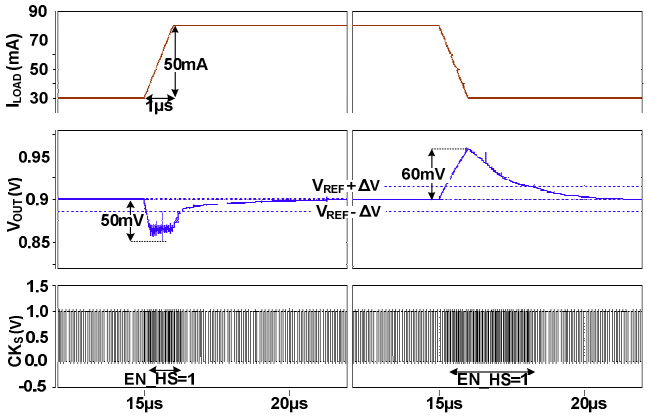

Fig.8. Simulated transient response with V_{IN}=1V, V_{OUT}=0.9V and load step from 30mA to 80mA in 1µs. Sampling clock frequency increases from 8.4MHz to 14.9MHz upon droop and overshoot detection.

detection circuit is removed and high-speed VCO mode is disabled (i.e. EN_HS=0) for the baseline design.

III. Stability Analysis

Fig. 6 shows the behavioral model of the DLDO. The VCO based quantizer is represented as a gain block of K_{VCO}/s for voltage to phase transformation, followed by the 1st order noise shaping multi-phase quantizer i.e. $m(1-z^{-1})$. K_{VCO} is the VCO voltage to frequency gain and m is the number of VCO phases. The VCO quantizer is followed by a 1st order digital integrator with gain K_I. Due to synchronous sampling in the quantizer, a z^{-1} delay is introduced before the integrator. Since the output of the digital integrator is held constant till the next clock edge, a zero order hold is placed at its output. The output stage that comprises PMOS switch-arrays and the output load, introduces a pole at frequency, $a \approx 1/R_P C_L$, where R_P is the effective resistance of the PMOS array and C_L is the load capacitance. $R_P = (V_{IN} - V_{REF})/I_{LOAD}$, is much lower than the effective load resistance. The dc gain of the output stage (K_O) is dependent on the load current and can be expressed as, $K_O = \Delta R_P I_{LOAD}$, where ΔR_P is the effective resistance change of the PMOS array for a 1LSB change at the integrator output. Therefore, open-loop z-domain transfer function is written as:

$$G(z) = \frac{mK_{VCO}K_IK_O(1-e^{-aT})}{(z-1)(z-e^{-aT})} = \frac{K}{(z-1)(z-e^{-aT})} \quad (1)$$

T is the time period of the sampling clock CK_S, and K is the dc loop gain, which is proportional to $1/I_{LOAD}$. G(z) has two poles: (1) z_{p1}=1 is on the unit circle and is due to the digital integrator, (2) $z_{p2}=e^{-aT}$ is from the output stage and is inside the unit circle. z_{p2} is a function of both the output pole (a) and the sampling

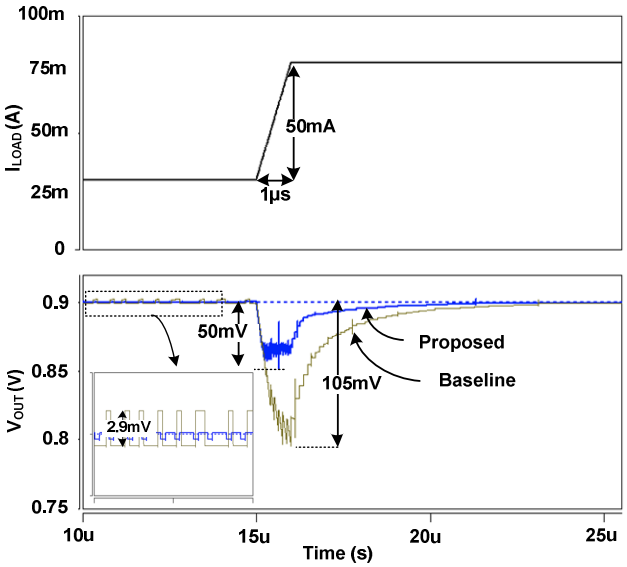

Fig.9. Transient simulations comparing the performance of the proposed DLDO with the baseline design. Steady state voltage ripple is reduced due to the higher resolution of the multi-phase quantization.

clock frequency (f_S=1/T). The root locus in Fig. 6 (right), as obtained by varying K, crosses the unit circle at K=K', making the DLDO stable for 0<K<K'. Increasing f_S moves z_{p2} towards z_{p1}, reducing the value of K' required for stability. The multi-bit quantizer based DLDO, due to its lower f_S requirement, provides better stability over a wide operating range, compared to a 1-bit comparator based architecture. This is the main

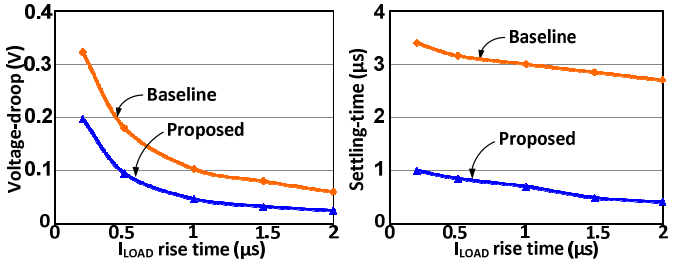

Fig.10. Simulated voltage droop and settling time for a load step from 30mA to 80mA with different rise time at V_{IN}=1V, V_{OUT}=0.9V.

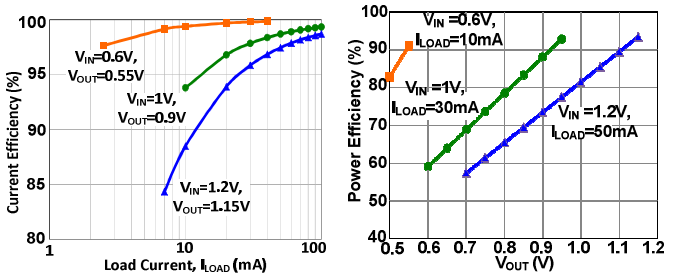

Fig.11. Current and power efficiency plot as calculated by sweeping I_{LOAD} and V_{OUT} respectively.

advantage of using a multi-bit quantizer. The closed loop pole locations are plotted in Fig. 7 by sweeping I_{LOAD} for V_{IN}=1V and V_{REF}=0.9V. The loop is stable for I_{LOAD} larger than 3.2mA for f_S=8.4MHz and K_I=1. Other loop parameters are used from circuit implementation. However, near minimum load current condition, since fewer numbers of PMOS switches are on, output voltage experience large change with the code. So minimum operating load current should be larger than 3.2mA.

IV. Simulation Results

The proposed DLDO isimplemented in 65nm CMOS technology and simulations are performed for a wide operating condition to verify the functionality. Fig. 8 shows the transient response when I_{LOAD} changes from 30mA to 80mA with a rise/fall time of 1µs. V_{IN} and V_{REF} are 1V and 0.9V respectively. During large load transient, when V_{OUT} goes above V_{REF}+15mV or below V_{REF}-15mV, VCO high-speed mode is enabled that enhances f_S from 8.4MHz to 14.9MHz for faster response, generating voltage droop and overshoot of 50mV and 60mV respectively. V_{OUT} transient response is then compared with the baseline design in Fig. 9, which shows 105mV droop for the same load transient. The 5-phase VCO quantizer generates only 0.5mV steady-state voltage ripple in comparison to 2.9mV in the case of a single-phase baseline design. Output voltage droop and settling time, as plotted in Fig. 10 for I_{LOAD} step from 30mA to 80mA with a varying rise time. Dynamically adaptive sampling speed in the proposed design reduces the voltage droop by 40% – 60% while achieving 3.5 – 6.5 times faster settling, compared to the baseline DLDO. Fig. 11 plots the simulated efficiency of the DLDO. Current efficiencies are plotted by sweeping I_{LOAD} for different V_{IN} and V_{OUT}. At V_{IN}=1V, V_{OUT}=0.9V, current efficiency increased from 93.8% to 99.3% when load current is varied from 10mA to 100mA. Total quiescent current consumption (I_Q) in this condition is 660µA (VCOs: 530µA, Switching: 110µA and droop/overshoot detector: 20µA). Current efficiency increases for lower operating voltages as I_Q reduces due to lower VCO and switching frequency. VCO frequency varies from 430MHz at V_{OUT}=0.5V to 880MHz at V_{OUT}=1.15V. Power efficiencies are also plotted as a function of V_{OUT} for different V_{IN} and I_{LOAD}. Power efficiency increases with V_{OUT} due to reduction in dropout voltages, achieving maximum of 92.8% for V_{IN}=1V. Table 1 compares the performance of the proposed DLDO with other state-of-the-art DLDO designs. The figure-of-merit (FOM) of speed calculated from [4] is 0.53ps.

TABLE I. Result Summery and Performance Comparison

	This Work€	TPE'13 [5]	ISSCC'15 [3]	TVLSI'15 [6]
Technology	65nm	180nm	130nm	110nm
ADC type	Multi-bit VCO	Multi-bit SAR	1-bit Comp.	Multi-bit VTC+TDC
V_{IN} range (V)	0.6 – 1.2	0.9 – 1.8	0.5 – 1.2	0.6 – 1.2
V_{OUT} range (V)	0.5 – 1.15	0.8 –1.5	0.45 –1.14	0.5 – 0.9
I_{LOAD}(mA)	10 –100*	1 –200	0.5 –4.6	80
I_Q (µA)	660*	750	78	32
Max. Current Efficiency (%)	99.3*	99.6	98.3	99.98
C_L (nF)	0.04	1000	1	1
Steady-state f_s (MHz)	8.4*	5	25	1
ΔV_{OUT} (mV)	50**	70	40	53
Settling Time (µs)	0.7**	2	1.1	38
FOM# (ps)	0.53**	5250	76.5	0.26

€ Simulation results
*At V_{IN}=1V and V_{OUT}=0.9V
#FOM=$C_L\Delta V_{OUT}I_Q/(\Delta I_{LOAD})^2$
**I_{LOAD} step from 30-80mA in 1µs

V. Conclusion

A digital intensive LDO architecture is presented in 65nm CMOS technology utilizing a multi-phase VCO quantizer based ADC operating across a wide range of load current and input/output voltages. A dynamically adaptive sampling clock depending on the load transients reduces the output voltage ripple and provides faster settling. A maximum current efficiency of 99.3% is observed for an output voltage of 0.9V and the FOM is only 0.53ps.

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