An Ultra-Dense Irradiation Test Structure with a NAND/NOR Readout Chain for Characterizing Soft Error Rates of 14nm Combinational Logic Circuits

S. Kumar, M. Cho*, L. Everson, H. Kim, Q. Tang, P. Mazanec, P. Meinerzhagen*, A. Malavasi*, D. Lake*, C. Tokunaga*, M. Khellah*, J. Tschanz*, S. Borkar*, V. De* and C. H. Kim

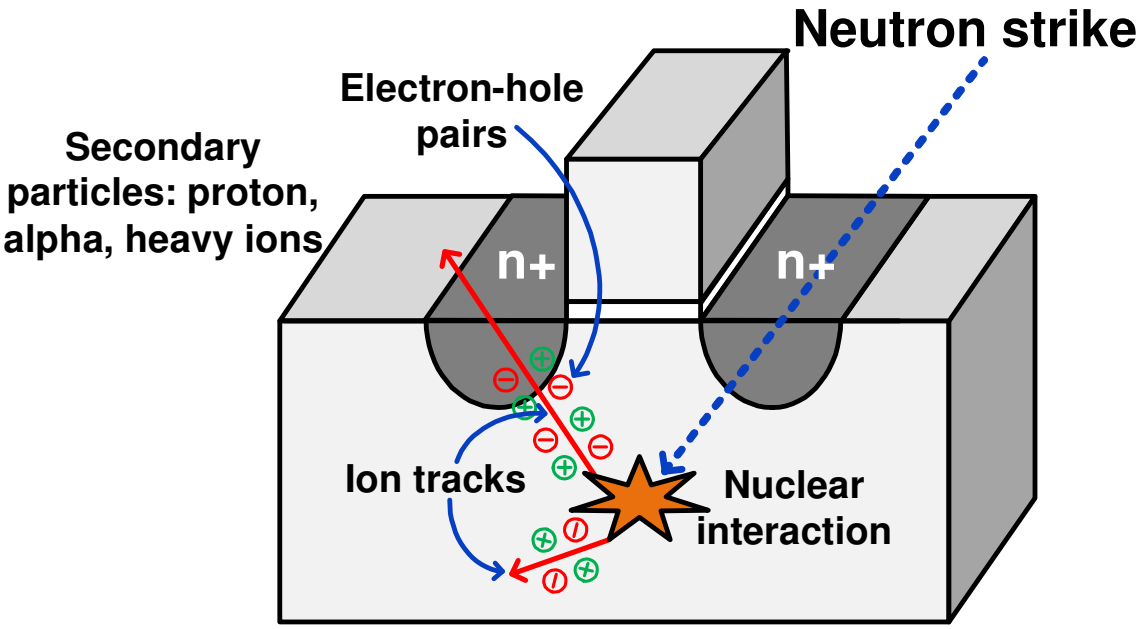
Dept. of ECE, University of Minnesota

*Circuit Research Lab, Intel Corporation

Outline of Presentation

- **Introduction**
- **Proposed ultra-dense logic soft error test circuit**
- **14nm test-chip and irradiation board design**
- **Neutron beam irradiation results**
- **Conclusion**

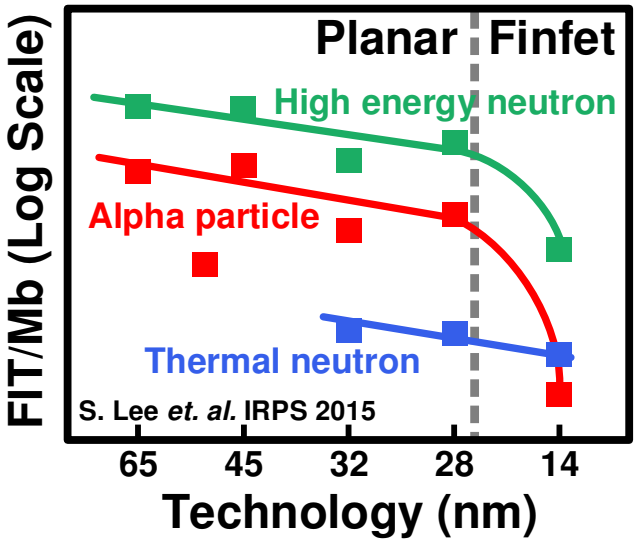
Radiation Effects in CMOS

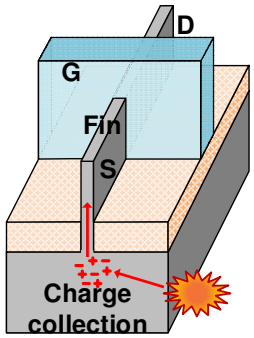


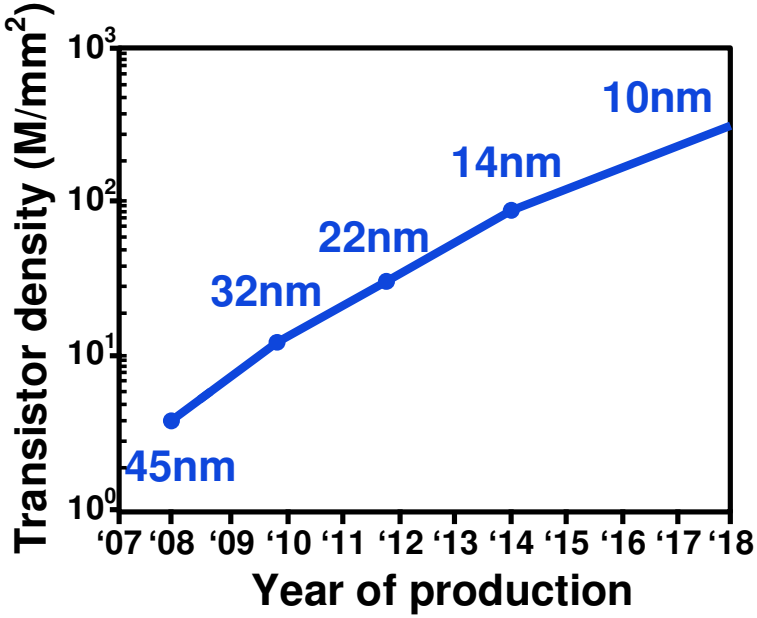
- **Neutron → secondary particles → electron-hole pairs → logic and memory soft errors**

FinFET Chip-Level SER

Per transistor SER ↓ × Device count per chip ↑

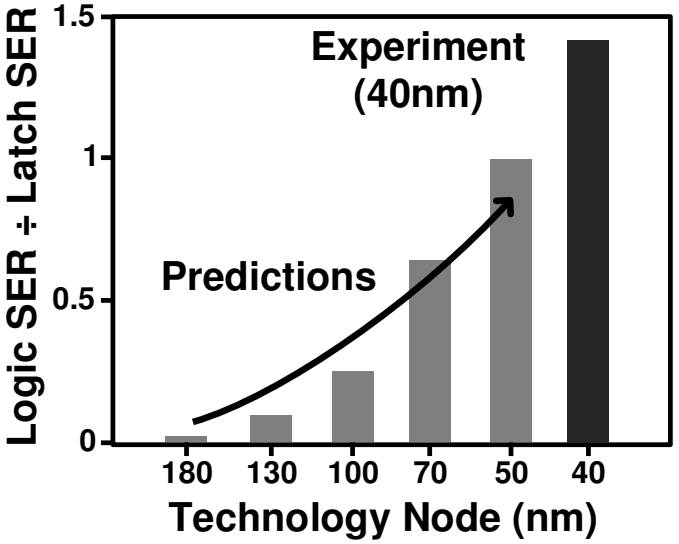




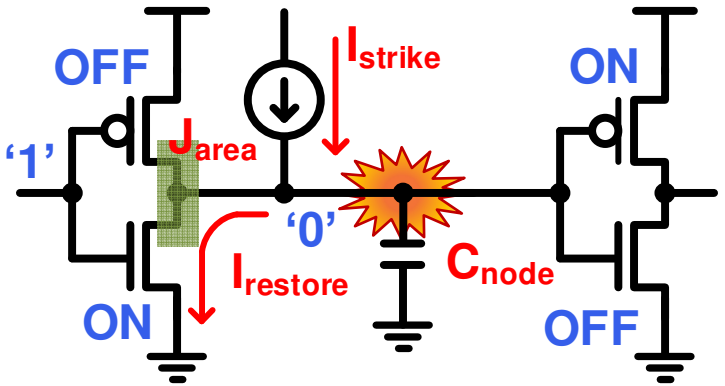


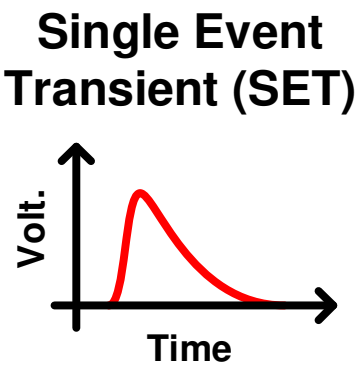
Combinational Logic SER

N. Mahatme, et al., TNS 2014



- With technology scaling, logic SER is expected to increase

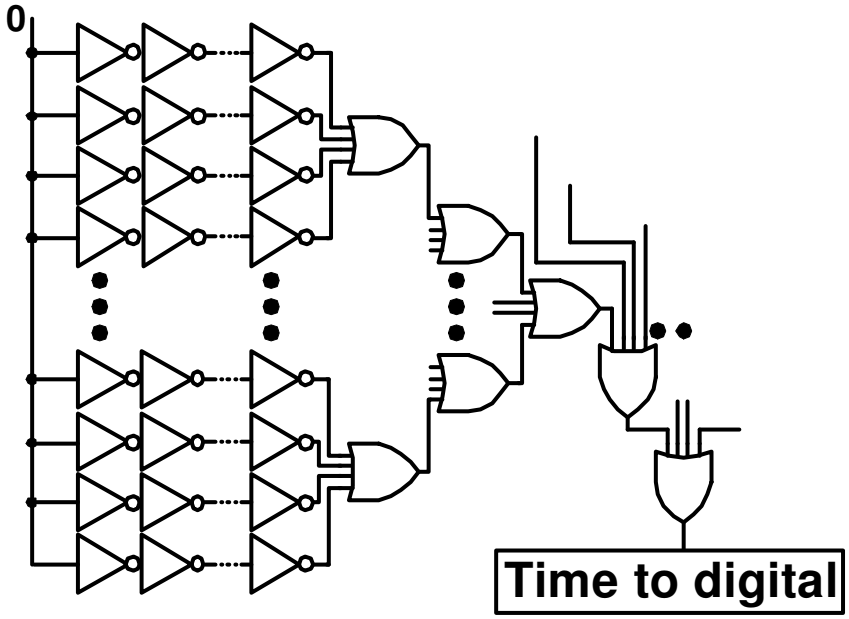




- Circuit parameters impacting SER: Restore current, junction area, node capacitance, logic chain length

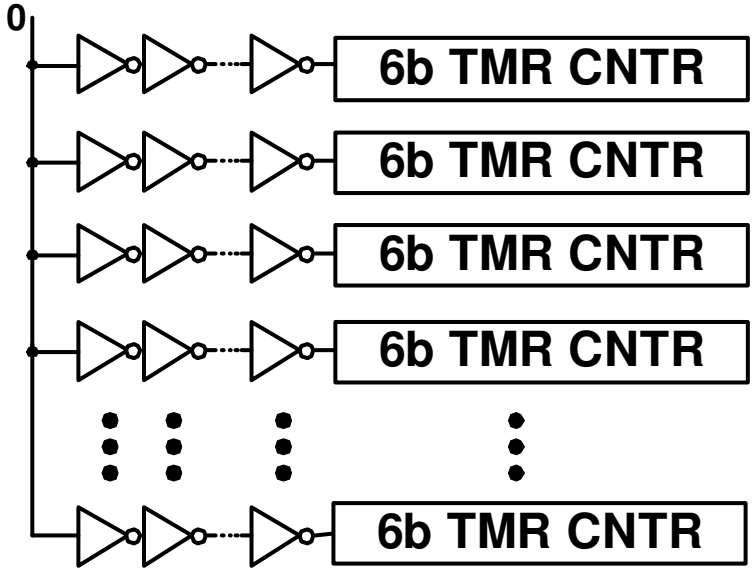
Previous SET Detection Circuits

T. D. Loveless *et. al.* TNS 2012



Tree structure: Irregular layout, measures both pulse width and count

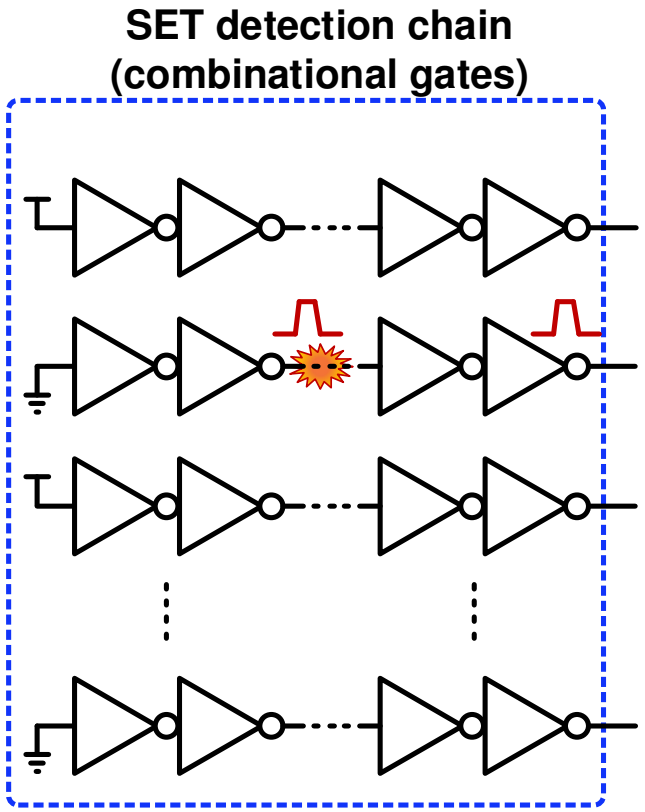
R. Pawlowski *et. al.* CICC 2014



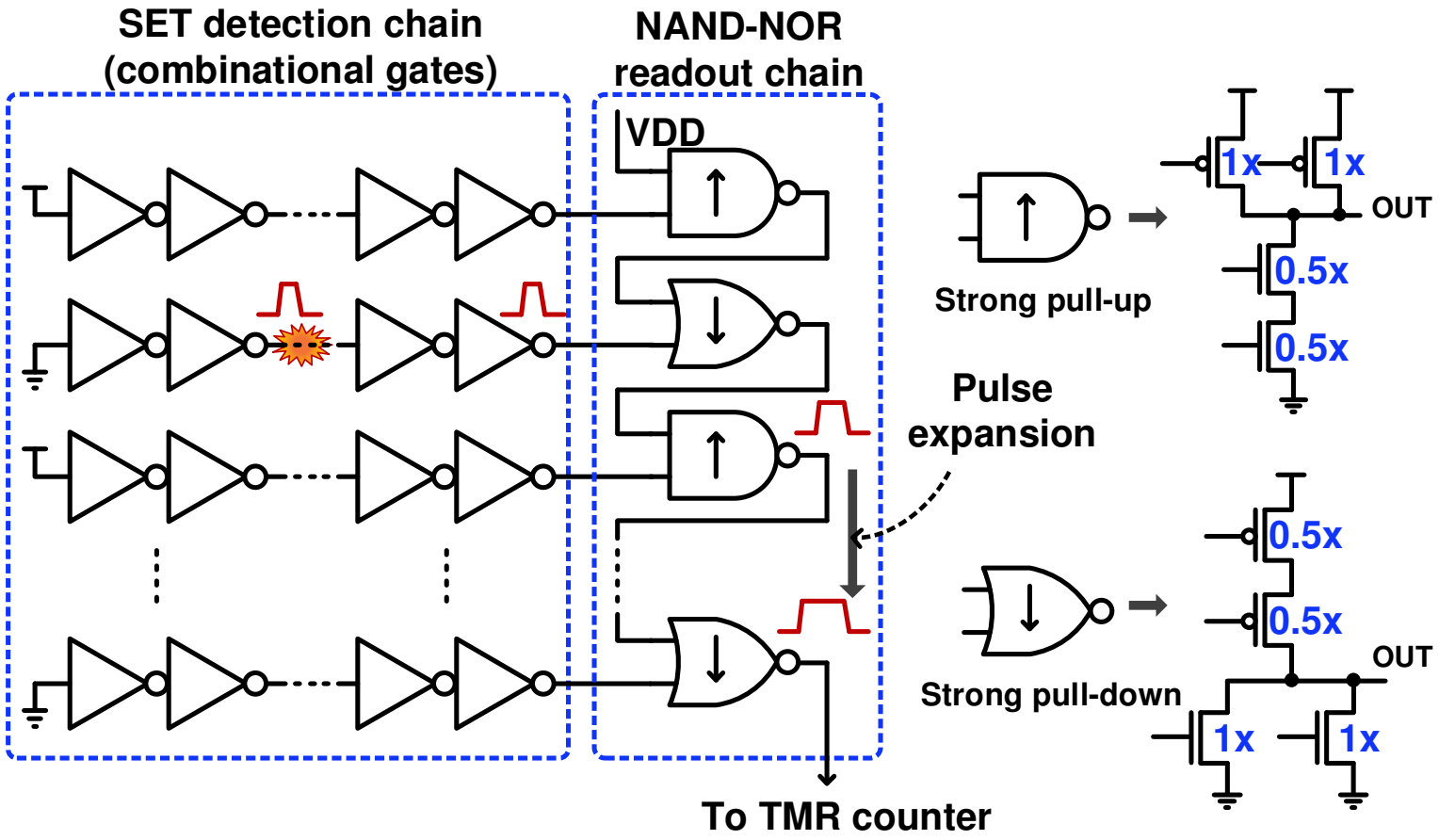
Parallel structure: large area overhead

SET: Single Event Transient
TMR: Triple Modular Redundancy

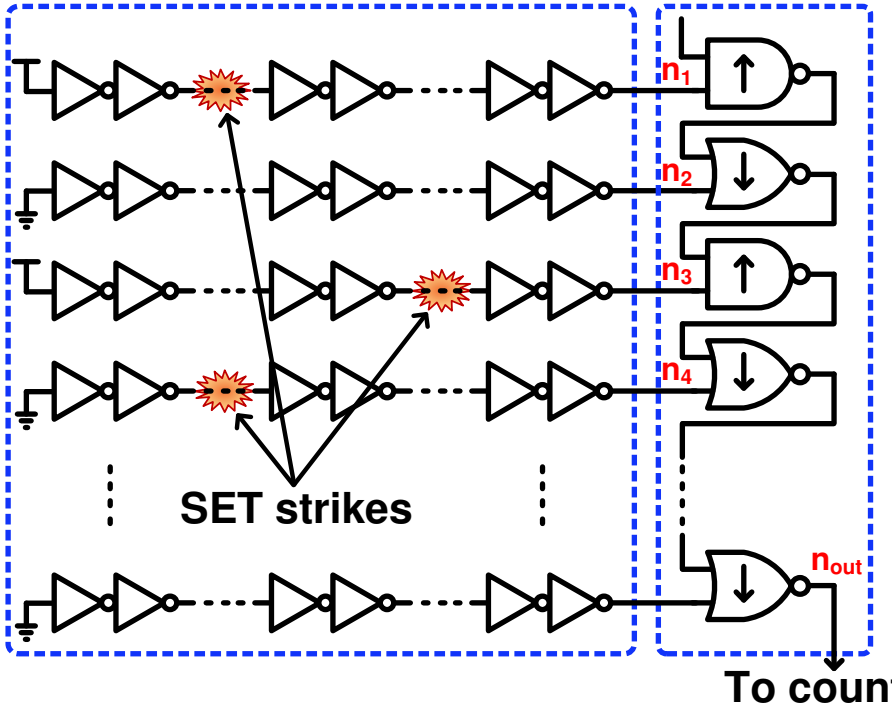
Proposed Irradiation Circuit

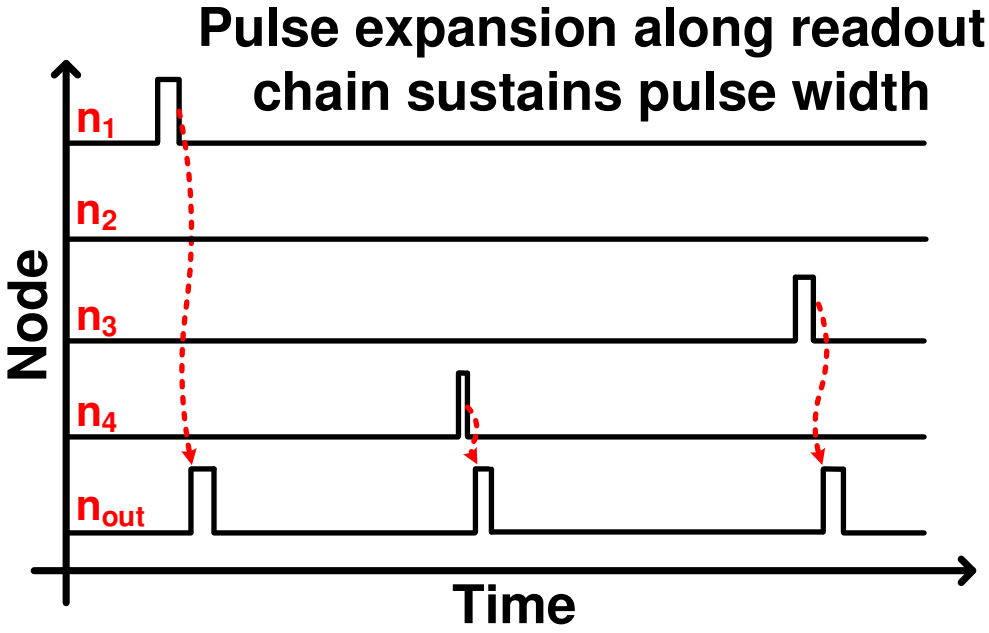


Proposed Irradiation Circuit



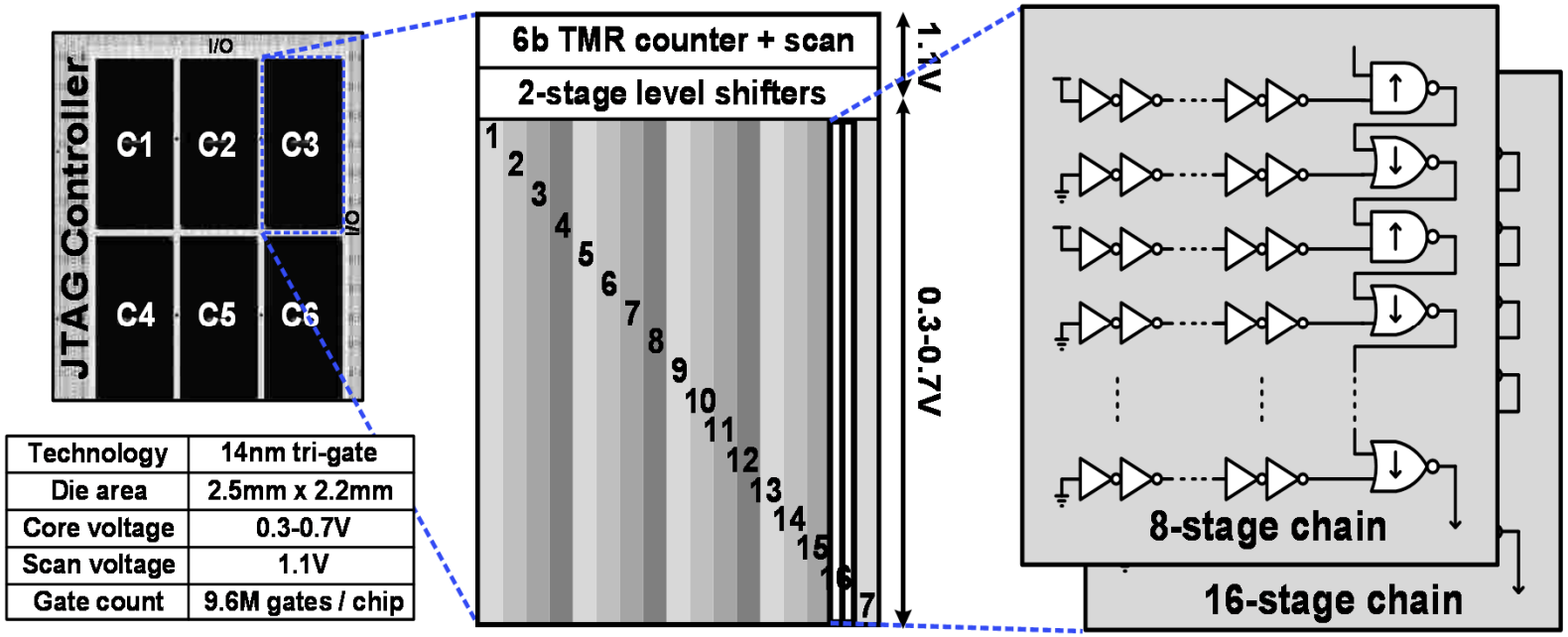
Proposed Irradiation Circuit





- **Sparse nature of SET events: Minimal overlap probability among SET pulses**

14nm Test-Chip Design

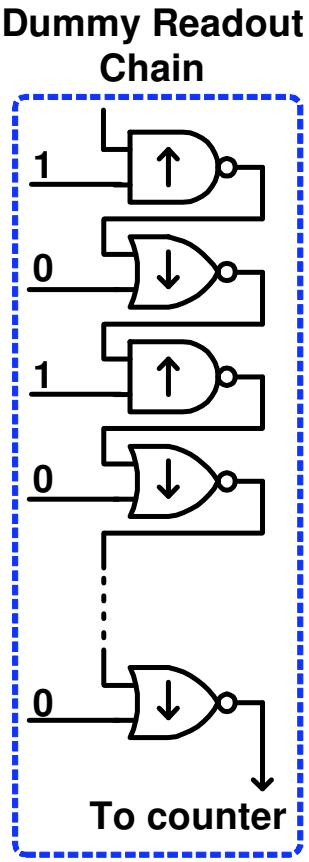


Technology	14nm tri-gate
Die area	2.5mm x 2.2mm
Core voltage	0.3-0.7V
Scan voltage	1.1V
Gate count	9.6M gates / chip

- TMR counters: Redundancy for soft error correction in counters
- Large scale implementation with 93% area utilization (1,975 rows)
- Pulse expansion: ensures all pulses reach the counter

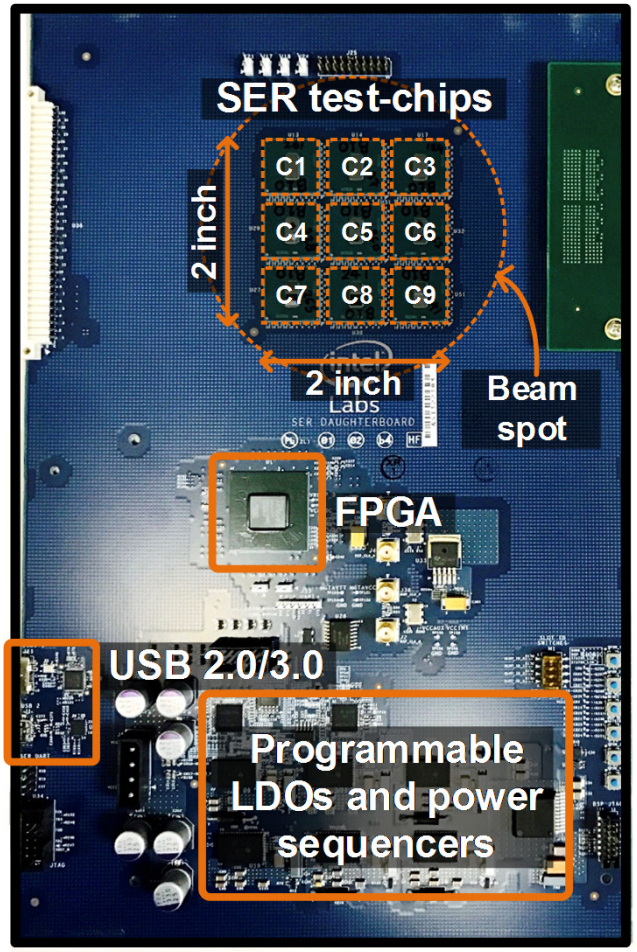
Gate Topologies Implemented

	Gate type	Description
1	INV8(16)-1X-RVT	8(16)-stage 1x inverter, regular V_T
2	INV8(16)-1X-LVT	8(16)-stage 1x inverter, low V_T
3	INV8(16)-1X-HVT	8(16)-stage 1x inverter, high V_T
4	INV8(16)-2X-RVT	8(16)-stage 2x inverter, regular V_T
5	INV8(16)-3X-RVT	8(16)-stage 3x inverter, regular V_T
6	INV8(16)-1X-RVT-FO3	8(16)-stage 1x inverter, fan-out 3, regular V_T
7	NAND8(16)-1X-RVT	8(16)-stage 1x nand, regular V_T
8	NAND8(16)-1X-LVT	8(16)-stage 1x nand, low V_T
9	NAND8(16)-1X-HVT	8(16)-stage 1x nand, high V_T
10	NAND8(16)-1X-RVT-FO3	8(16)-stage 1x nand, fan-out 3, regular V_T
11	NOR8(16)-1X-RVT	8(16)-stage 1x nor, regular V_T
12	NOR8(16)-1X-LVT	8(16)-stage 1x nor, low V_T
13	NOR8(16)-1X-HVT	8(16)-stage 1x nor, high V_T
14	NOR8(16)-1X-RVT-FO3	8(16)-stage 1x nor, fan-out 3, regular V_T
15	NAND_REV8(16)-1X-RVT	8(16)-stage 1x nand_rev, regular V_T
16	NOR_REV8(16)-1X-RVT	8(16)-stage 1x nor_rev, regular V_T
17	Dummy Readout Chain	For measuring SER in readout chain itself

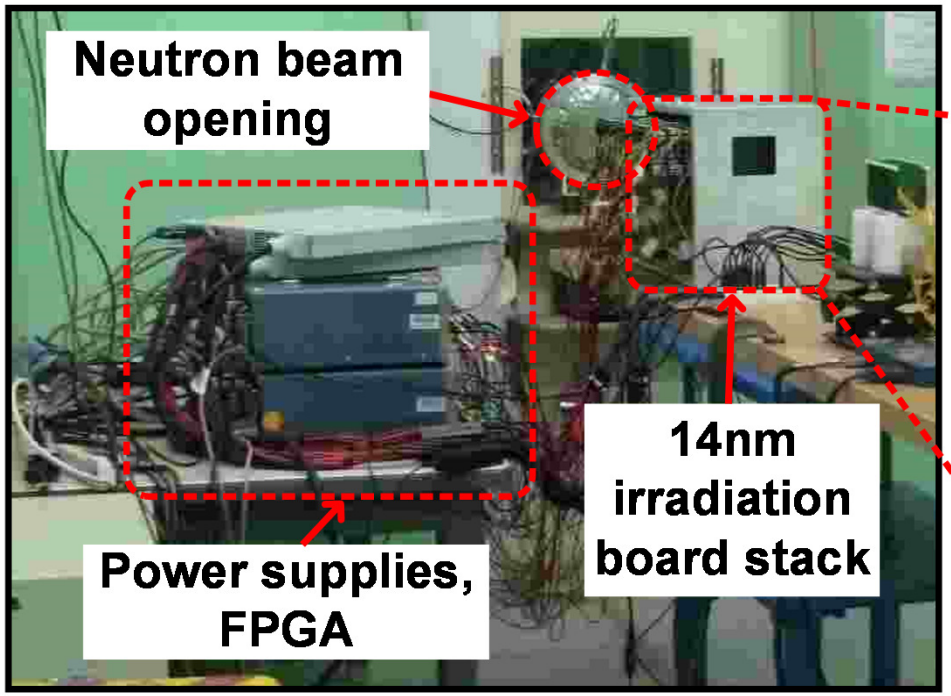


Irradiation Test-Board

- Neutron beam diameter: 3 inches
- FPGA with JTAG support for automated test control
- 9.6M x 9 chips = 86M gates per board



Neutron Beam Test Setup

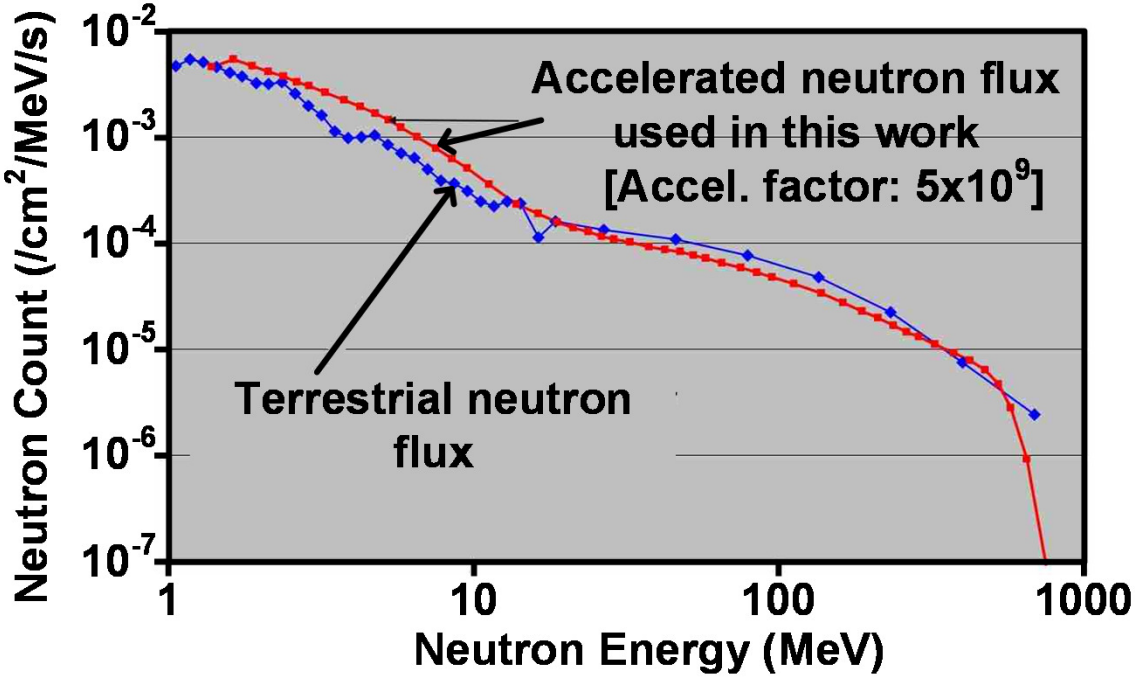


10 boards x 9 chips x 9.6M gates
= 0.86B gates

Custom aluminum enclosure for vertically stacking test-boards

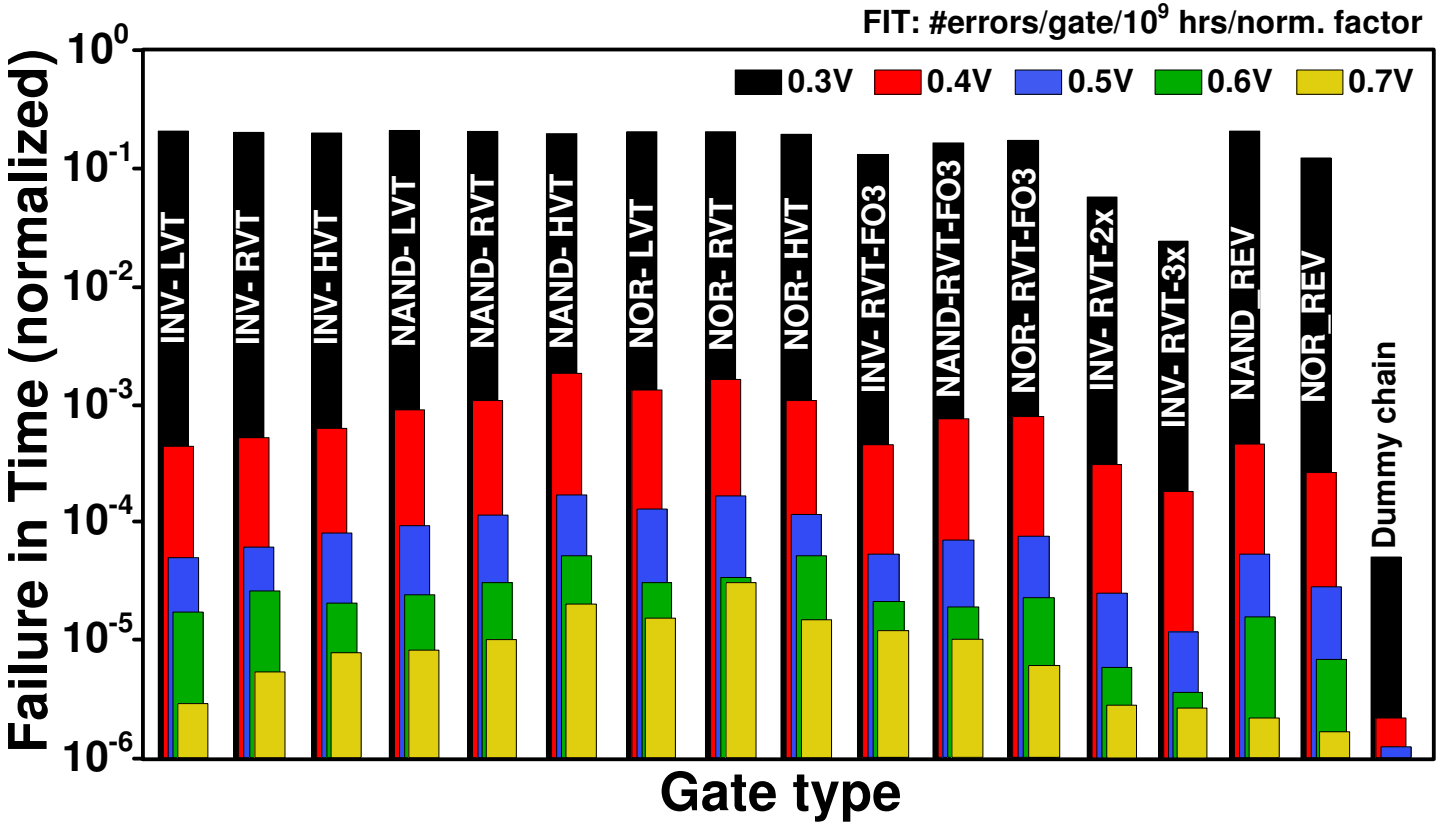
- Neutron irradiation tests performed at Los Alamos National Laboratory
- 90 chips irradiated for 5 days to collect real SET rate in logic chains

Neutron Beam Specs



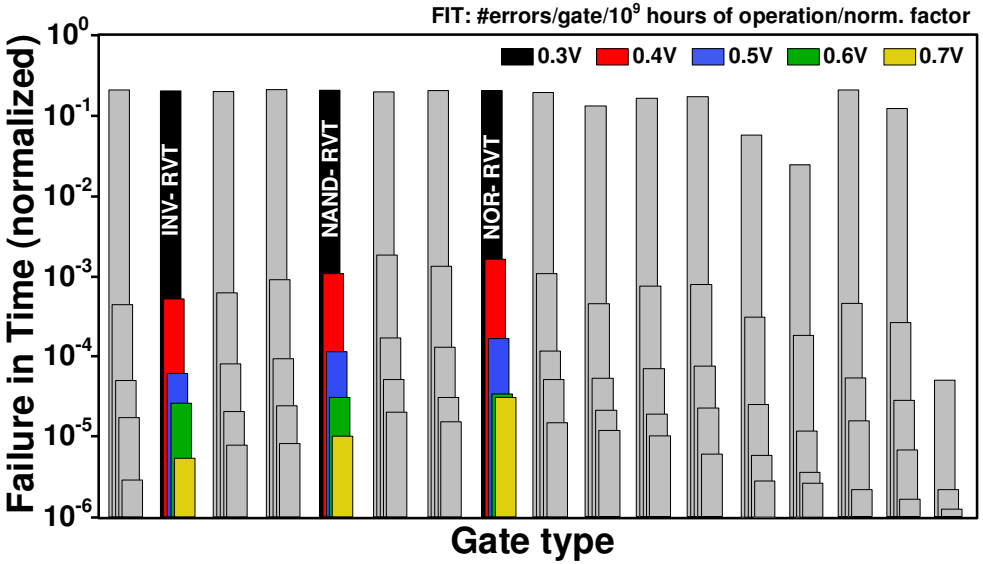
- Accelerated beam follows the terrestrial neutron energy profile
- Average beam energy range: 1.38 – 750MeV
- Average neutron flux: 4.2×10^4 neutrons/cm^2/s

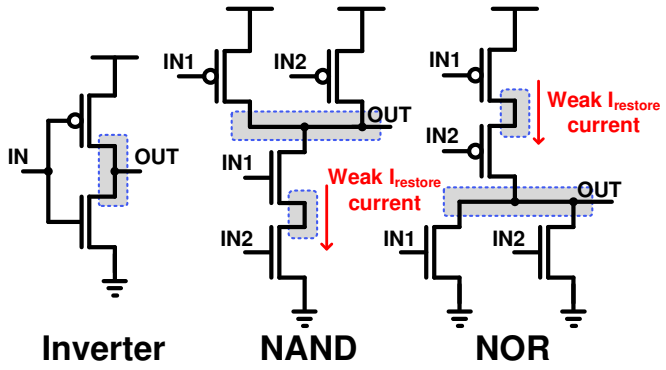
Neutron Irradiation Test Result

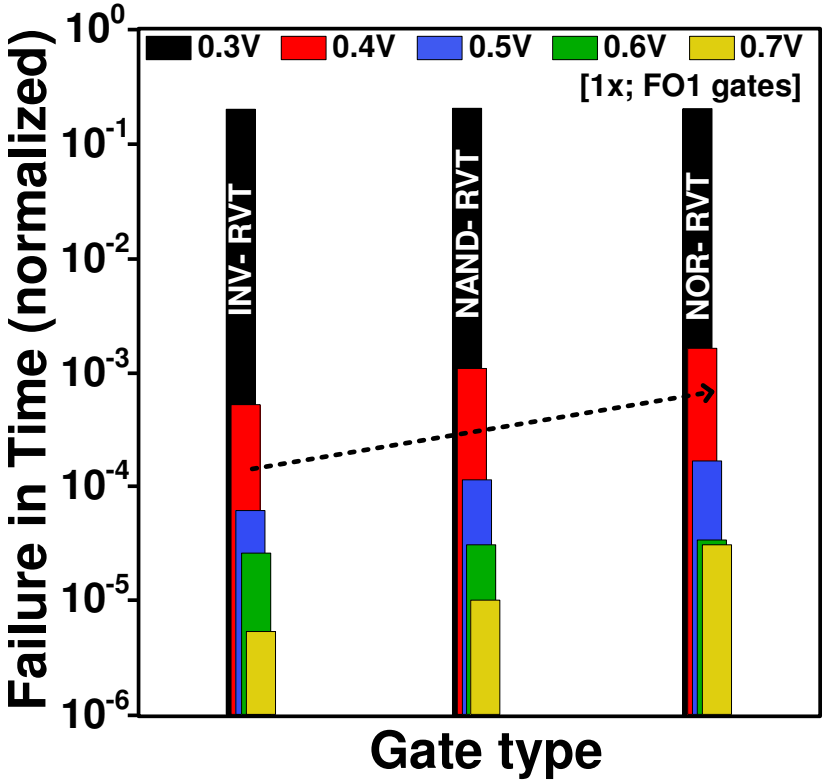


- **Combined SER for both 8 and 16 stage chains plotted**

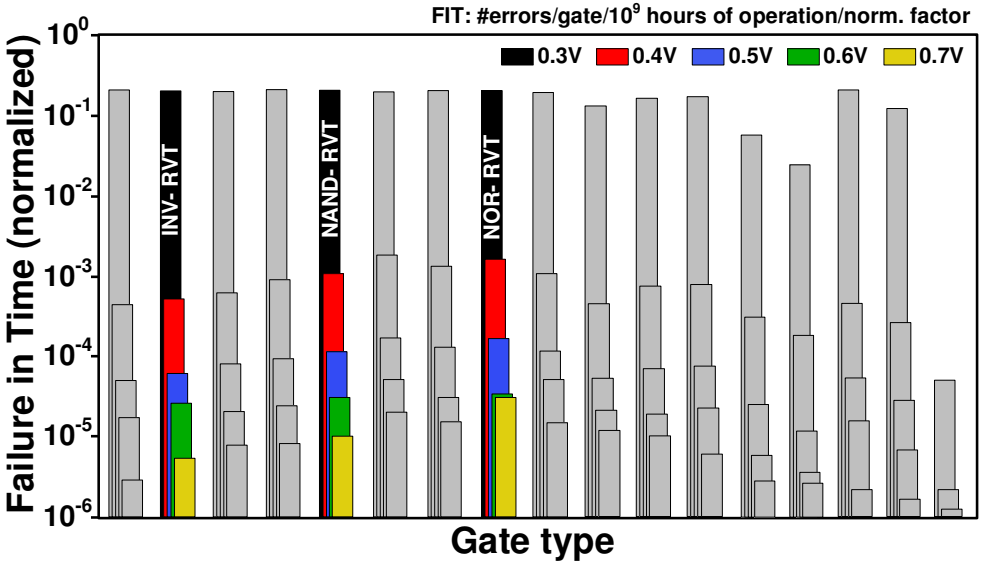
Gate Type Dependency

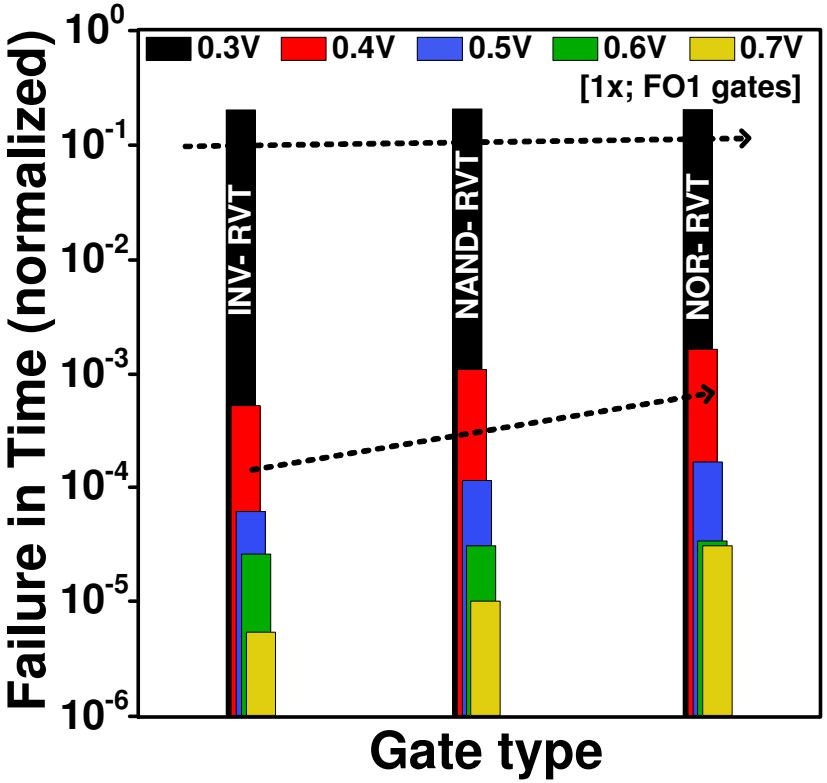






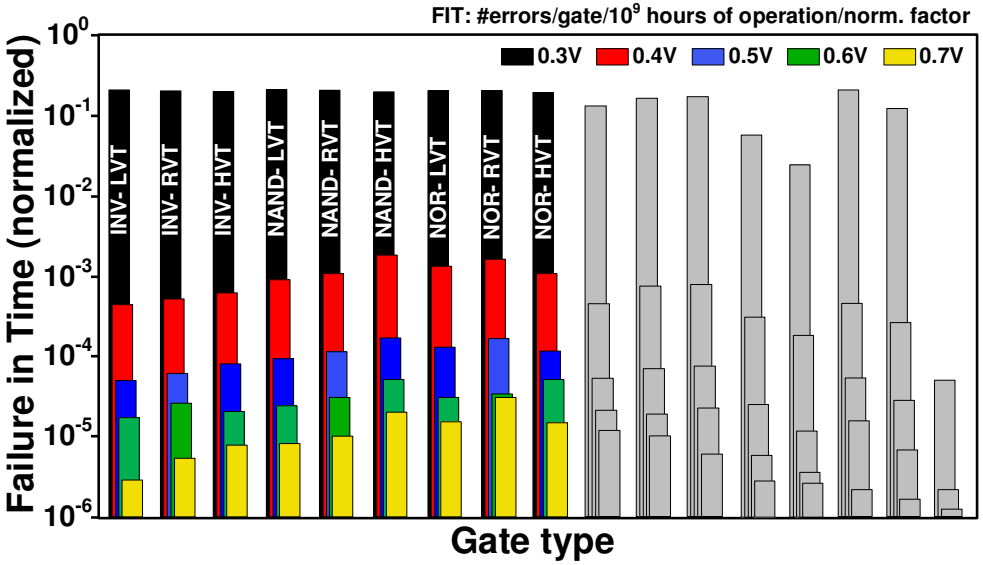
Supply Voltage Dependency



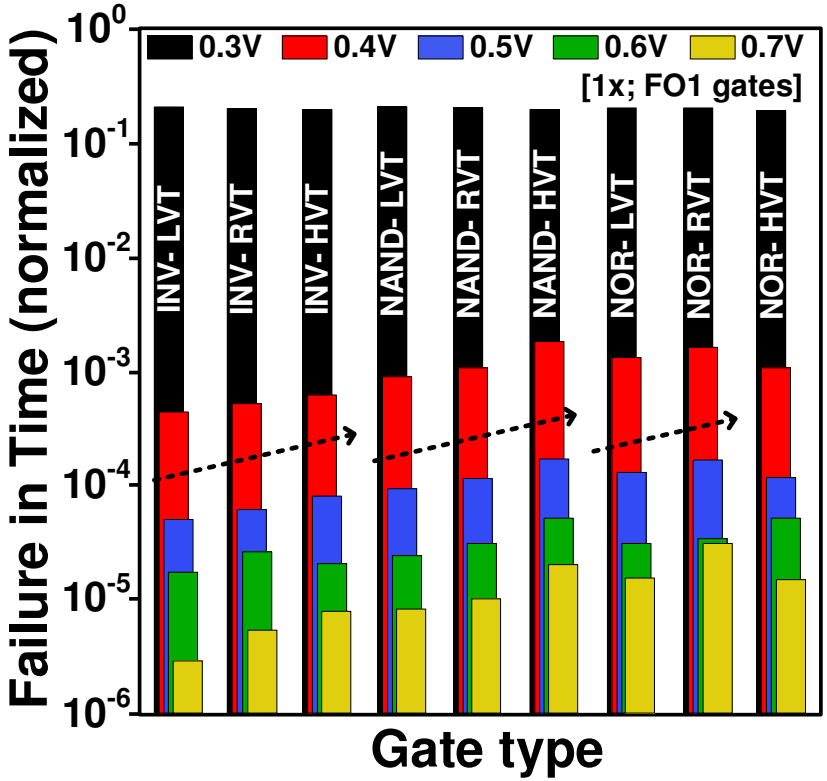


- **At 0.3V, SER does not depend as much on gate type**

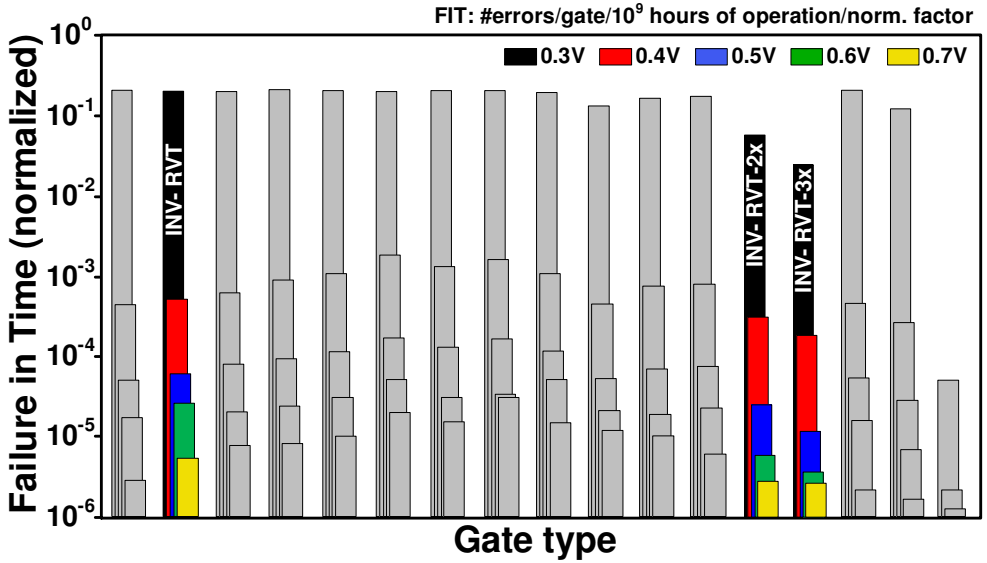
Threshold Voltage Dependency



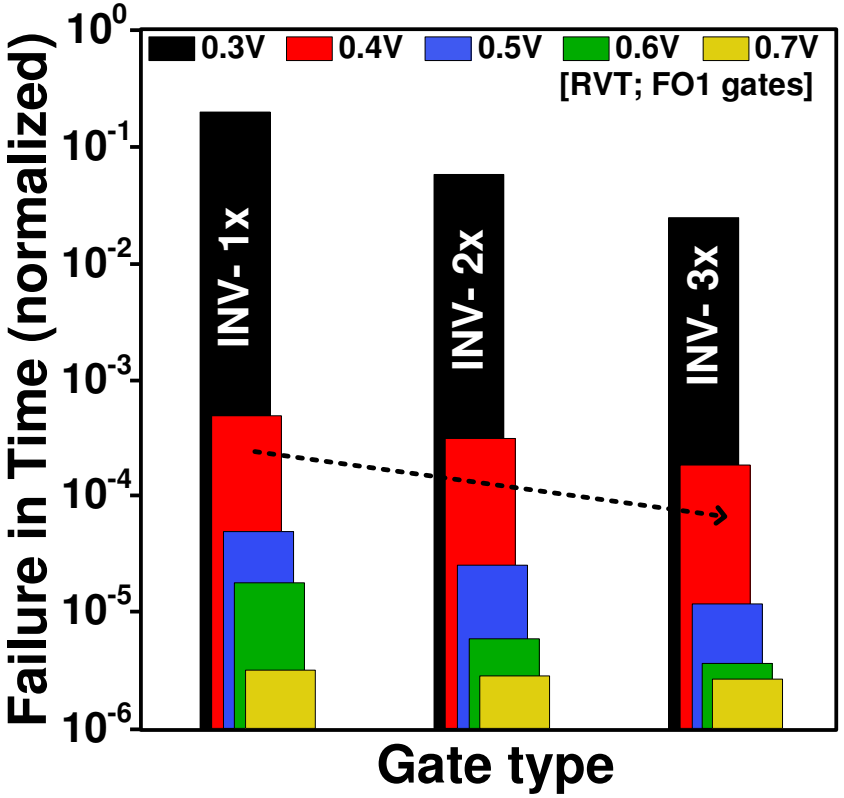
- $V_T\downarrow \rightarrow I_{restore}\uparrow \rightarrow$ SER decreases (with the exception of NOR HVT)



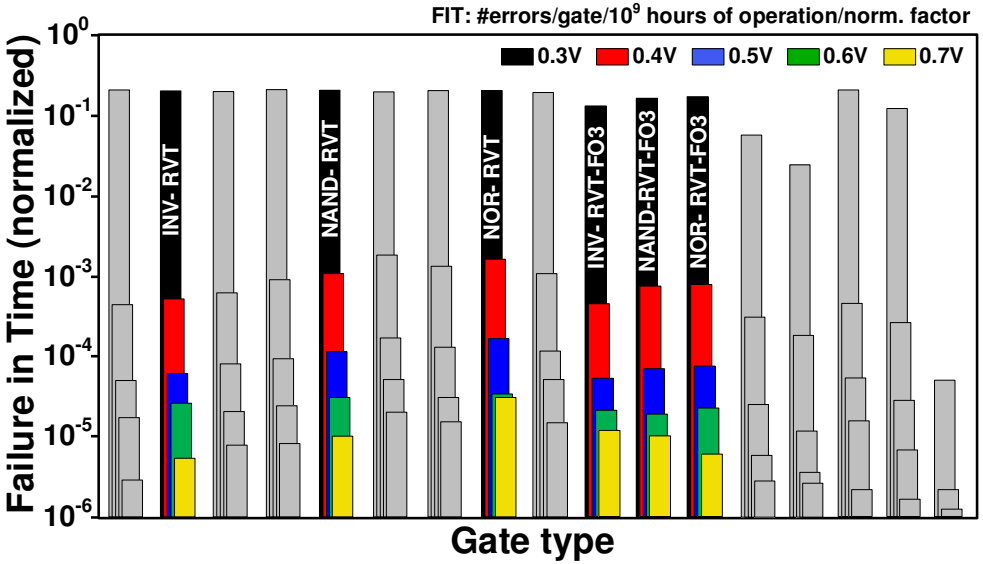
Device Size Dependency



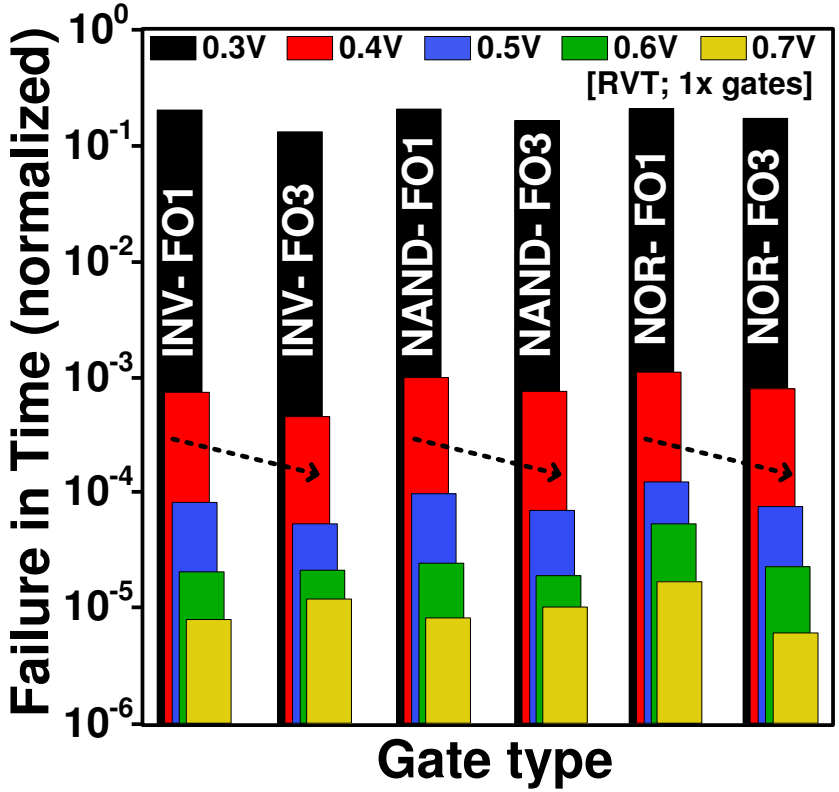
- W↑ → $I_{restore}$↑ → SER decreases
- W↑ → C_{node}↑ → SER decreases
- W↑ → J_{area}↑ → SER increases



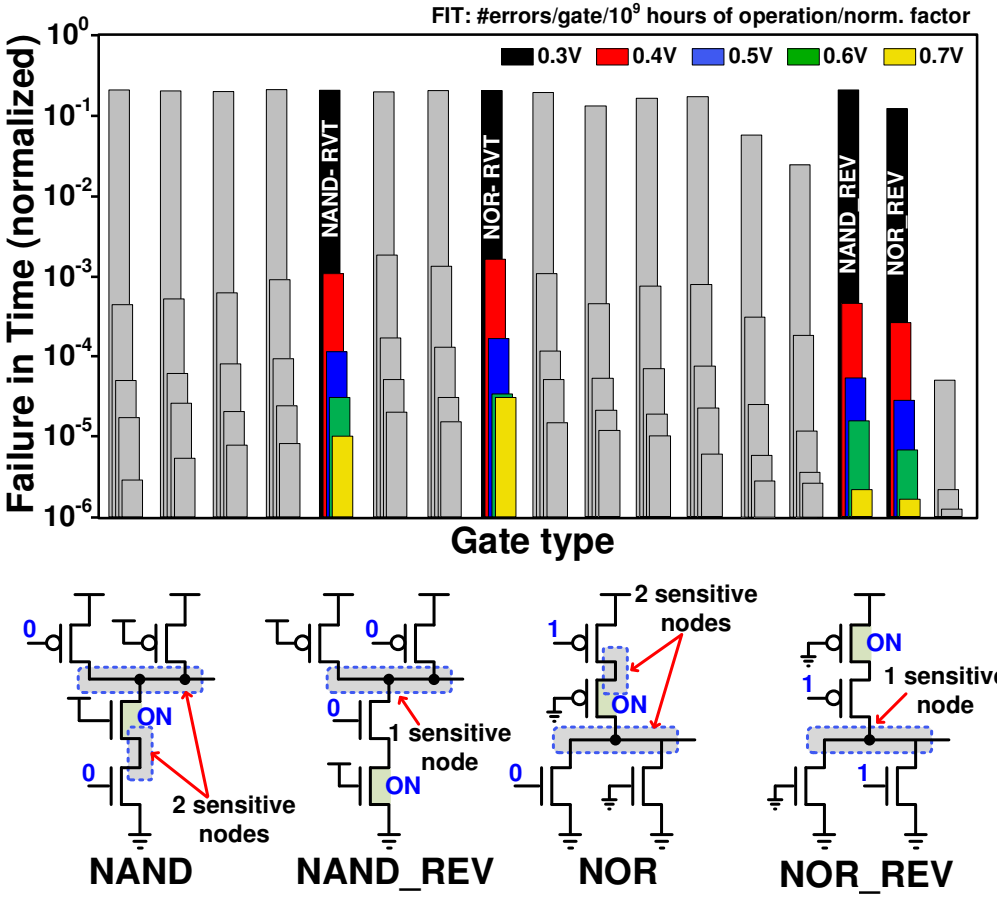
Fan-out Dependency

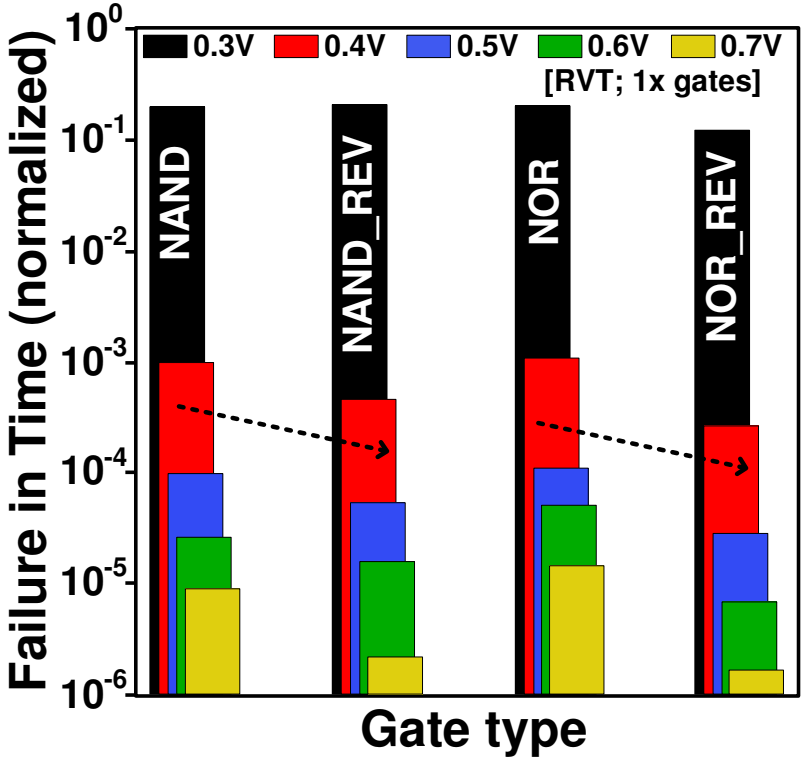


- Fanout↑ → C_{node}↑ → SER decreases
- Impact of capacitance on SER trends is similar across all VDDs

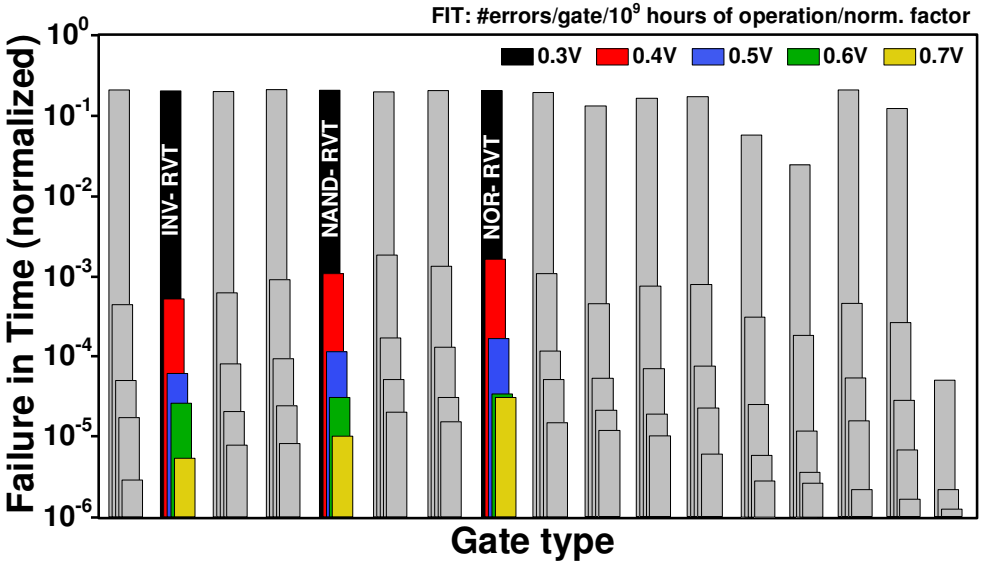


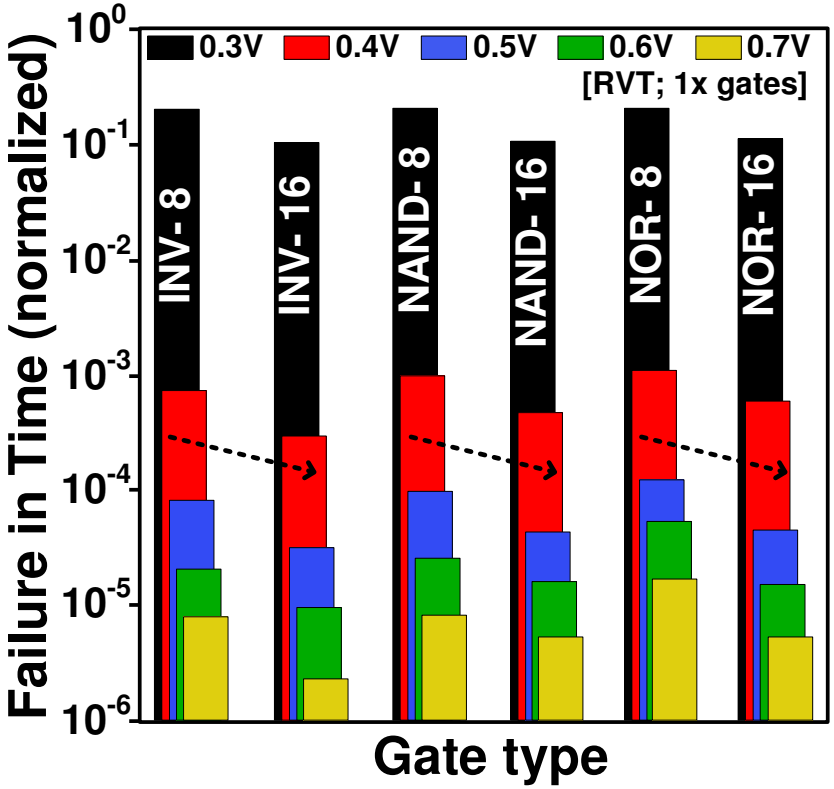
Input Connection Dependency





Chain Length Dependency

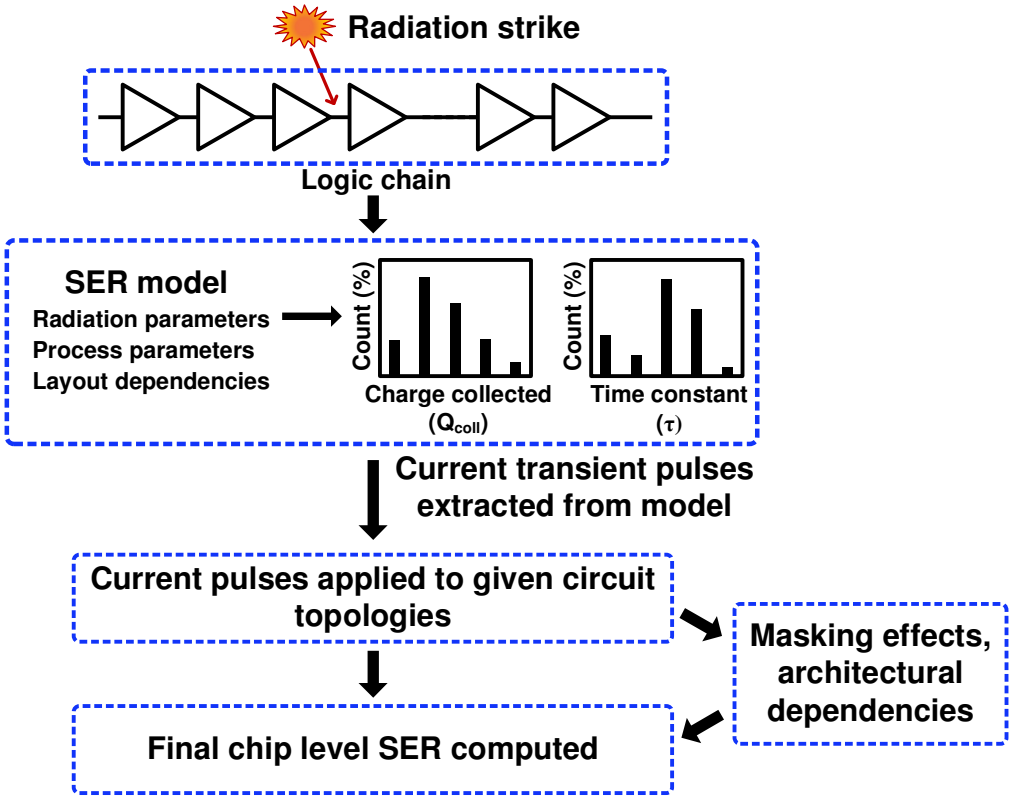




- **Longer chains: Increased number of marginal SET pulses get filtered out**

On-going Work: System-Level SER Estimation Framework Based on 14nm Logic SER Data

- Circuit dependencies: Input to analytical SER model
- SER Model: Extracts strike current parameters
- Can be applied to any given circuit/technology for SER estimation



Conclusion

- **Novel irradiation test structure with skewed NAND-NOR readout chain for logic SER characterization presented**
- **Proposed circuit is scalable, regular, and ultra-dense**
- **14nm test-chips irradiated under neutron beam**
- **Measured data captures SER dependence on various circuit parameters → basis for SER estimation framework**

Acknowledgements: **The authors would like to thank Dr. Heather Quinn at Los Alamos National Labs for her help with the neutron beam tests. This work was funded in part by the U.S. Government. The data analysis work was partially supported by the Defense Threat Reduction Agency under Basic Research Award No. HDTRA1-14-1-0042. The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the U.S. Government.**