An Ultra-Dense Irradiation Test Structure with a NAND/NOR Readout Chain for Characterizing Soft Error Rates of 14nm Combinational Logic Circuits

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Abstract

This paper describes a 14nm test chip employing a novel NAND/NOR readout chain for characterizing soft error rate (SER) in combinational logic gates. The proposed test structure uses high density standard logic gates as detection circuit for sensing Single Event Transients (SETs) that are then forwarded to a skewed NAND-NOR readout chain which funnels all SET pulses while expanding the pulse width to ensure they reach the final triple modular redundant (TMR) counter. The proposed circuit is compact, has a scalable architecture based on a unit cell layout, and incurs minimal area overhead. Different gate configurations (device size, threshold voltage, fan-out and chain length) were implemented in the 14nm test-chip and irradiated under a neutron beam to collect a massive amount of statistical data. Radiation data captures, for the first time, the impact of various circuit parameters on combinational logic SER in 14nm tri-gate technology.

Introduction

Soft error remains a critical reliability concern in scaled technologies due to the increasing transistor count per chip and the reduced operating voltage [1, 2, 3]. In order to tackle radiation effects in integrated circuits, designers need to accurately analyze circuit dependencies that impact soft error rate (SER). Fig. 1 illustrates a combinational SER event occurring in a logic gate chain and a sequential SER event occurring in a latch storage node, respectively. As the radiation particle penetrates the silicon, an ion track is generated along its strike path. This results in charge generation which is collected by nearby diffusion junctions. The collected charge, if large enough, induces a transient pulse in case of combination logic path or a bit flip in case of a memory storage node. The former is referred to as Single Event Transient (SET) while the latter is called Single Event Upset (SEU).

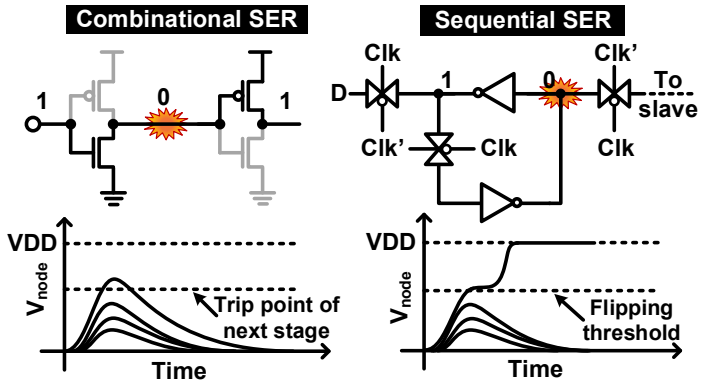


Fig. 1. Combinational versus sequential SER illustration. Radiation particle strike can induce a transient pulse in logic chain resulting in an SET event. In case of a latch/flop storage node, the strike can flip the logic state resulting in single event upset (SEU) error. SET is dynamic while SEU is a static event.

Recent studies [4, 5] have shown a steady rise in combinational logic SER contribution as compared to sequential/memory (or latch) SER, with process scaling and increasing clock frequencies. Previous works have focused mostly on memory or latch SER and only few works have studied circuit factors contributing to logic SER. This work represents the first attempt to assess various circuit dependencies that impact logic SER in FinFET technology.

Critical charge (Q_{crit}) is typically defined as the minimum collected charge at a circuit node that can cause an SET or SEU event. Q_{crit} associated with a given circuit node is a function of radiation, process, and circuit parameters. Radiation parameters affecting SER include particle flux, linear energy transfer, and the angle of incidence. Process parameters such as fin geometry, doping profile, doping density, and junction geometry affect the charge collection efficiency. Finally, circuit parameters listed in Fig. 2 such as transistor width, threshold voltage (V_T), fan-out, chain length, supply voltage, and P/N ratio have a strong impact on SER. Understanding the contribution of various circuit parameters on SER is a critical aspect in developing a radiation hardening strategy.

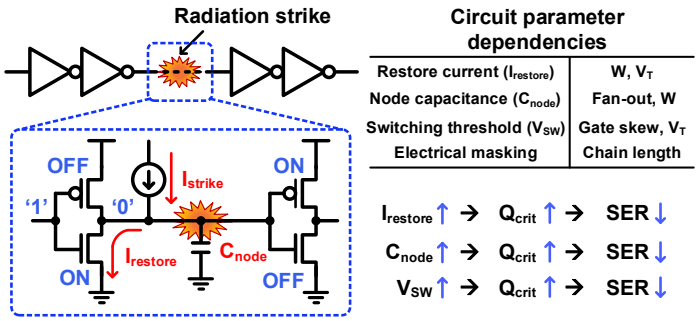


Fig. 2. Various circuit dependencies that impact SER on circuit level and the associated circuit parameters. To design an optimized RHBD circuit, proper understanding of these dependencies is a must.

In order to accurately analyze logic SER and impact of various circuit parameters on it, we need an irradiation test structure that meets the following requirements: good representation of standard logic gates; numerous gate configurations; uniform layout; ultra-high density; scalable architecture; and minimal area overhead for readout circuits. These requirements are critical for collecting a statistically significant amount of data from various gate types across different supply voltages within a limited beam time. In this work, we designed dedicated SER test structures in 14nm tri-gate technology that satisfy all the requirements listed above. The test chips were taken to Los Alamos National Laboratory (LANL) and irradiated under a neutron beam to collect a large amount of statistical data for studying SER dependence on various circuit parameters.

NAND/NOR Readout Chain

The proposed high-density SER characterization circuit is shown in Fig. 3. The circuit consists of two main parts, viz. the SET detection chain that consists of multiple chains of serially connected standard logic gates and a readout chain implemented using skewed NAND-NOR gates. Detection chains are implemented in several gate type configurations such as inverter, NAND, NOR gates. For each gate type, different device size, threshold voltage, fan-out and chain length topologies are implemented, each capturing a specific circuit dependency.

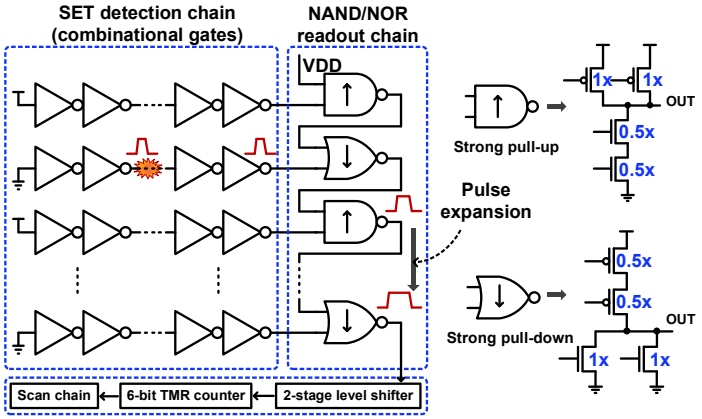


Fig. 3. SER measurement circuit consisting of SET detection chains and a NAND/NOR readout chain. Readout chain is comprised of opposite skewed NAND-NOR gates, each one connected to one detection chain branch. Skew enables pulse expansion along the readout path so that all pulses reach the TMR counter.

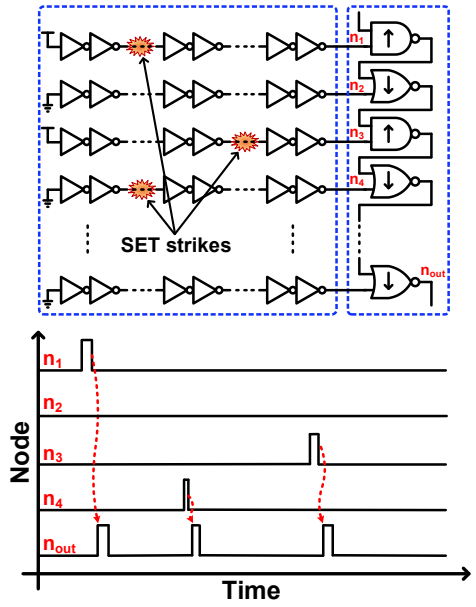


Fig. 4. SET pulse collection using skewed NAND-NOR readout chain.

Fig. 4 illustrates the operation of the NAND/NOR readout chain. All detection chains are connected in parallel to the readout chain. This enables funneling of all SET pulses in the readout chain from where these propagate to the final output node where a 6-bit TMR counter keeps track of the pulse count. Skewed NAND/NOR gates allow for pulse expansion once the SET pulses enter the readout chain. This ensures that all pulses injected by the detection chains reach the final output node without disappearing in the middle. This feature allows for large scale expansion of this circuit without compromising the pulse counting accuracy.

Fig. 5 shows the chip layout and overall core architecture of the 14nm test-chip. Six identical ultra-dense cores, each consisting of 16 pairs of different gate topologies are implemented in 8 and 16 stage chain lengths. A dummy NAND-NOR chain is also included to measure the SER of the readout chain itself. Later radiation tests confirm that the number of SET events in the NAND-NOR readout chain is negligible compared to the number of SET events in the logic gate chains. Table I enlists all the gate configurations implemented in the test chip. Each gate type is implemented in chain lengths of 8 and 16 stages to study the impact of electrical masking effect. NAND_REV and NOR_REV chains consist of the NAND/NOR gates with reversed input connections. This helps in analyzing the dependence of SER on input connection.

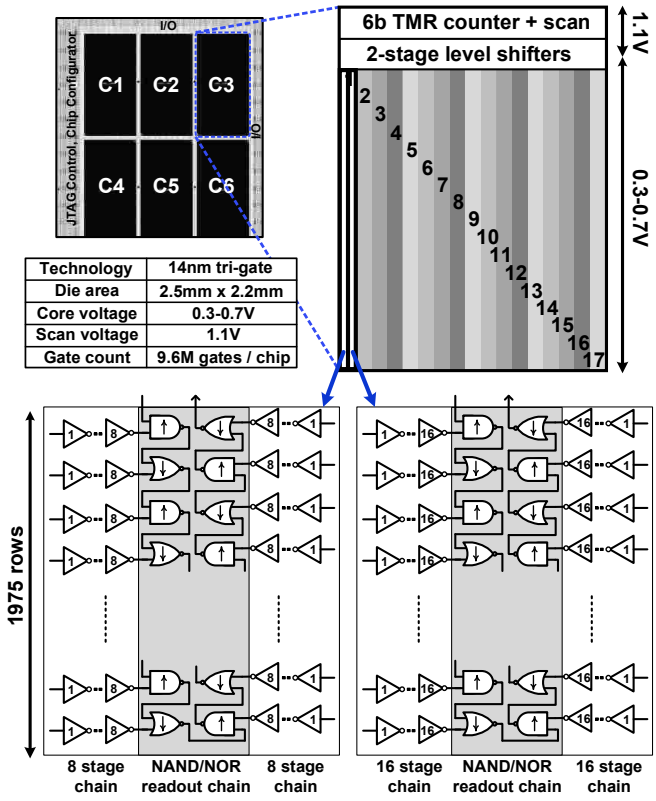


Fig. 5. 14nm test chip layout and core implementation. Uniform and scalable architecture allows maximum detection area and script-based automated layout generation. Skewed NAND-NOR readout chain induces pulse expansion thereby ensuring each SET pulse reaches the TMR counter.

Table I. Various gate configurations implemented in 14nm SER test chip

	Gate type	Description
1	INV8(16)-1X-RVT	8(16)-stage 1x inverter, regular V_T
2	INV8(16)-1X-LVT	8(16)-stage 1x inverter, low V_T
3	INV8(16)-1X-HVT	8(16)-stage 1x inverter, high V_T
4	INV8(16)-2X-RVT	8(16)-stage 2x inverter, regular V_T
5	INV8(16)-3X-RVT	8(16)-stage 3x inverter, regular V_T
6	INV8(16)-1X-RVT-FO3	8(16)-stage 1x inverter, fan-out 3, regular V_T
7	NAND8(16)-1X-RVT	8(16)-stage 1x nand, regular V_T
8	NAND8(16)-1X-LVT	8(16)-stage 1x nand, low V_T
9	NAND8(16)-1X-HVT	8(16)-stage 1x nand, high V_T
10	NAND8(16)-1X-RVT-FO3	8(16)-stage 1x nand, fan-out 3, regular V_T
11	NOR8(16)-1X-RVT	8(16)-stage 1x nor, regular V_T
12	NOR8(16)-1X-LVT	8(16)-stage 1x nor, low V_T
13	NOR8(16)-1X-HVT	8(16)-stage 1x nor, high V_T
14	NOR8(16)-1X-RVT-FO3	8(16)-stage 1x nor, fan-out 3, regular V_T
15	NAND_REV8(16)-1X-RVT	8(16)-stage 1x nand_rev, regular V_T
16	NOR_REV8(16)-1X-RVT	8(16)-stage 1x nor_rev, regular V_T
17	Dummy Readout Chain	For measuring SER in readout chain itself

Neutron Irradiation Test and Measurement Results

Fig. 6 (top) shows the test setup at Los Alamos National Laboratory where 10 test-boards, each having 9 test-chips (90 chips in total) were irradiated in parallel under a neutron beam. Massive statistical data was collected for multiple supply voltage points. Fully automated irradiation tests were conducted for a duration of four effective days using an FPGA based remote control setup. The neutron beam energy spanned from 1.38MeV to 750MeV. Fig. 6 (bottom) shows the energy spectrum of the accelerated neutron beam used for our irradiation test which closely matches that of terrestrial neutron exposure (after accounting for the acceleration factor). The average neutron beam flux was 4.2×10^4 particles/cm^2/s. Due to their low stopping power, neutrons can penetrate through multiple dies without any appreciable loss of energy. This allows the boards to be stacked along the beam path without any issues of diffraction or significant energy loss.

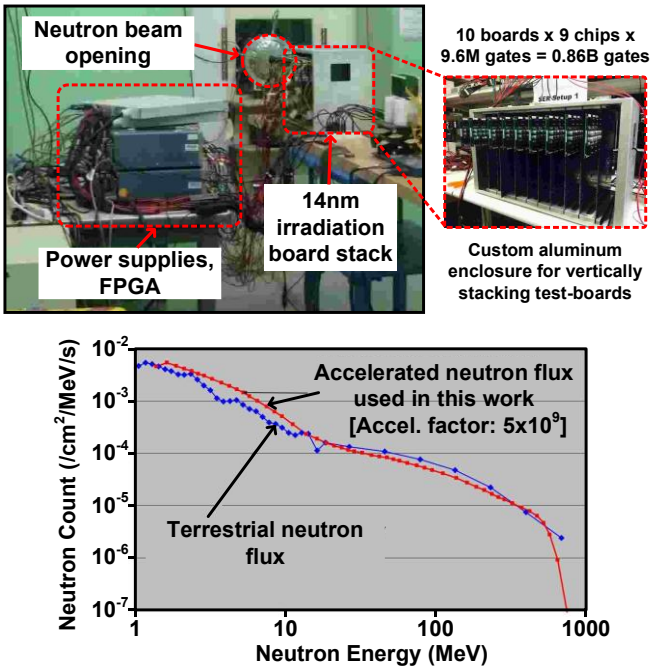


Fig. 6. LANL test setup for neutron irradiation experiment. Spallation neutron beam spectrum at LANL closely follows the terrestrial energy spectrum with an associated acceleration factor to speed up SER induction.

The following sub-sections discuss in detail, measured results from the irradiation test, capturing individual circuit dependency and its impact on the SER trends. All measurements have been taken for supply voltages from 0.3V to 0.7V.

A. Threshold voltage (V_T) dependency

As the transistor V_T increases, restore current ($I_{restore}$) gets weaker which makes the circuit node more susceptible to radiation strikes. This trend is evident in the radiation data shown in Fig. 7 where normalized failure in time (FIT) rates for gates with different V_T have been shown for 0.3-0.7V supply voltages. FIT is defined as the number of soft errors per gate in a billion hours of circuit operation.

Low V_T (LVT) gates exhibit lower SER as compared to regular V_T (RVT) and high V_T (HVT) gates. Supply voltage scaling also has a strong impact on SER. For a lower VDD, SER increases exponentially. This can be attributed to the fact that with lower VDD, Q_{crit} reduces resulting in higher SER. There is about a 10^5x increase in FIT rate when VDD is scaled from a nominal value of 0.7V to a near-threshold (NTV) value of 0.3V. Moreover, at NTV, Q_{crit} becomes extremely low and hence almost all particles that induce charge collection, result in a soft error. This is reflected in the black bars in Fig. 7. That is, V_T does not have a dominating impact on FIT rate at 0.3V resulting in constant FIT rates irrespective of the V_T type.

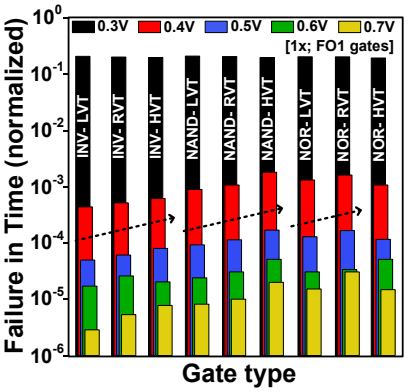


Fig. 7. Measured FIT rates for various gates with different threshold voltages plotted for multiple supply voltage points.

FIT rates of NAND and NOR gates were higher compared to inverters. This can be attributed to the fact that in both NAND and NOR gates, there are two sensitive nodes susceptible to SER as compared to single node in case of an inverter. Stacked transistors in NAND/NOR gates further weaken $I_{restore}$, thereby, contributing to a higher FIT rate.

B. Device size (W) dependency

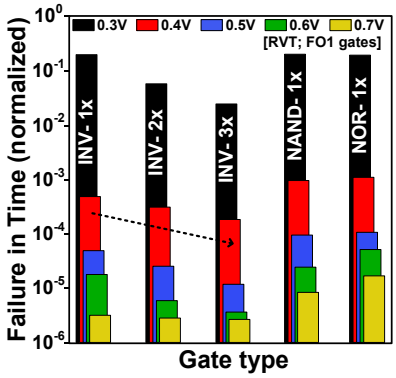


Fig. 8. Measured FIT rates for various gates with different device size plotted for multiple supply voltage points

Fig. 8 shows the measured FIT rates for various gates with different device size (W). As the device size increases, $I_{restore}$ gets stronger, junction area becomes larger, and gate capacitances get bigger. These cumulative effects result in much higher Q_{crit}, thereby, leading to a much lower SER across all VDD points. Unlike the case of varying V_T, here noticeable variation can be seen in FIT even at 0.3V. This can be attributed to the fact that although the contribution from $I_{restore}$ is small at lower VDDs, variation in node capacitance can still dominate the final SER values even at lower voltages.

C. Fan-out dependency

For higher fan-out, the output node capacitance increases which reduces the SER. Fig. 9 shows measured FIT results for inverter, NAND and NOR gates with fanout=1 and fanout=3 topologies.

Results confirm that with an increased fan-out, node capacitance goes up, resulting in a higher Q_{crit} and hence lower SER. Results for 0.3V show that the impact of capacitance is still prevalent even at lower voltages. This confirms that increasing the capacitance of a sensitive circuit node is a viable option for reducing the SER across different supply voltages.

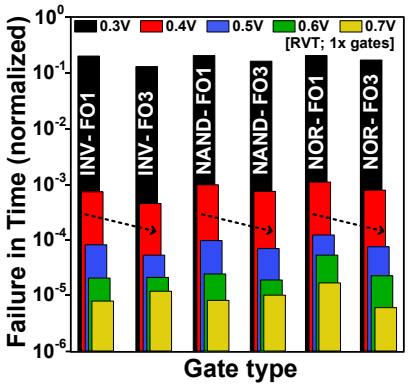


Fig. 9. Measured FIT rates for various gates with different fan-out (node capacitance) plotted for multiple supply voltages

D. Input connection dependency

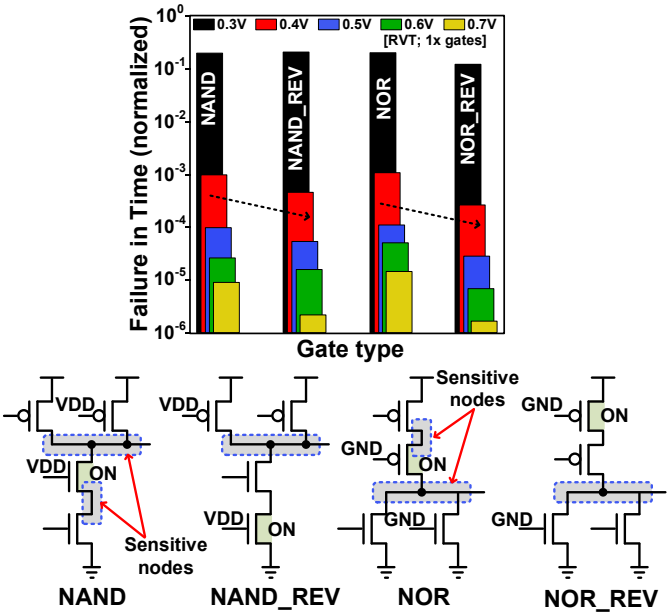


Fig. 10. Measured FIT rates for NAND and NOR gates with different input connections plotted for multiple supply voltage points

Fig. 10 shows FIT rates for NAND and NOR gates with different input connection orders. Changing the input order results in reduction of a sensitive node in case of both NAND_REV and NOR_REV gate configurations. This directly impacts the effective diffusion area susceptible to soft errors. Results show similar trends with the REV versions reporting lower FIT rates as compared to the default input configuration.

E. Chain length dependency

Previous studies [6] have shown that pulse width quenching and/or broadening is a common phenomenon as SET pulses propagate down a logic path. This contributes to electrical masking effect where SET pulses in longer chains may shrink and expand before getting captured by the read-out chains in our test chip. Fig. 11 shows FIT rates measured for 8 and 16 stages chains which allows us to study this effect. Clearly, per gate SER for a longer chain length is smaller as compared to the shorter one. This can be attributed to electrical masking and possible pulse quenching occurring in the detection circuit.

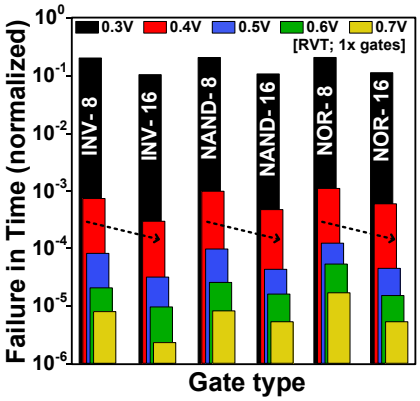


Fig. 11. Measured FIT rates for gates with two different chain lengths (i.e. 8 and 16) plotted for multiple supply voltage points

Comparison with Prior Art

Fig. 12 shows the comparison summary table with respect to prior arts. The proposed SER measurement circuit has the following unique features: (i) uniform and scalable layout geometry, (ii) different gate topologies to accurately study various circuit dependencies, (iii) minimal area overhead in terms of counters and (iv) immunity to pulse width distortion effects in read-out path.

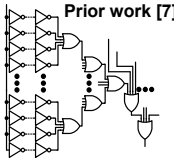
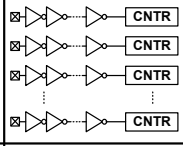
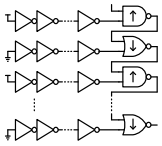
	Prior work [7]	Prior work [8]	This work
			
Features	Pulse count and pulse width meas.	Pulse count meas.	Pulse count meas.
Layout	Irregular, not easily scalable	Regular, not scalable	Regular, scalable
Area overhead	Small	Large (dominated by counter area)	Small
Pulse width distortion	Susceptible	Immnue	Immune
Technology	45nm SOI	65nm bulk	14nm bulk

Fig. 12. Comparison summary table

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References: [1] D. Rossi, et al., TVLSI, 2009. [2] S. Kumar, et al., VLSI Circuits Symposium, 2017. [3] S. Kumar, et al., NSREC, 2017, [4] N. N. Mahatme, et al., TNS, 2011. [5] N. N. Mahatme, et al., TNS, 2014. [6] J. R. Ahlbin, et al., TNS, 2009. [7] T. D. Loveless, et al., TNS, 2012. [8] R. Pawlowski, et al., CICC, 2014.