A 0.0054-mm^2 Frequency-to-Current Conversion-Based Fractional Frequency Synthesizer in 32 nm Utilizing Deep Trench Capacitor

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***Abstract*—In this brief, a frequency-to-current conversion-based fractional frequency synthesizer is implemented in 32-nm technology utilizing a high-density deep trench capacitor. The technique proposed here can replace the use of multiple crystal oscillators or a phase-locked loop for medium accuracy clock generation with very low chip area and power consumption. In addition to exploiting the inherently low variation of capacitors as compared to that of transistors, the proposed circuit generates an output frequency proportional to the capacitor ratio, canceling out any small process-voltage-temperature (PVT) dependences of the capacitor. The performance of the fractional synthesizer is verified from chip measurement results. An output frequency range of 16–156 MHz is covered with a frequency resolution of 0.8 MHz using a 4-MHz reference clock. The total area of the frequency synthesizer core is only 0.0054 mm^2, and it consumes 116 μW of power from a 0.9-V supply while generating an output frequency of 48 MHz. The output frequency variation is $\pm$0.14% at 48 MHz for a temperature sweep from -40 °C to 90 °C. Periodic jitter measured from an on-chip high-resolution jitter measurement circuit is 115 ps (rms) at 76 MHz.**

***Index Terms*—Deep trench capacitor, frequency synthesizer, on-chip jitter measurement, voltage-controlled oscillator.**

I. Introduction

INTEGRATED circuits for Internet-of-Things applications, such as health care monitoring, inventory tracking, automotive sensors, smart grid, and robotic systems, require a medium frequency accuracy clock with low power consumption and small form factor. These systems typically require multiple clocks with frequencies ranging from a few hertz (e.g., low frequency internal wake-up timers) to hundreds of megahertz (e.g., memory or signal processing) [1]. Crystal oscillators generate a clean clock, but the use of multiple crystals increases the form factor and cost. Therefore, high frequency clocks are typically generated using frequency synthesizers that multiply the frequency generated from an external low frequency crystal oscillator.

Phase-locked loops (PLLs) are conventionally used to generate very accurate frequency multiplications. However, maximum bandwidth limitation [2] requires large loop filter area and higher settling time. High power consumption and insufficient stability over a wide frequency range are other key challenges for PLL design in scaled technologies. All digital PLLs [3] have been gaining popularity for area reduction, but it requires a high-resolution time-to-digital converter that increases power consumption, quantization noise, and output frequency spurs. To address these limitations of PLL, Drago *et al*. [4] propose a duty-cycled integer-N PLL that sacrifices frequency accuracy to reduce power and settling time. In [5] and [6], free-running oscillators are used with periodic frequency calibration. However, these approaches suffer from inaccurate output frequencies. A frequency-to-voltage converter-based frequency synthesizer is proposed in [7] by capacitive charge redistribution. However, voltage generation will have large inaccuracy due to leakage in advanced technologies. On top of that, depending on the input and output frequency, comparator input voltages may vary over a large range, and that can change the comparator gain and frequency accuracy. Also, this implementation is not verified with actual chip measurement results. In this brief, a circuit technique based on frequency-to-current conversion is proposed that can replace a PLL or the use of multiple crystal oscillators in a single chip, for medium accuracy frequency synthesis over a wide frequency range (e.g., 10X). This technique uses multiple current branches to tune the output frequency very precisely. The proposed technique is implemented in 32-nm technology, and performance is verified from measurement results. Unlike other compensated ring oscillator-based architectures [10] that rely on the accuracy of the reference generation circuit and the capacitor, here, the capacitance ratio in the final frequency expression cancels any PVT variations of the capacitor. High-density deep trench capacitors can significantly reduce the silicon area because their 3-D nature is used for loop stability. A detailed mathematical model of the loop is derived for stability analysis. In addition, a high-resolution digital on-chip jitter measurement circuit is implemented to measure the clock periodic jitter accurately.

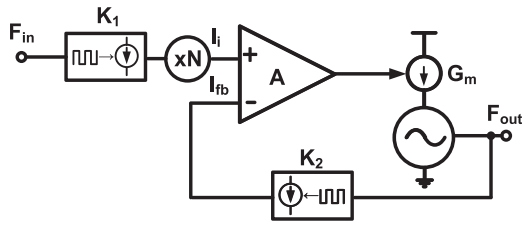

Fig. 1. Proposed frequency synthesizers based on current multiplier.

Manuscript received May 9, 2015; revised September 10, 2015; accepted November 21, 2015. Date of publication November 26, 2015; date of current version April 28, 2016. This brief was recommended by Associate Editor M. Shuo-Wei Chen.

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Digital Object Identifier 10.1109/TCSII.2015.2504263

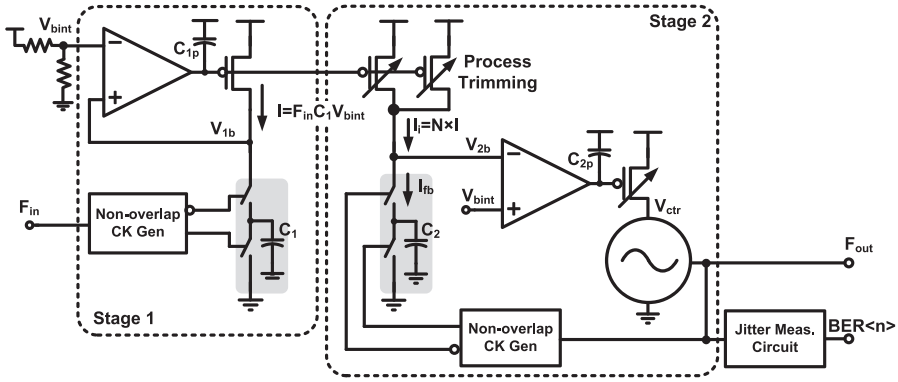


Fig. 2. Proposed current multiplier-based frequency synthesizer schematic with on-chip periodic jitter measurement circuit.

Section II describes the proposed architecture of the frequency synthesizer. Section III provides the circuit implementation details. The small signal loop model and stability analysis are performed in Section IV. The on-chip jitter measurement circuit is covered in Section V. Section VI shows the measurement results, followed by the conclusion in Section VII.

II. Proposed Frequency Synthesizers

Fig. 1 shows the proposed architectures of the frequency synthesis technique by a frequency-to-current converter (FTC) circuit. In this current multiplication-based dividerless architecture shown in Fig. 1, the input frequency $(F_{\rm in})$ is converted to an equivalent current by an FTC of gain K_1 and then multiplied by a factor of N to generate current I_i. The oscillator output frequency $(F_{\rm out})$ is converted to an equivalent current $(I_{\rm fb})$ by an FTC with a gain of K_2. A high-gain amplifier is used to make these two input currents equal by adjusting the voltage-controlled oscillator (VCO) frequency. If the loop gain is high, the input and output frequency relationship can be written as

$$F_{\rm out} = N\frac{K_1}{K_2}F_{\rm in}. \tag{1}$$

The frequency multiplication factor here is N^*K_1/K_2. Because N can be implemented in the analog domain by current mirrors, it can be designed to be very large without increasing hardware complexity, as in the case of a digital PLL. Also, fractional-N can be easily generated without any fractional frequency divider or delta-sigma modulator [8]. However, due to process mismatch, N cannot be exact. A Monte Carlo simulation shows a 2.2% σ/μ variation in N due to process mismatch. Therefore, additional process-trimming current branches are required to compensate this mismatch effect. The number of branches can be tuned during initial frequency calibration by comparing $F_{\rm out}$ with desired output frequency. As the frequency multiplication factor depends on the K_1/K_2 ratio, any PVT dependences of FTCs get cancelled. Both K_1, K_2 can be minimized to reduce power consumption, keeping the K_1/K_2 ratio fixed.

III. Circuit Implementation

Fig. 2 shows the circuit implementation of the proposed frequency synthesizer. Stage 1 converts input frequency $(F_{\rm in})$ to proportional current by an FTC of gain $K_1 = C_1V_{\rm bint}$. Current multiplication is performed in stage 2 using a current mirror. Additional current branches are used to compensate the process mismatch in the circuit. In the layout design, a common centroid technique is used to minimize the process mismatch. A high-gain comparator is used to detect the difference between the multiplied input current (I_i) and the feedback current $(I_{\rm fb})$ generated from output frequency by an FTC of gain $K_2 = C_2V_{\rm bint}$. Therefore, the frequency multiplication factor here is N^*C_1/C_2. As $V_{\rm bint}$ gets cancelled in the final expression, it can be generated simply by dividing the supply voltage. Also, the capacitance ratio makes the output frequency insensitive to temperature variation.

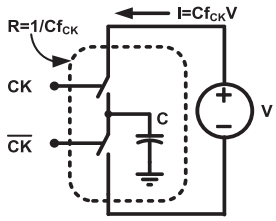


Fig. 3. Frequency-to-current conversion circuit.

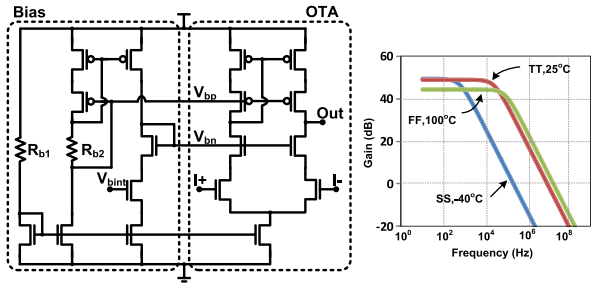


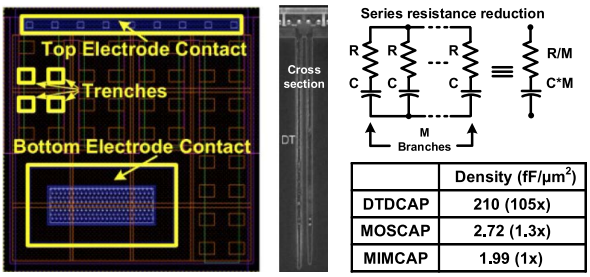
Fig. 4. High-gain OTA schematic and simulated gain plot.

A. Frequecncy-to-Current Conversion

As shown in Fig. 3, frequency-to-current conversion is performed by a switched capacitor resistor combined with a voltage-to-current converter [10] that produces an output current proportional to the input clock frequency. In this design $C_1 = 8$ pF, $C_2 = 1$ pF is used considering the effect of switch parasitic capacitances. Two FTCs are placed together in layout design to minimize process mismatch.

B. High-Gain OTA

Fig. 4 shows the schematic of the high-gain telescopic operational transconductance amplifier (OTA) used in each



	Density (fF/μm²)
DTDCAP	210 (105x)
MOSCAP	2.72 (1.3x)
MIMCAP	1.99 (1x)

Fig. 5. Deep trench capacitor for area reduction.

stage of the frequency synthesizer. The circuit was designed to operate at the nominal supply voltage of 0.9 V. A low voltage internal bias circuit is used to keep every transistor in saturation mode under PVT variations. The input pair operates near the threshold voltage region to achieve maximum gain. The OTA voltage gain varies between 45 dB at fast-fast, 100 °C to 50 dB at slow-slow, and −40 °C in simulation (which is equivalent to only 0.05% output frequency change) while consuming 10 μA of static current.

C. Deep Trench Capacitors

C_{1p} and C_{2p} of 50 and 60 pF, respectively, are used to ensure loop stability. A PLL of comparable bandwidth and output frequency range using the same VCO would require at least a 2-nF loop filter capacitor for a 20-μA charge-pump current [8]. Small capacitors ($<$ 10 pF) are added at V_{1b} and V_{2b} nodes to remove high frequency switching noise. All capacitors (including C_1 and C_2) used in this design are based on deep trench capacitors (dtdcap) available in this process, which are roughly 80X denser than standard MOS capacitors, and hence significantly reduce the area. Due to higher density, two capacitors can be placed very close to each other, providing better matching and reducing parasitics. Leakage current is also lower than MOS capacitors due to the thicker dielectric. Fig. 5 shows a cross-sectional view of the deep trench capacitor [9] along with a 4 × 4 deep-trench array layout. There is a parasitic series resistance associated with each trench capacitor that can be minimized by simply connecting multiple trenches in parallel.

D. Voltage-Controlled Oscillator

The VCO is a five-stage current-starved ring oscillator. The transconductance of this current source is made proportional to N in order to maintain a nearly constant loop gain for a wide output frequency range. However, typical (TT) corner simulation shows 5X change in VCO gain for 10X (16–156 MHz) frequency change due to the large $V_{\rm ctr}$ variation.

IV. Model for Loop Stability Analysis

The small signal model of the current multiplier-based frequency synthesizer is shown in Fig. 6. Only stage 2 is considered here, as the stage 1 operation will not be affected by the output frequency change. Small signal input $(f_{\rm in})$ and output $(f_{\rm out})$ frequencies are represented in terms of equivalent voltages, and FTCs are replaced by voltage-controlled current sources. A(s) denotes the small signal ac gain of the OTA, while G_m denotes the transconductance of the VCO current source, which is made proportional to N (i.e., $G_m = g_m N$), to keep

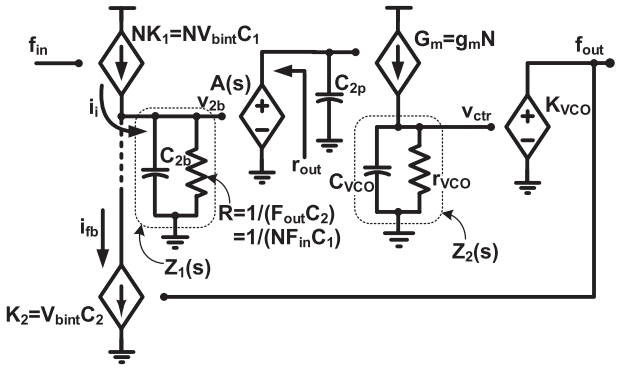


Fig. 6. Equivalent small signal model for loop stability analysis.

the loop gain constant over the entire frequency range. $F_{\rm in}$ and $F_{\rm out}$ are the fixed input and output operating frequencies, respectively. The comparator output's pole is made dominant by adding C_{2p}. The switched capacitor pair is represented by a resistor R with a value of $1/NF_{\rm in}C_1$, which remains nearly constant at a given operating point of small signal analysis. R and C_{2b} [i.e., $Z_1(s)$] will create a nondominant pole. $Z_2(s)$ is the input impedance of the VCO looking from the node $V_{\rm ctr}$. It will also introduce another high frequency nondominant pole. The expressions for the low frequency small signal input current, output frequency, and feedback current are as follows:

$$i_i = NV_{\rm bint}C_1 f_{\rm in}. \tag{2}$$

$$f_{\rm out} = G_m K_{\rm vco} A(s) Z_1(s) Z_2(s) i_i \approx \frac{G_m K_{\rm vco} A(s) r_{\rm VCO}}{NC_1 F_{\rm in}} i_i. \tag{3}$$

$$i_{\rm fb} = V_{\rm bint} C_2 f_{\rm out}. \tag{4}$$

Therefore, the open-loop gain can be calculated as

$$\left.\frac{i_{\rm fb}}{i_i}\right|_{OL} = \frac{V_{\rm bint}C_2 f_{\rm out}}{NV_{\rm bint}C_1 f_{\rm in}} = \frac{C_2}{C_1}\frac{g_m K_{\rm vco} A(s) r_{\rm VCO} V_{\rm bint}}{F_{\rm in}}. \tag{5}$$

If $A(s) = A/(1 + s/\omega_{3\rm dB})$, where $\omega_{3\rm dB}$ is the 3-dB bandwidth of OTA, the close-loop frequency transfer function is given by

$$\left.\frac{f_{\rm out}}{f_{\rm in}}\right|_{CL} = N\frac{C_1}{C_2}\left.\frac{i_{\rm fb}}{i_i}\right|_{CL} = N\frac{C_1}{C_2}\frac{G_0}{1+G_0}\frac{1}{1+\frac{s}{\omega_{3\rm dB}(1+G_0)}}. \tag{6}$$

G_0 is the dc open-loop gain obtained from (5) for $A(s) = A$. $\omega_{3\rm dB}G_0$ is the unity gain bandwidth. The steady-state frequency error can also be calculated as

$$\left.\frac{\Delta f_{\rm out}}{f_{\rm out}}\right|_{s\to 0} \approx \frac{1}{G_0} = \frac{1}{\frac{C_2}{C_1}\frac{g_m K_{\rm vco} A r_{\rm VCO} V_{\rm bint}}{F_{\rm in}}}. \tag{7}$$

Hence, depending on the frequency accuracy requirement, circuit parameters can be tuned. The loop gain and phase response of the model for maximum and minimum operating frequencies are plotted in Fig. 7 showing the phase margin. The loop gain is 65 dB, and the bandwidth varies between 200 and 500 kHz for a frequency variation between 16 and 156 MHz. The transient start-up simulation of the actual circuit is shown in Fig. 8 for an output frequency of 76 MHz. Stage 1 initially takes 5 μs to settle, and stage 2 takes 3.5 μs to reach the desired frequency. The settling time can be reduced further by increasing the loop bandwidth.

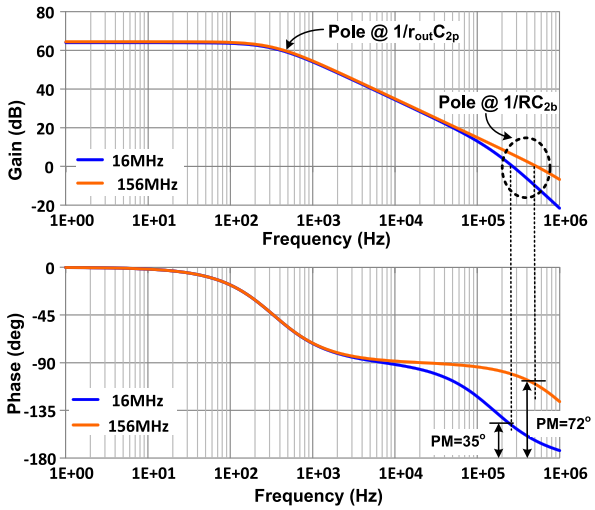


Fig. 7. AC simulation plot of loop model.

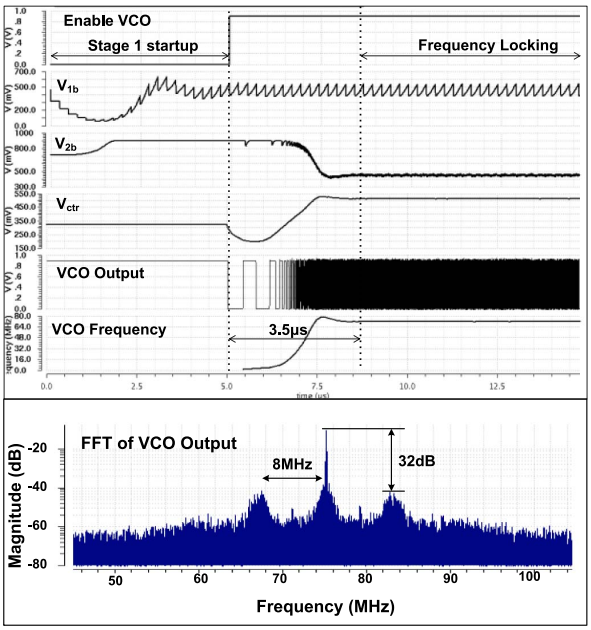


Fig. 8. Frequency synthesizer transient response and output fast Fourier transform (FFT) (simulation).

V. On-Chip Periodic Jitter Measurement Circuit

An on-chip periodic jitter measurement circuit is implemented using the concept of bit error rate (BER) measurement [11]. Fig. 9 shows the proposed jitter measurement circuit. Timing error is detected by the BER monitor when the programmable delay is longer than the instantaneous clock period. A BER plot is obtained by sweeping this delay precisely by changing its supply voltage $V_{\mathrm{DD\_SEP}}$ and calculating the average time period of the divided output clock BER⟨n⟩. Error detection is similar to other on-chip measurement schemes [13]. However, the off-chip time period calculation gives a more accurate BER value, as it is no longer limited to the maximum count of the on-chip counter. The slope of this curve gives the rms periodic jitter (measured BER plot shown later in Fig. 13). The programmable delay is measured by connecting it in ring oscillator fashion (i.e., EN_RO = 1) and measuring its frequency.

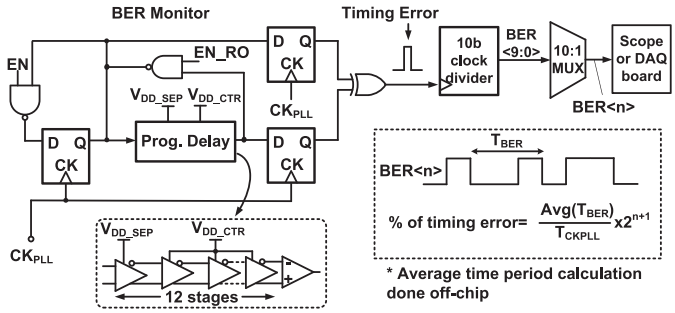


Fig. 9. On-chip periodic jitter measurement circuit [11].

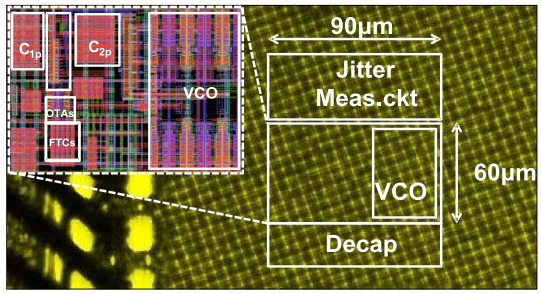


Fig. 10. 32-nm test chip die photograph and core layout.

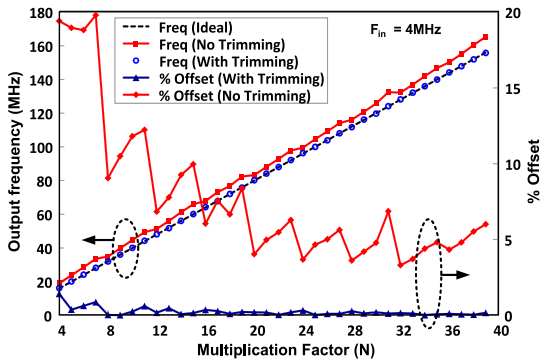


Fig. 11. Process trimming results.

VI. Measurement Results

A test chip is implemented in 0.9-V 32-nm technology to demonstrate the performance of the proposed frequency synthesizer under PVT variations. The die photograph and core layout are shown in Fig. 10, indicating a core area of 0.0054 mm^2. The frequency synthesizer core consumes 116 and 209 μW at 48 and 76 MHz, respectively. The measured output frequencies and corresponding systematic offset are shown in Fig. 11. One time process trimming is required at each frequency point to minimize this systematic offset. The frequency resolution of $F_{\mathrm{in}}/5$, i.e., 0.8 MHz for the 4-MHz input clock, is achieved by precisely controlling the current multiplication factor (N). Fig. 12 compares the measured voltage and temperature dependence of the frequency synthesizer (i.e., close loop) with the free-running open-loop VCO. The close loop shows only a $\pm 0.22\%$ frequency variation compared to the $\pm 13\%$ frequency variation of the free-running oscillator for a 100-mV supply variation. The frequency spread due to temperature sweep from -40 °C to 90 °C is $\pm 0.14\%$, i.e., 21 ppm/°C, for the close loop and $\pm 7\%$, i.e., 1076 ppm/°C, for the open-loop oscillator. The

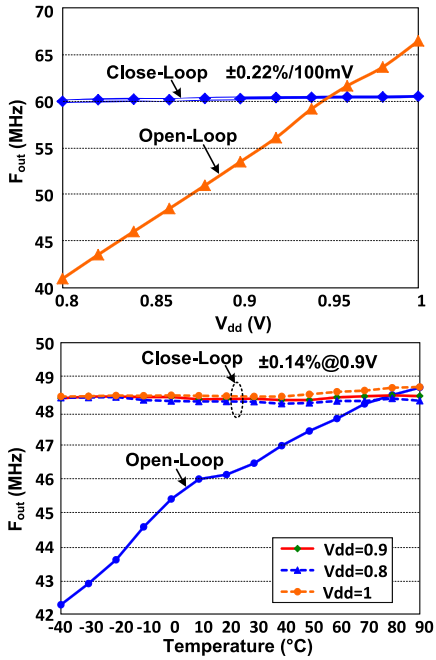


Fig. 12. Measured voltage and temperature dependence.

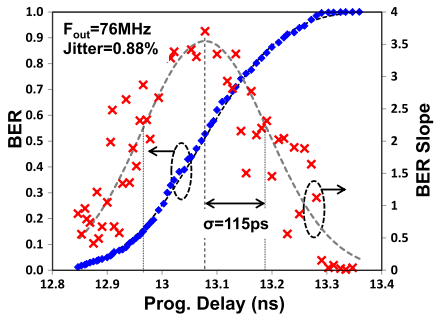


Fig. 13. BER and periodic jitter from on-chip jitter measurement block.

maximum spread is 70 ppm/°C at 150 MHz measured over the entire frequency range. Fig. 13 shows the BER plot and its slope obtained from on-chip jitter measurement circuit at 76 MHz. The first programmable delay is measured for different V_{DD_SEP} and V_{DD_CTR} by connecting the delay in ring oscillator mode. Finally, BER is calculated for different delays. The rms periodic jitter is 115 ps, i.e., 0.88% of the time period, obtained by Gaussian curve fitting on the measured data. Table I compares the performance with other clock generators. The figure of merit (FoM) [6] is 2.4 μW/MHz calculated at 48 MHz. Fig. 14 compares FoM with state-of-the-art on-chip clock generators of comparable frequencies. Four different samples were tested to verify the stability with chip-to-chip variation.

VII. Conclusion

A 16–156 MHz frequency-to-current conversion-based fractional frequency synthesizer is proposed. A 32-nm test chip is fabricated by utilizing a deep trench capacitor to implement the circuit in only 0.0054-mm^2 core area. The measurement result shows the frequency spread of 21 ppm/°C at 48 MHz with a FoM of 2.4 μW/MHz. Periodic jitter measured from an on-chip jitter measurement circuit is 115 ps rms at 76 MHz.

TABLE I
Performance Comparison

Parameters	This Work	Jee ISSCC'13	Ueno ESSCIRC'09	Smedt JSSC'09	Lee VLSI'09
Technique	Freq.-to-Curr. ROSC	Leakage ROSC MDLL	Temp. comp. Resistor	Wienbridge oscillator	Temp. comp. Feedback
Technology	32nm SOI	65nm	0.35µm	65nm	180nm
Frequency	48MHz (16- 156 MHz)	3.2MHz	30MHz (2- 100MHz)	6MHz	10MHz
Ref. Freq.	4MHz	32kHz	-	-	-
Temp. Coefficient	22ppm/°C (-40° to 90°C)	None	90ppm/°C (-40° to 100°C)	86ppm/°C (0° to 100°C)	57ppm/°C (-20° to 120°C)
Voltage Regulation	3.6%/V	None	4%/V	NA	0.06%/V
Start- up Time	8.5µs	~400µs	2.5µs	NA	NA
RMS Period Jitter[%]	1.27%	2.5%*	NA	NA	NA
Power (µW)	116	0.42	180	66	80
FoM (µW/MHz)	2.4	0.132	6	11	8
Chip area (mm^2)	0.0054	0.026	0.08	0.03	0.22

*10kHz to 1MHz integrated rms jitter

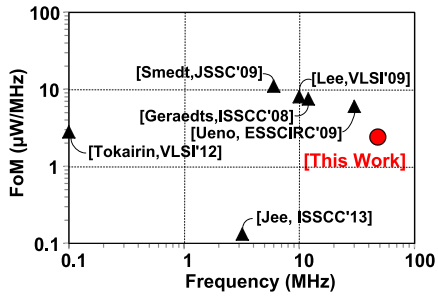


Fig. 14. FoM comparison with other clock generators.

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