A 0.2-to-1.45GHz Subsampling Fractional-N All-Digital MDLL with Zero-Offset Aperture PD-Based Spur Cancellation and In-Situ Timing Mismatch Detection

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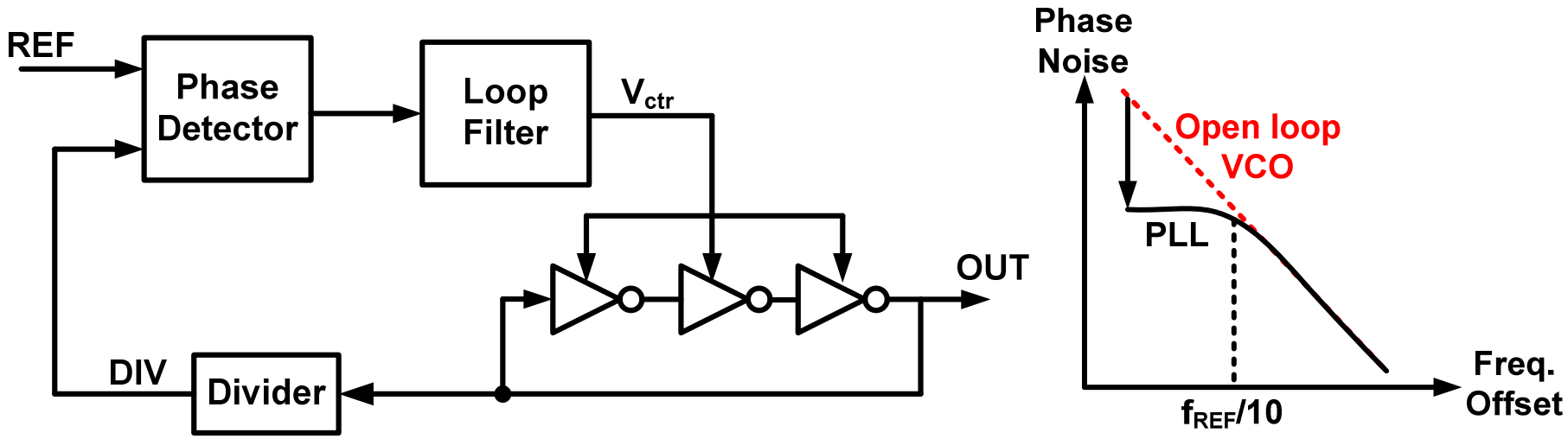
Outline

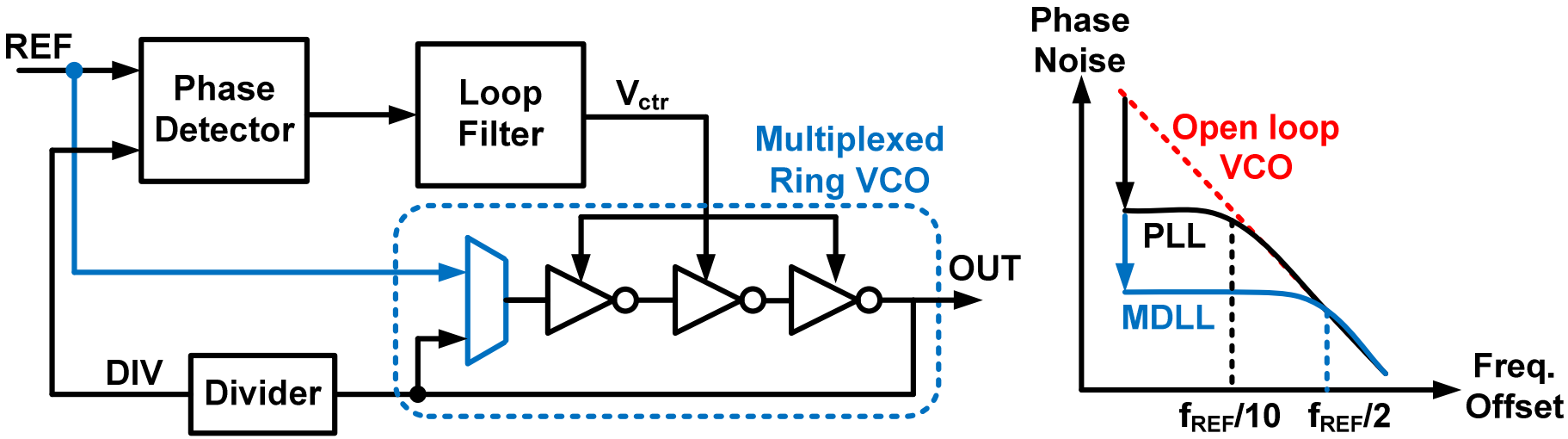
- Background: PLL vs. MDLL
- Reference Spur Cancellation
- In-situ Reference Spur Detection
- 65nm Test Chip Architecture
- Measurement Results
- Conclusion

PLL based Clock Generation



- VCO phase noise is filtered by PLL loop bandwidth
- Maximum PLL bandwidth is roughly $f_{REF}/10$

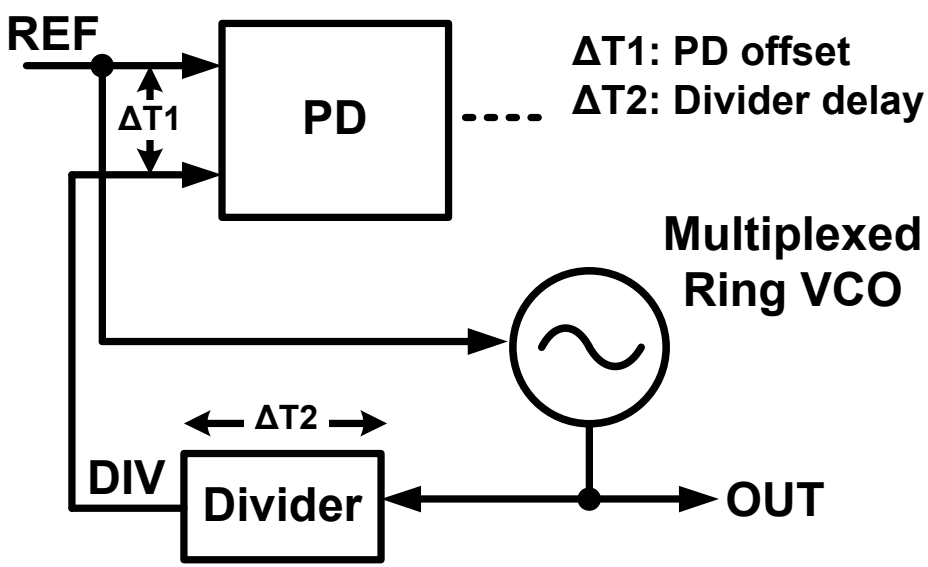
Multiplying DLL (MDLL) based PLL

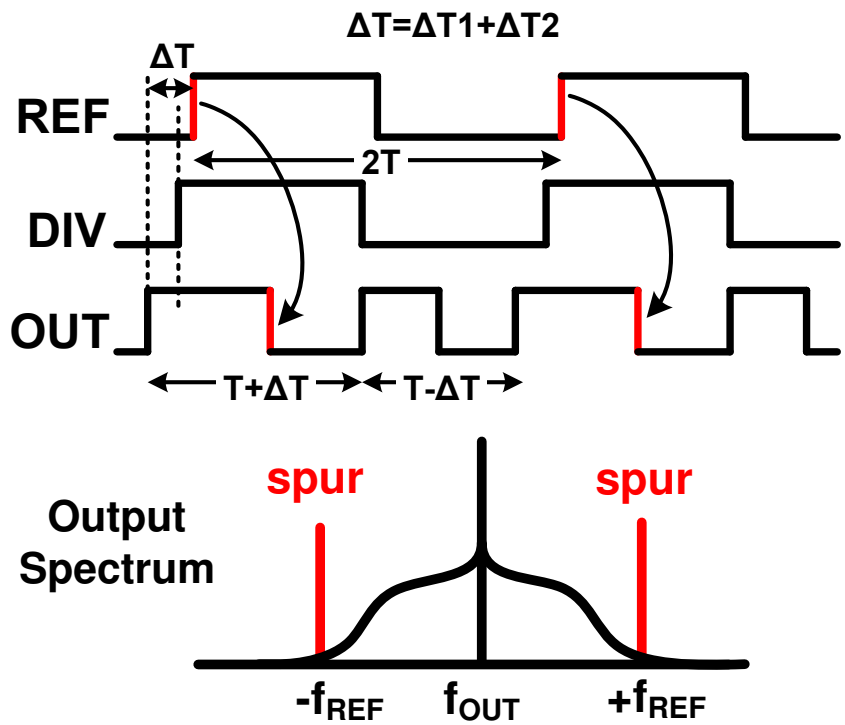


- **VCO phases are periodically replaced by reference phases**
- **Main advantage: Phase noise suppression above the PLL bandwidth**

Ref: S. Ye, et al., JSSC'2000

Reference Spur Issue in MDLL





- **Mismatch in phase detection and reference injection path causes reference spur**
- **Divider delay and phase detector (PD) fixed offset are significant source of mismatch**

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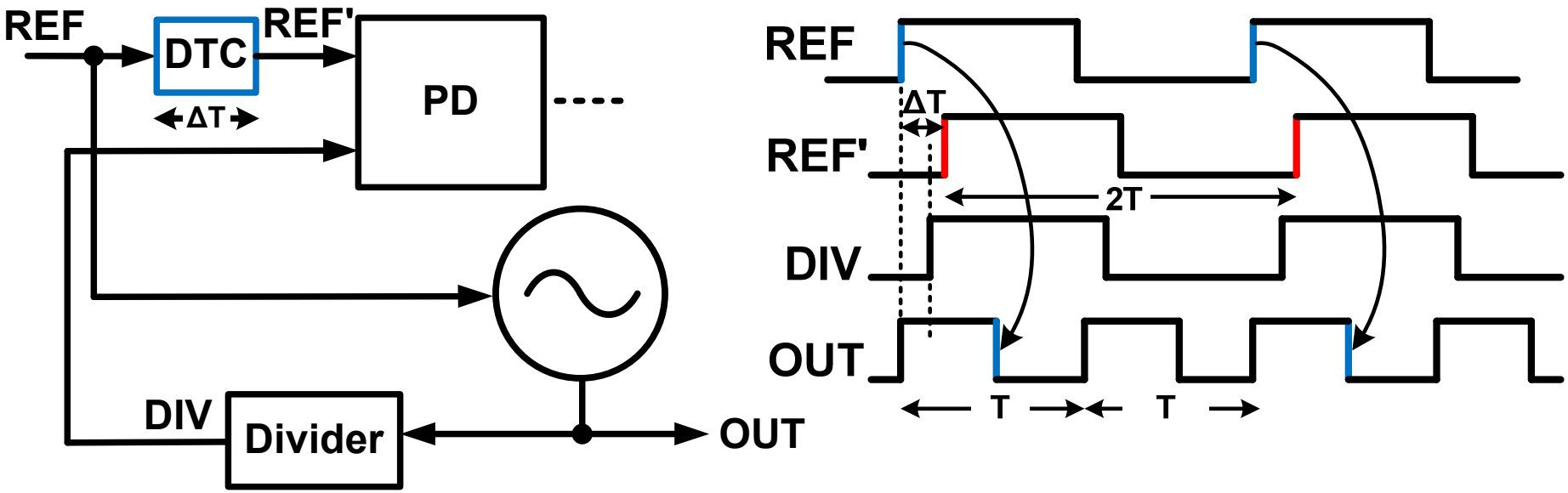
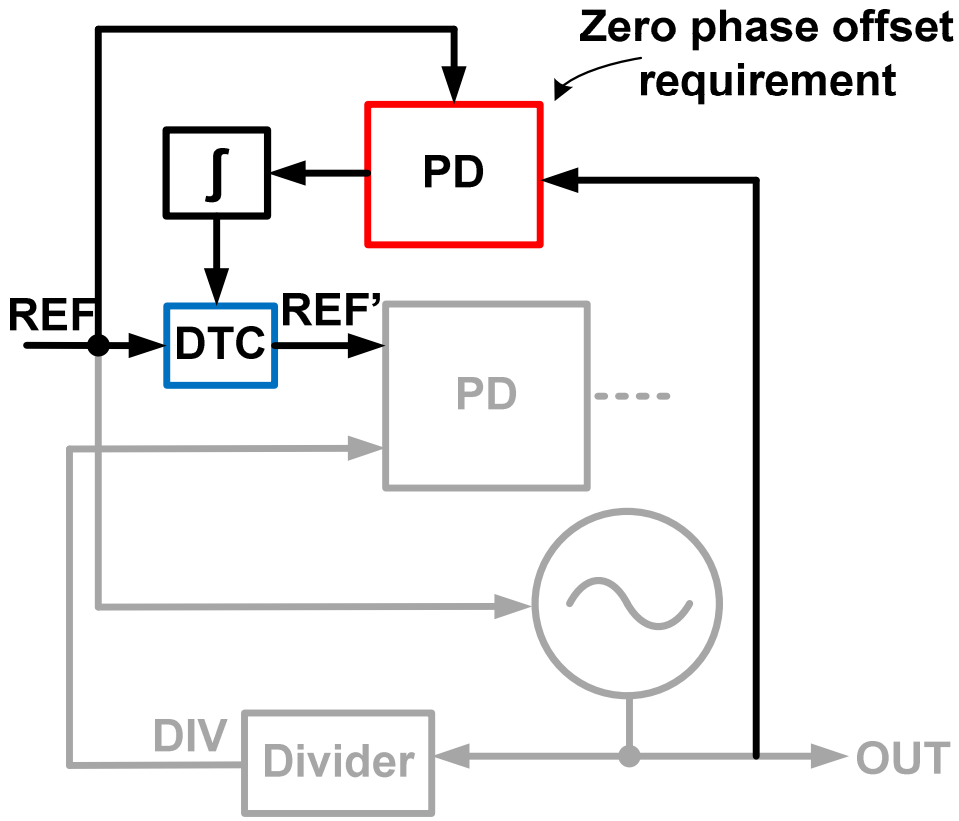
Reference and DCO Phase Realignment



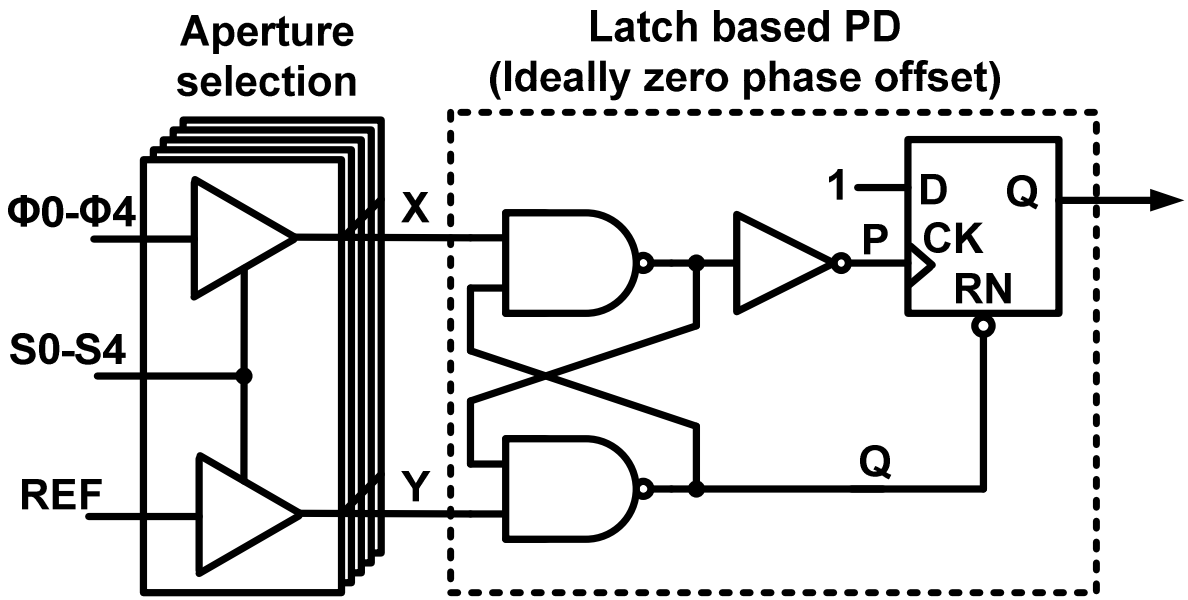
- Additional reference delay in phase detection path cancels spur
- Challenge: Delay should be adjusted and tracked precisely

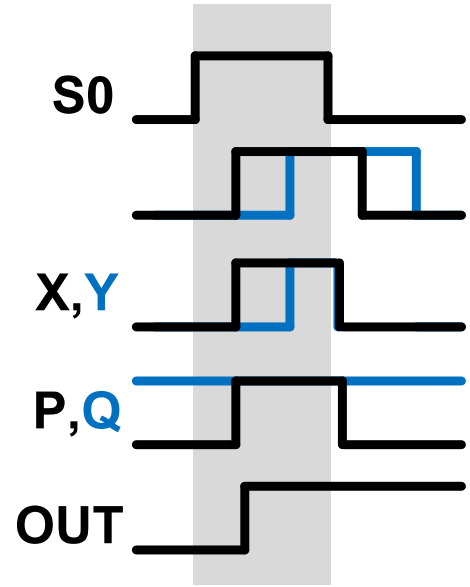
Reference and DCO Phase Realignment



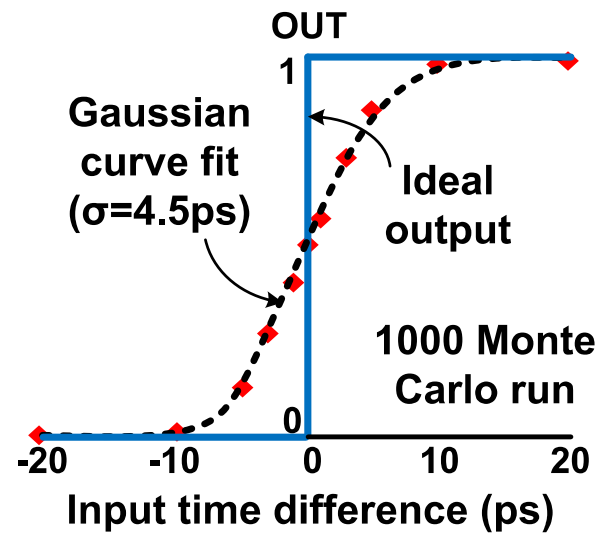
- **Phase detector for reference and DCO phase realignment should have no inherent phase offset**

Zero-offset Aperture Phase Detector





- **Latch based PD has ideally zero phase offset**



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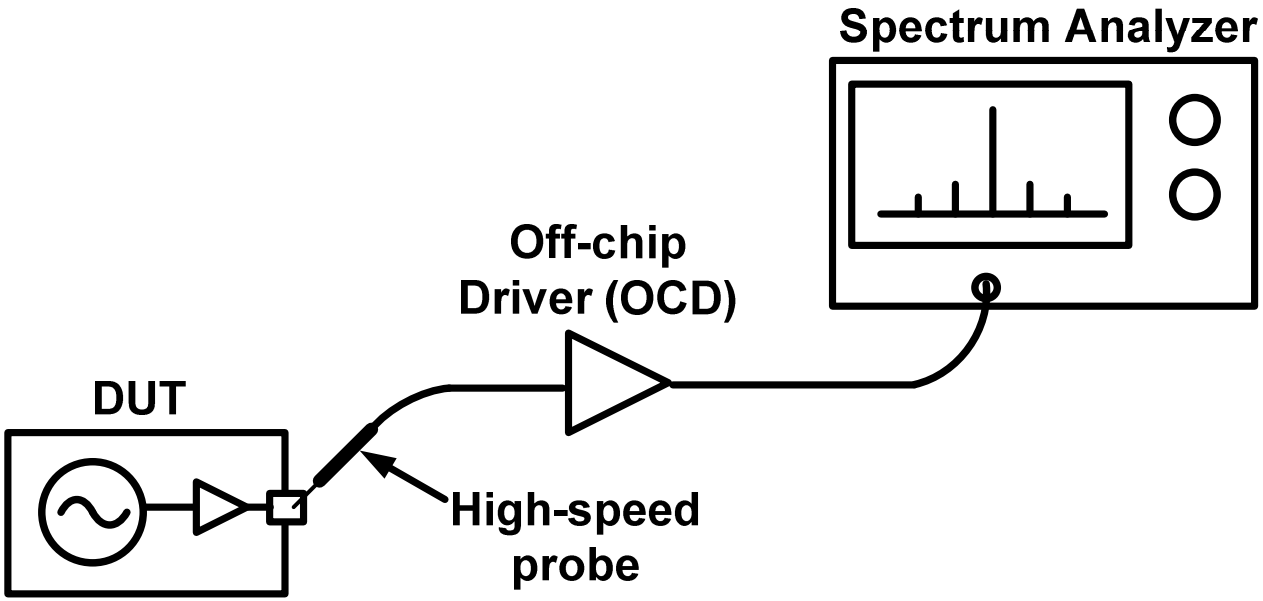
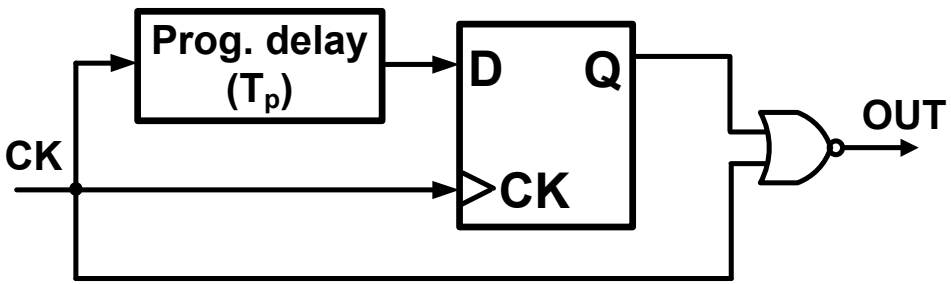
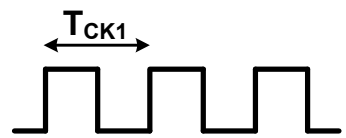
Drawback in Off-chip Measurement

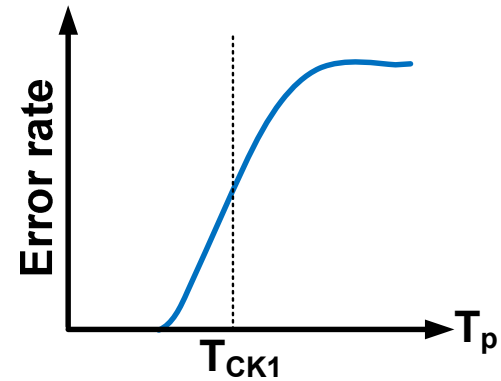


- Requires high frequency probes or packages, off-chip drivers and connectors
- Each of these components introduces inaccuracy in the measurement

Error Rate Calculation



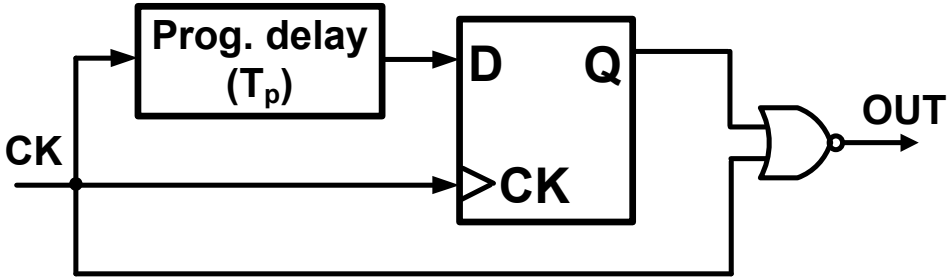




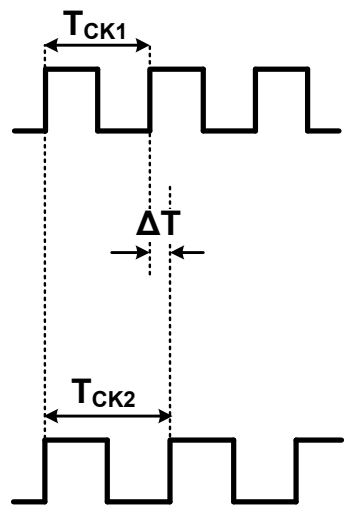
$$\text{Error Rate} = \frac{\text{Avg}(T_{OUT})}{T_{CK}}$$

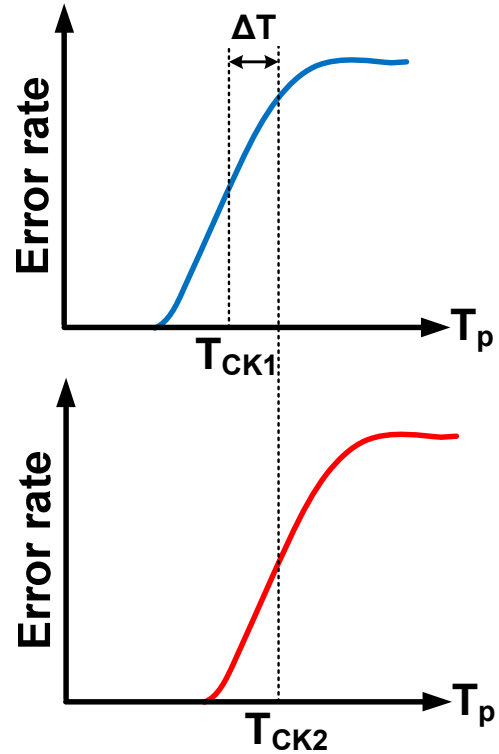
- **Error pulse generated when programmable delay is larger than clock period**

Error Rate Calculation



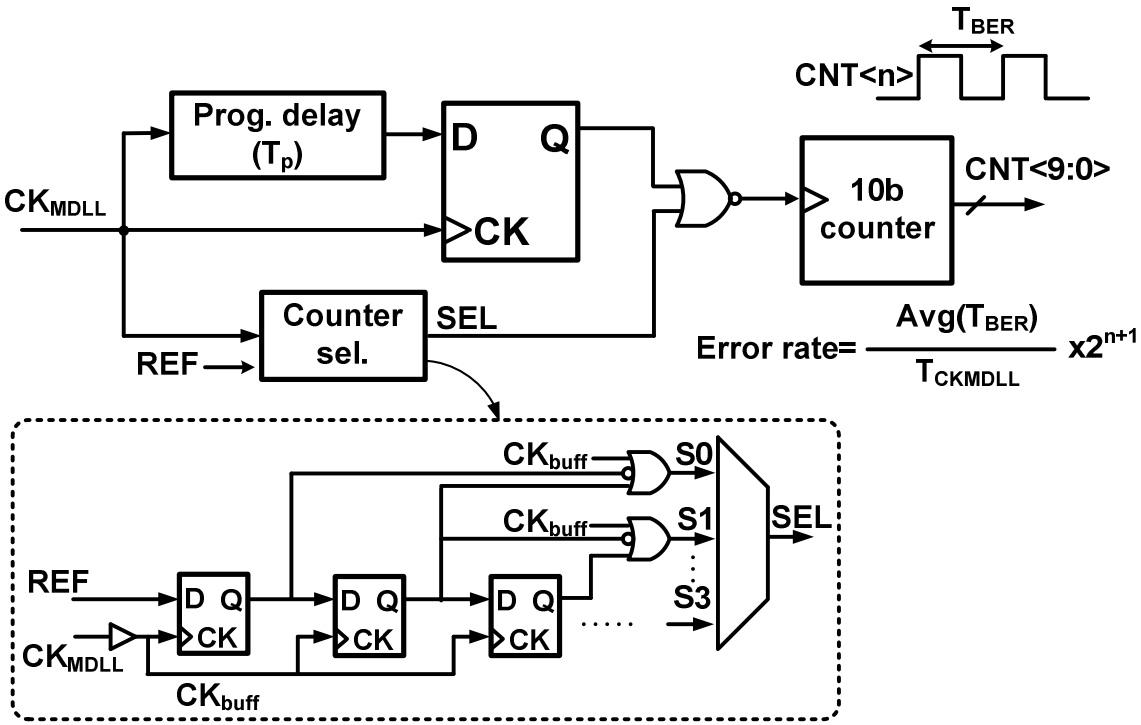
$$\text{Error Rate} = \frac{\text{Avg}(T_{OUT})}{T_{CK}}$$

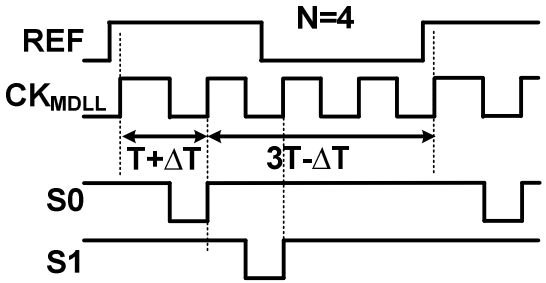




- **Skew between two error rate plot is the time period difference**

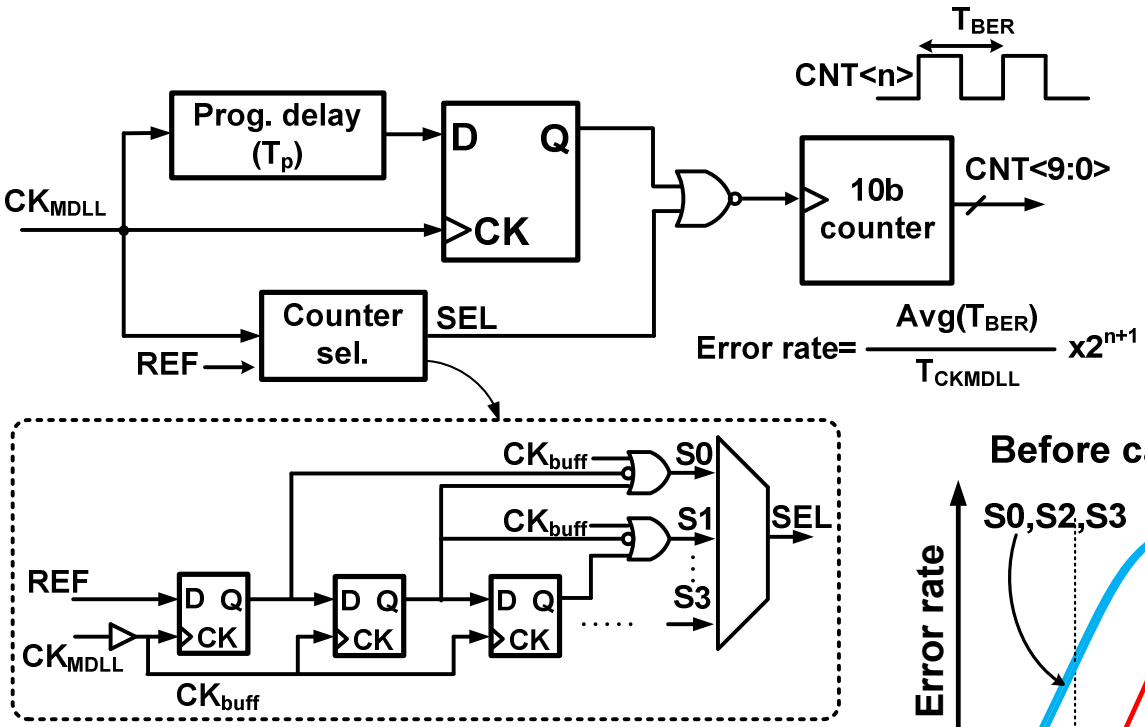
Timing Mismatch Detection from Error Rate Calculation

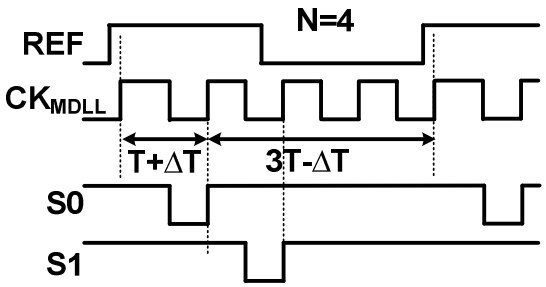


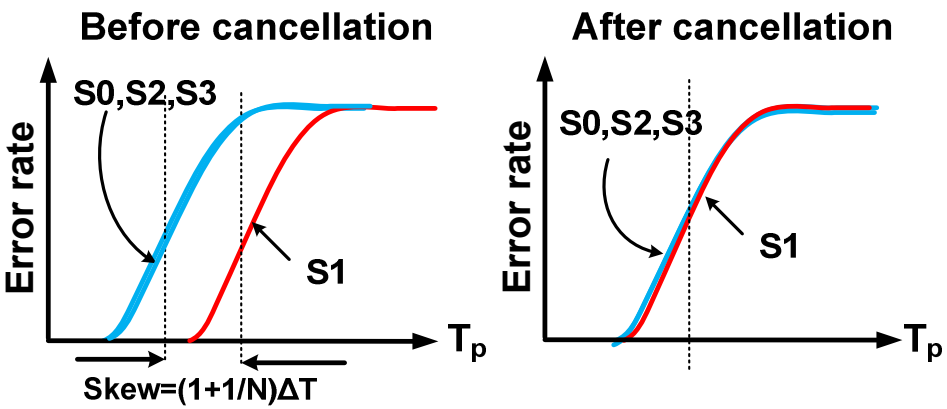


- S0 selects 1st clk period, S1 selects 2nd, and so on
- Error rate is calculated for each selection

Timing Mismatch Detection from Error Rate Calculation







- **In-situ time domain measurement of phase mismatch in MDLL**

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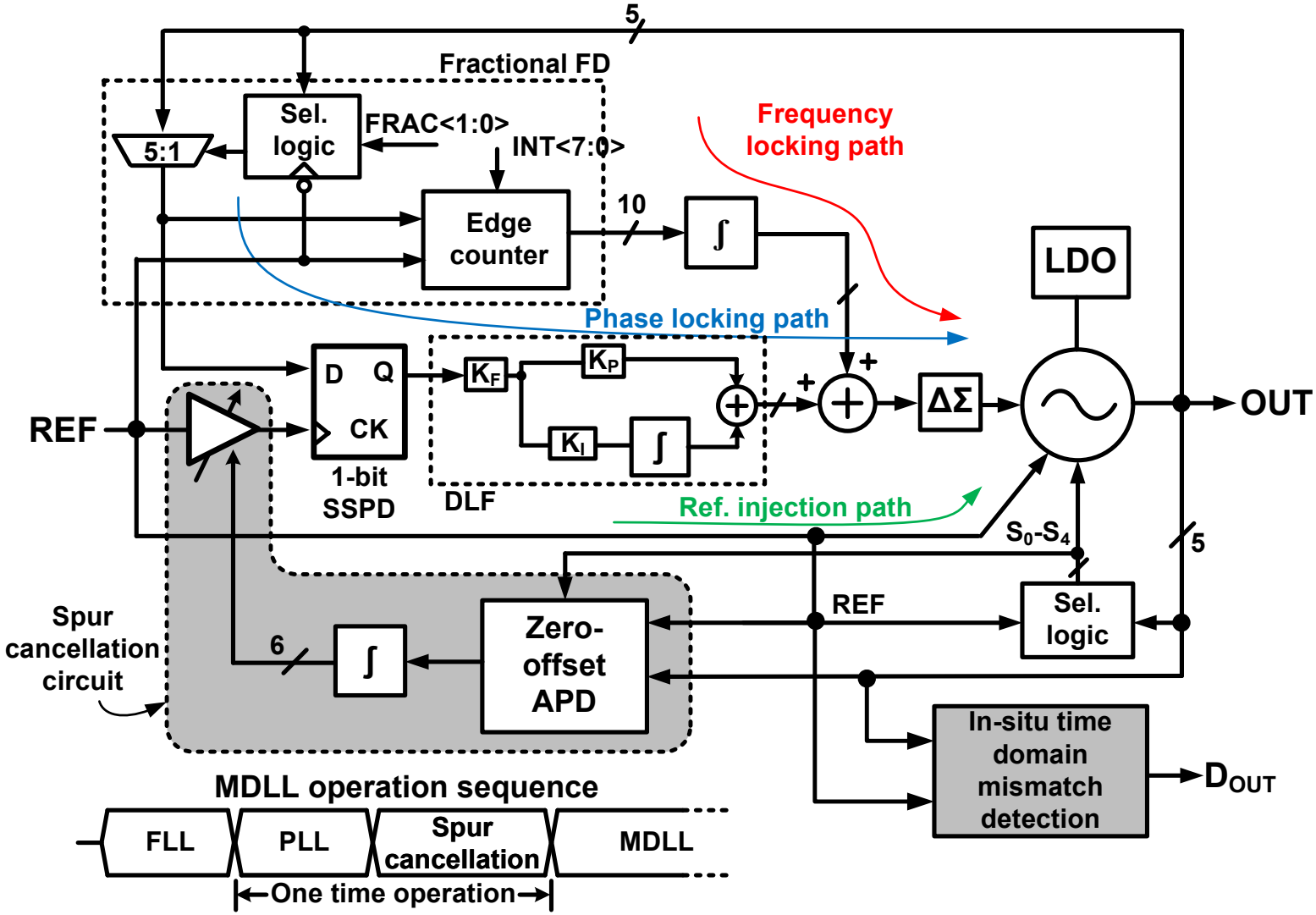
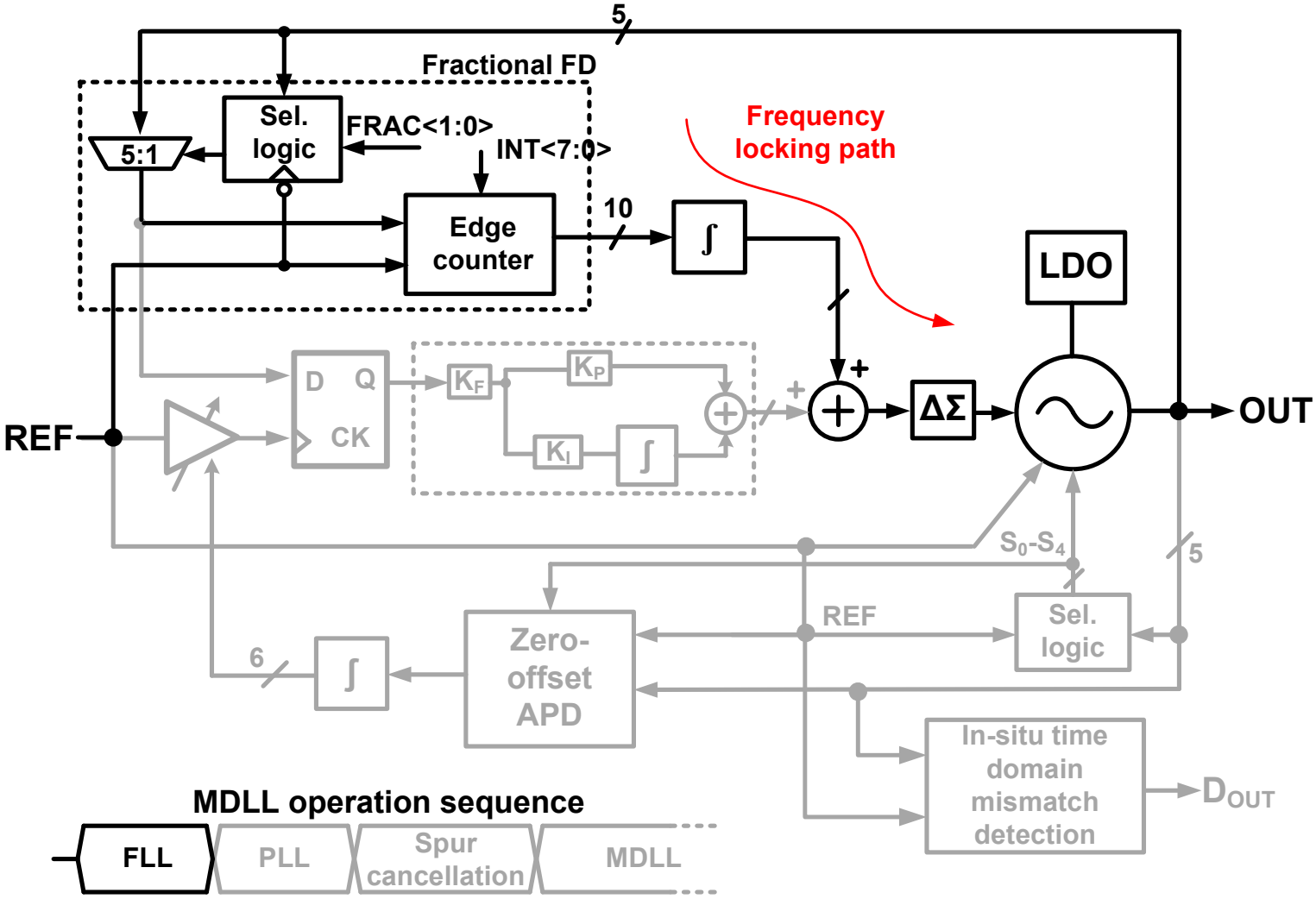
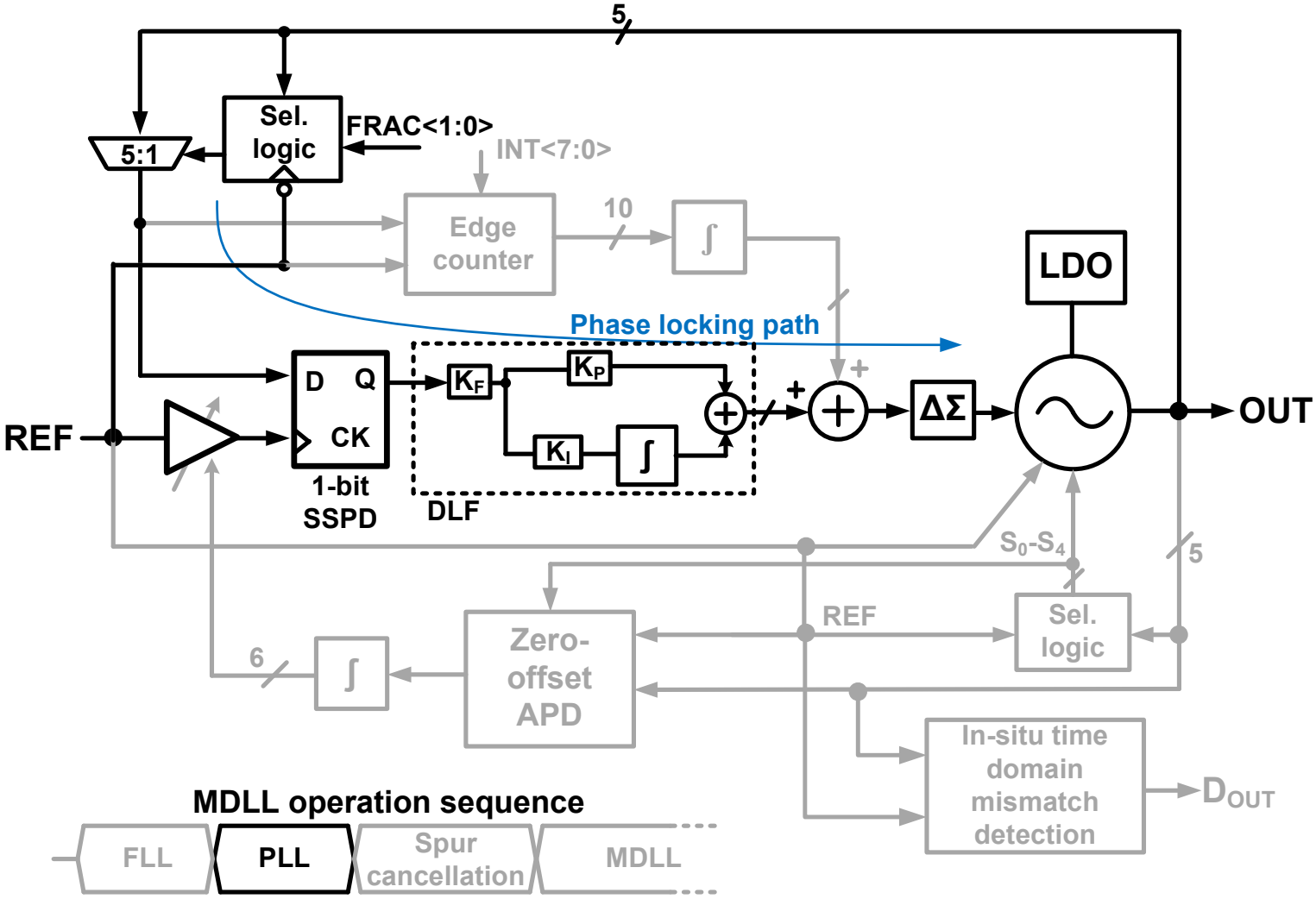
Proposed MDLL Architecture



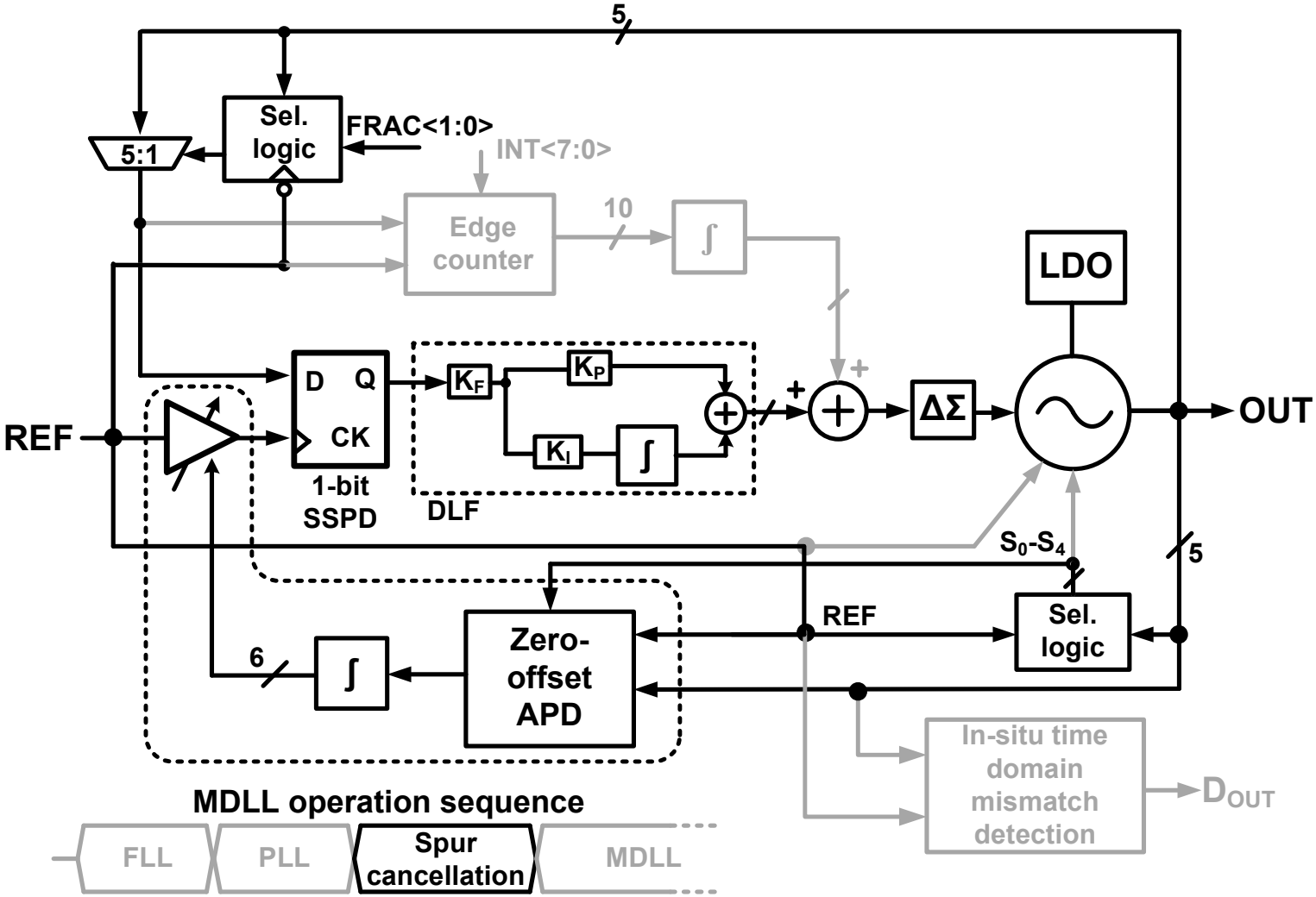
Frequency Locking



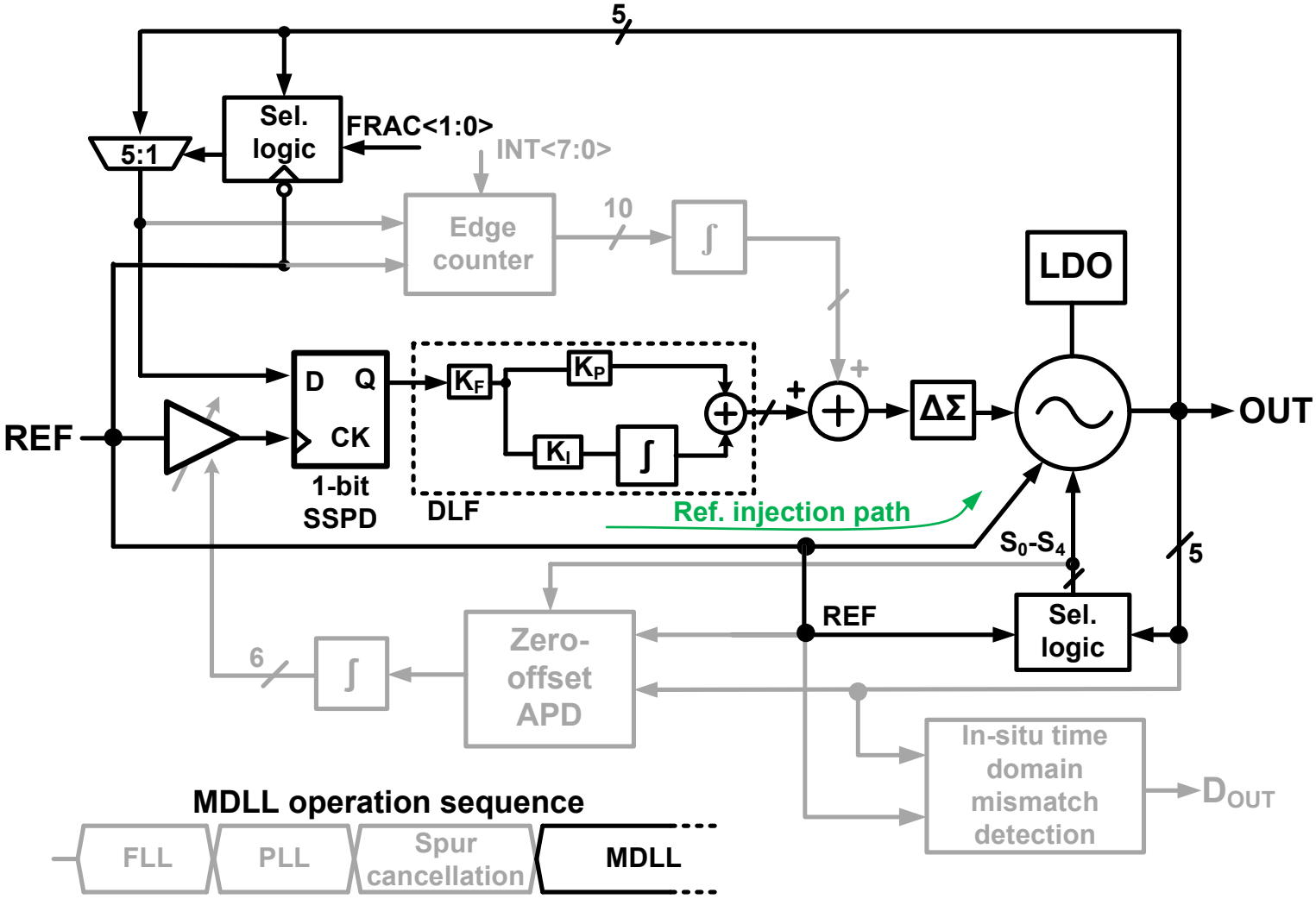
Phase Locking



Spur Cancellation



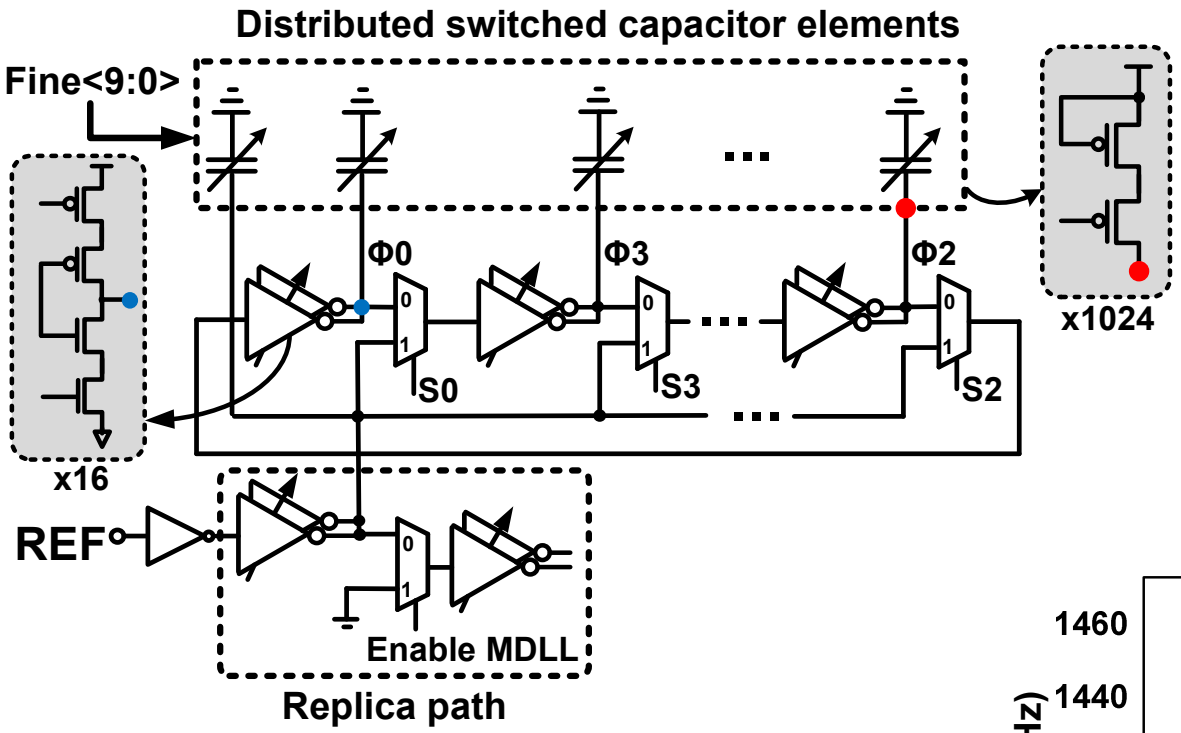
Reference Injection

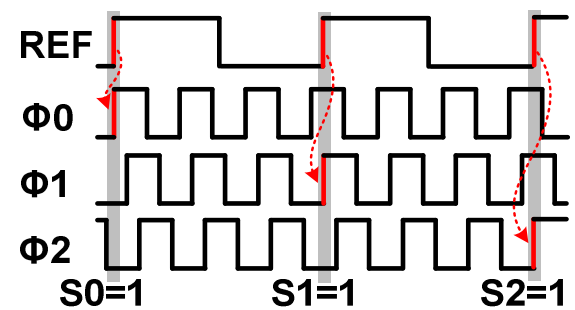


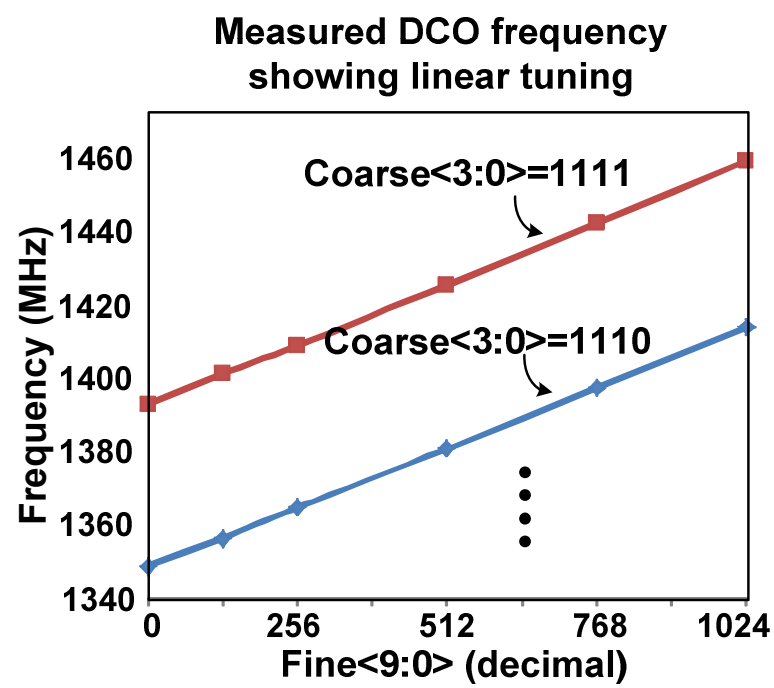
Key Design Features

- **Subsampling 1-bit phase detector for in-band noise reduction**
- **Fractional-N MDLL by periodic rotation of multiple DCO phases**
- **Phase mismatch cancellation loop with zero-offset aperture phase detection**
- **In-situ phase mismatch detection in time domain**

Reference Realigned DCO







- **Replica path matches the rise time of injected reference and DCO phase**

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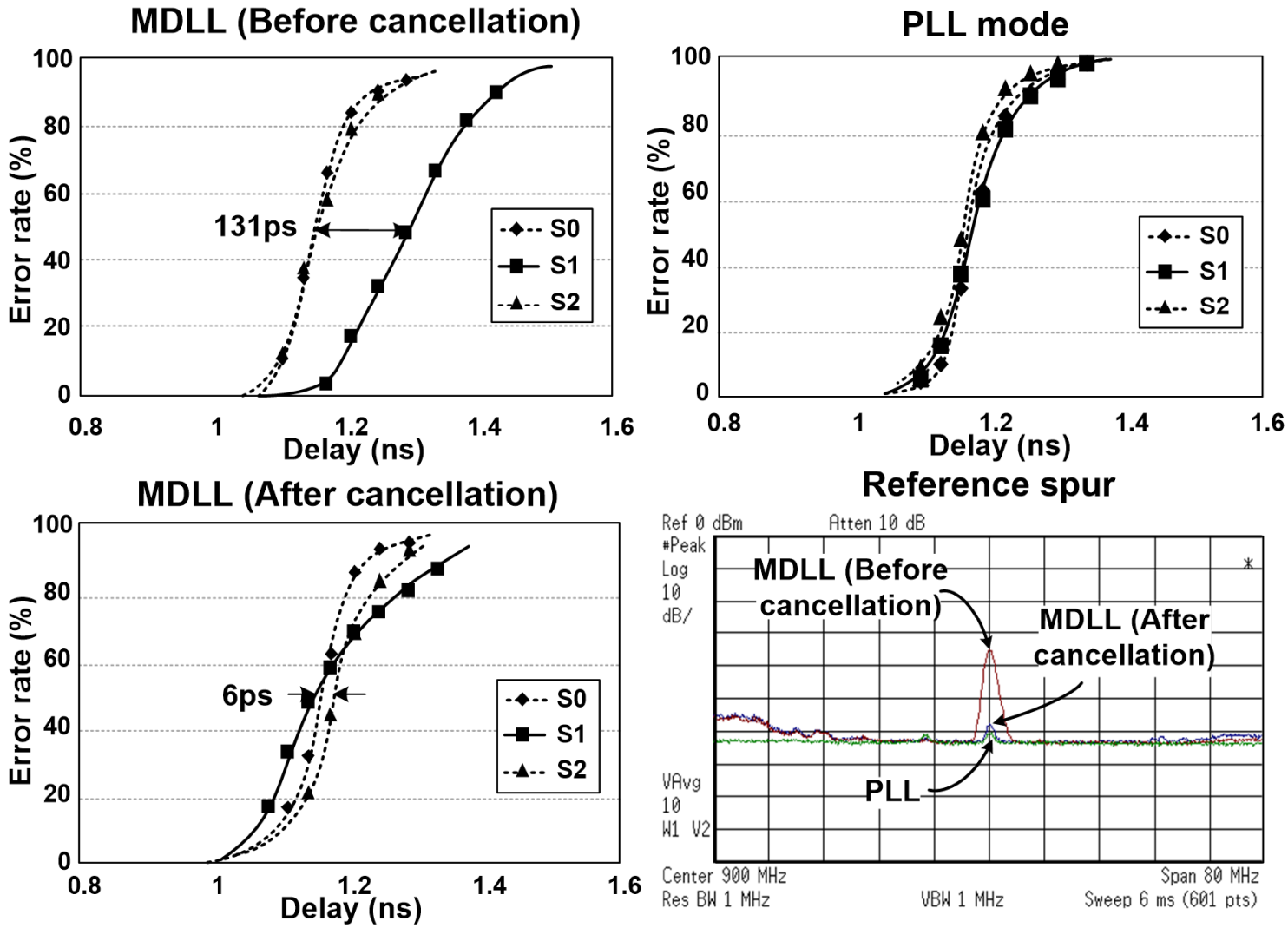
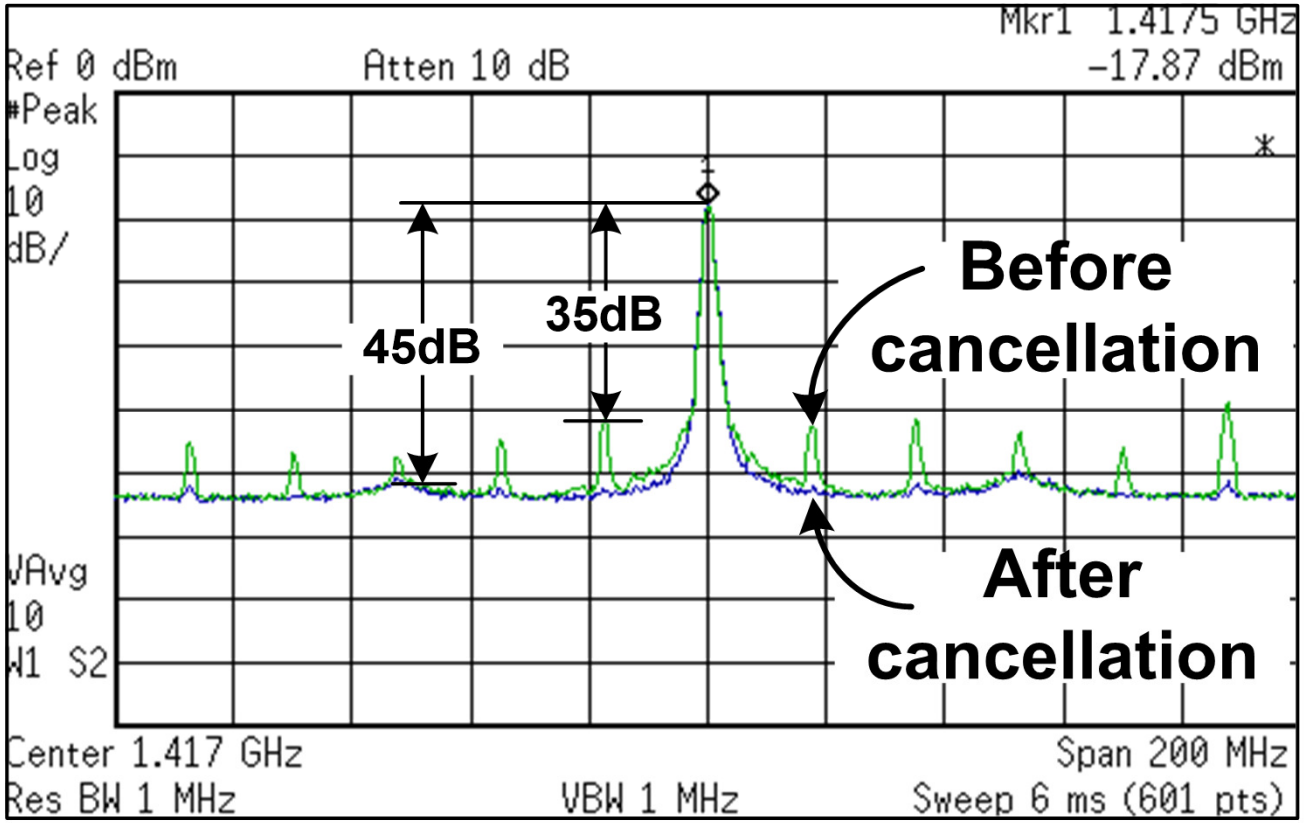
Measured Error Rate for Mismatch Detection



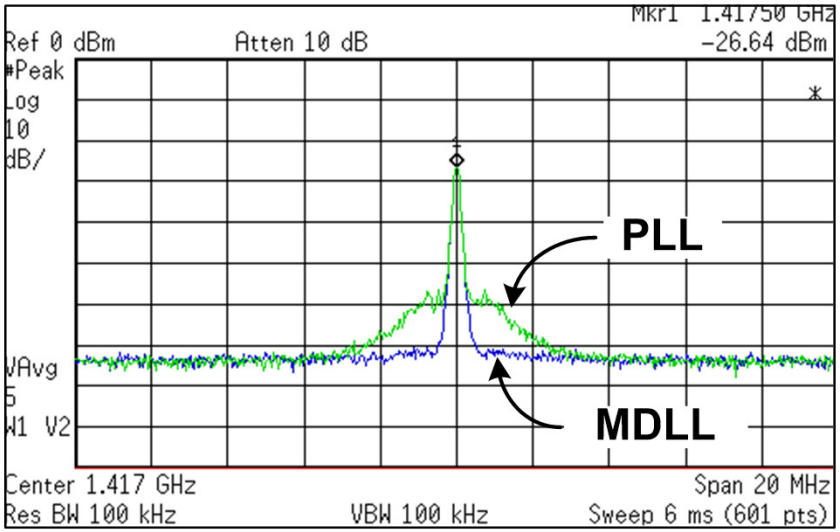
MDLL Fractional Spur



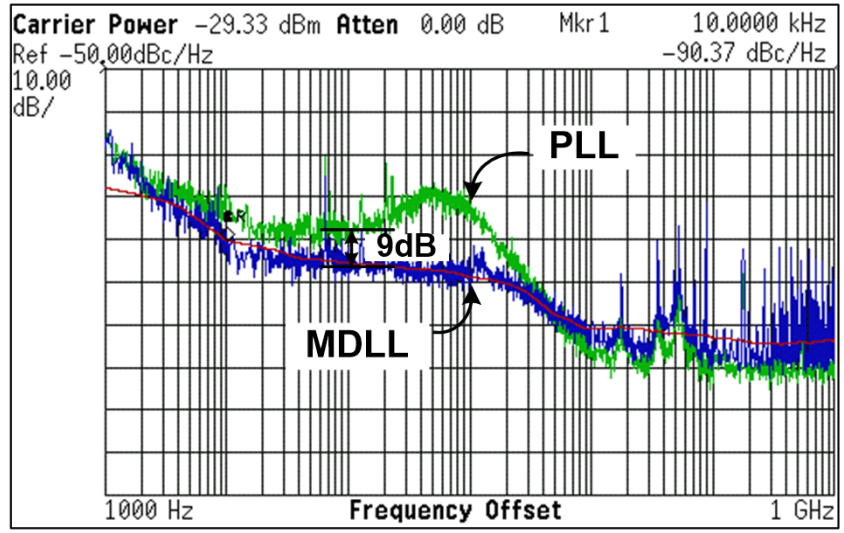
- **Spurs at the multiple of $f_{REF}/5$ are cancelled by the cancellation circuit**

Measured Output Spectrum and Phase Noise

Output Spectrum



Phase Noise



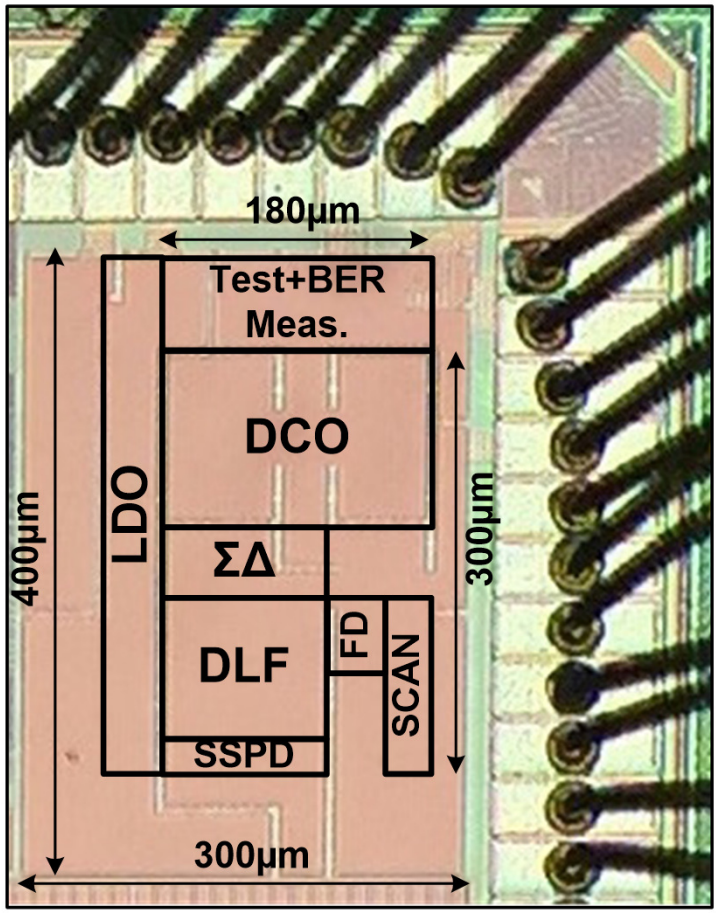
- **Input frequency 87.5MHz, output frequency 1.4175GHz**
- **MDLL shows 9dB lower noise than PLL at 100kHz offset**

Performance Comparison Table

	This Work	[6] ISSCC'15	[1] ISSCC'14	[3] ISSCC'12
Architecture	MDLL	Soft IL-PLL	MDLL	IL-PLL
Process	65nm	65nm	65nm	65nm
Output frequency /Range (GHz)	1.4175 /(0.2–1.45)	1.5222 /(0.8–1.7)	1.651 /(1.6– 1.9)	0.581 /(0.58– 0.611)
Ref. frequency (MHz)	87.5	380	50	32
Power (mW)	8	3	3	10.5
Intg. RMS jitter (ps)	2.8 (0.39%) (10kHz – 10MHz)	3.6 (0.55%) (1kHz – 100MHz)	1.4 (0.23%) (30kHz – 30MHz)	8 (0.46%) (100Hz – 40MHz)
FoM * (dB)	-222	-224	-232	-211
Area (mm^2)	0.054	0.048	0.4	0.083

*FoM=20log(σ/1s)+10log(P/1mW)

Die Photo and Result Summary



		PLL	MDLL
Technology		CMOS 65nm, 1.2V	
Output frequency		Integer: 1.4GHz Fraction: 1.4175GHz	
Frequency range		0.2–1.45 GHz	
DCO type		5-stage ring oscillator	
In-band PN (dBc/Hz @100kHz)	Integer	-92	-108
	Fraction	-87	-96
Integ. RMS jitter (10kHz-10MHz)	Integer	8.1ps	2ps
	Fraction	11.7ps	2.8ps
Power (mW)	DCO	4.5	
	Total	8.0	
FOM (dB)	Integer	-212.8	-225
	Fraction	-209	-222
Area	Core	180µm x 300µm	
	Total	300µm x 400µm	

Conclusion

- **Subsampling fractional-N all-digital MDLL designed in 65nm CMOS**
- **Zero-offset aperture phase detector based spur cancellation circuit is implemented for reference and DCO phase alignment**
- **First in-situ detection circuit to measure the mismatch between reference and DCO phase in time domain**
- **MDLL measurement result shows 9dB lower phase noise than PLL at 100kHz offset**