19.2 A 0.2-to-1.45GHz Subsampling Fractional-N All-Digital MDLL with Zero-Offset Aperture PD-Based Spur Cancellation and In-Situ Timing Mismatch Detection

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Multiplying delay-locked loops (MDLLs) are gaining popularity due to their superior noise performance over conventional phase-locked loops (PLLs) [1,2]. Recent designs are trending towards an all-digital implementation that provides advantages such as compact area, good scalability and low power compared to traditional analog implementations. Achieving fractional frequency multiplication is, however, not very straightforward in MDLLs as the digitally controlled oscillator's (DCO's) edge is periodically replaced by a clean reference edge. Recently, a fractional-N MDLL was proposed in [1], where the reference edges are realigned using a digital-to-time converter (DTC). One major drawback of MDLL-based frequency synthesis is that the reference spur is generated at the output spectrum due to the timing mismatch between the phase detection path and reference injection path. One of the contributors to this timing mismatch in fully digital MDLLs is the set-up time of the D flip-flop used for phase detection that creates a static phase-offset between the DCO and reference phase under locked condition. It is very difficult to accurately cancel this offset as any digital phase-detector (PD) or time-to-digital converter (TDC) used for cancellation will have an inherent offset. A spur cancellation technique was proposed in [2] employing a gated ring oscillator (GRO)-based TDC. However, it relies on correlated-double-sampling and requires a high-resolution high-linearity TDC, which increases design complexity and power consumption. Another shortcoming of previous designs is that the timing mismatch measurement was done by looking at the spur in the output spectrum using an extensive high frequency measurement setup. This introduces off-chip measurement error and makes in-situ timing compensation schemes infeasible without a sophisticated testing setup. Furthermore, the frequency domain data must be converted to time domain, which makes it difficult to accurately estimate the exact timing mismatch. This paper proposes an all-digital fractional-N MDLL circuit where fractional-N generation is similar to the injection locking technique proposed in [3], but the advantages of subsampling techniques are utilized, hence removing the frequency divider in the feedback path. This reduces in-band phase noise and lowers power consumption. The same circuit can operate in either MDLL or PLL mode depending on the design requirement. A zero-phase-offset latch-based aperture phase-detector (APD) is designed to match the reference injection path and phase detection path precisely and thereby cancel the spur. Finally, we employ an in-situ timing detection scheme MDLL that directly measures the timing mismatch between the injected reference edge and different DCO edges, providing accurate time-domain data for MDLL characterization and tuning purposes.

Figure 19.2.1 shows the top-level block diagram of the proposed MDLL. The frequency locking path locks the frequency of the DCO first for subsampling operation. It consists of an edge counter-based fractional-frequency detector (FD) and an integrator. A selection logic block in the fractional FD selects different phases of the DCO periodically without creating a glitch to achieve the desired fractional frequency ratio set by external codes INT<7:0> and FRAC<1:0>. Once the frequency is locked, this path is disabled, turning on the phase-locking path. A simple D flip-flop is used here as a 1b subsampling phase-detector (SSPD). A latch-based APD along with a digital integrator and a DTC form the spur cancellation circuit. A 6b DTC code is adjusted based on the decision made by the APD. This loop can operate only once or can continuously adjust the DTC delay variation due to temperature change. Phase locking is performed before spur cancellation to bring the reference and DCO rising edges within the operation time window of the APD (i.e. when any one of S0-S4=1). Once the DTC codes settle and cancel the spur, the reference injection path is turned on for the final MDLL operation. The in-situ time-domain detection block is used to detect the timing mismatch before and after spur cancellation to measure the accuracy of the cancellation circuit.

Figure 19.2.2 (top) shows the zero-offset APD circuit, which adjusts the delay in the reference phase detection path to align the DCO feedback and reference injection paths. The aperture window is selected by S0-S4. One of these is ON for a small duration to capture the rising edges of reference and appropriate DCO phase, once in every reference cycle. Zero-offset phase detection is performed by an SR-latch followed by a D flip-flop that stores the detected value for the reference period. The timing diagram shows the instantaneous voltage at each node of the APD for an input sequence. Since perfect timing alignment happens under the nominal condition, and process mismatch can introduce some phase offset in the latch, we run Monte-Carlo mismatch simulation by sweeping the time difference between two input edges and calculating the fraction times the output is 1. The simulated RMS phase offset is 4.5ps. The reference-realigned DCO used for MDLL operation is shown in Fig. 19.2.2 (bottom). As the fraction generation is performed by periodic DCO phase rotation, a MUX is introduced in every stage that replaces the appropriate DCO phase with reference. The same signals (S0-S4) that enable the APD are also used here for MUX selection. 10b binary-weighted switched capacitor branches tune the DCO frequency. All 1024 branches are distributed uniformly among the 5-inverter stages [4] for good linearity. The fully symmetric DCO layout minimizes process variation. Measurement results (Fig. 19.2.2, right) also verify highly linear frequency tuning. A replica path matches injected reference rise time with the DCO internal phases for accurate mismatch detection at the APD irrespective of the mismatch in threshold crossing of APD input and DCO inverter stages.

Figure 19.2.3 illustrates the implementation of the in-situ time-domain mismatch detection block. When the programmable delay (T_p) is increased, an error pulse (Error_out) is generated by the NOR gate which increments a 10b counter. A transition in the n^{th} bit of the counter output CNT<9:0> indicates 2^{n+1} errors. By measuring the average period of the counter output and the clock frequency, error rate can be conveniently calculated [5]. Finally, an error rate plot for each MDLL clock cycle can be obtained by varying T_p. In the MDLL, only the first clock cycle in every reference period has a different time period than others, due to the timing mismatch. Counter selection logic selects a particular MDLL clock cycle for error rate measurements. For example, S0 selects the first cycle in every reference period calculating the error of its previous cycle and so on. Therefore, the error plot corresponding to S1 selection, which calculates the error rate of first cycle, will be slightly skewed relative to the others (i.e. S0, S2-S7). A ΔT timing mismatch between the reference and DCO phase generates $(1+1/N)\ \Delta T$ skew in the error plot for the N times frequency multiplying MDLL. T_p is calculated by connecting it in ring oscillator configuration (EN_RO=1) and measuring its frequency.

A test chip, implemented in a 1.2V, 65nm CMOS process, covers an output frequency range of 0.2-1.45GHz, occupying a core area of 0.054mm^2. Fig. 19.2.4 shows the measurement results from the on-chip mismatch detection block at 800MHz with 100MHz input. An error plot of first three clock cycles in a reference period (S0, S1, S2) are shown. As expected, before spur cancellation, the error plot for S1 is skewed by 131ps that corresponds to 116ps timing mismatch. After spur cancellation, S1 aligns with others, reducing the skew to only 6ps. An error plot in PLL mode is also shown and all results are compared with measured frequency-domain reference spur.

Figure 19.2.5 shows the output spectrum showing the spur cancellation and phase noise at 1.4175GHz (N=16.2). Integrated RMS jitter (from 10kHz to 10MHz) is 2.8ps. Phase noise at 100kHz offset is -95dBc/Hz, which is 9dB lower than in PLL mode. Core power consumption is 8mW of which the DCO consumes 4.5mW. Fig. 19.2.6 compares the performance with state-of-the-art inductor-less fractional-N frequency synthesizers. Fig. 19.2.7 shows the die photo and summarizes the performance for both the MDLL and PLL modes.

References:

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[2] B. Helal et al., "A low jitter 1.6 GHz multiplying DLL utilizing a scrambling time-to-digital converter and digital correlation," *IEEE Symp. VLSI Circuits*, pp. 166-167, 2007.

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[4] N. August et al., "A TDC-Less ADPLL with 200-to-3200MHz Range and 3mW Power Dissipation for Mobile SoC Clocking in 22nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 246-247, 2012.

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[6] W. Deng et al., "A 0.048mm^2 3mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique," *ISSCC Dig. Tech. Papers*, pp. 252-253, 2015.

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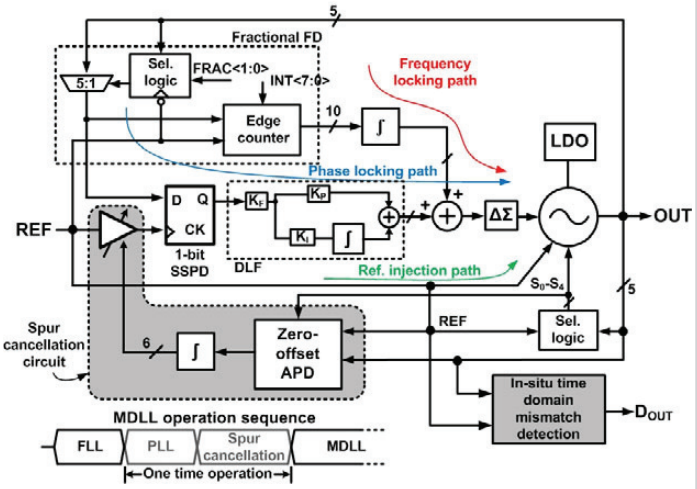

Figure 19.2.1: Block diagram of the fractional-N subsampling MDLL with proposed zero-offset APD-based spur cancellation and in-situ time-domain mismatch-detection circuit.

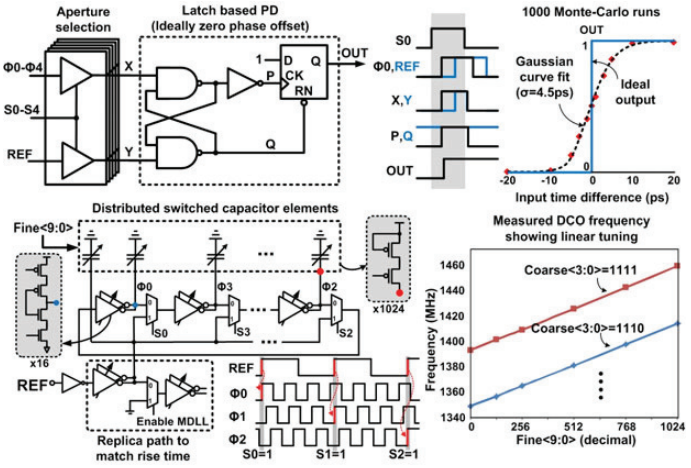

Figure 19.2.2: Zero-offset latch-based phase detector (top); reference realigned DCO with distributed switched capacitors for linear tuning (bottom).

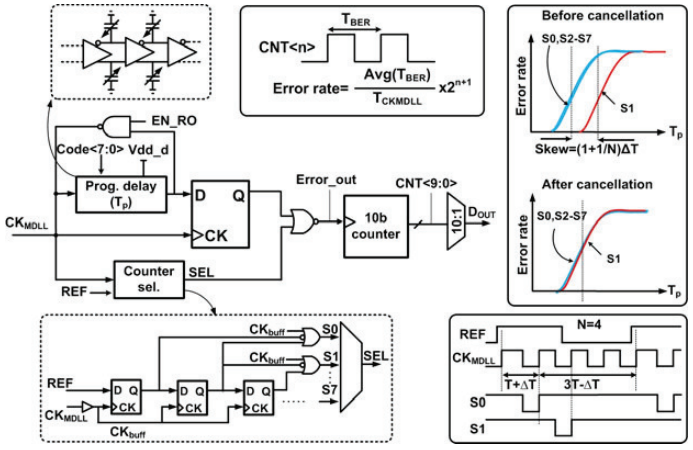

Figure 19.2.3: Proposed in-situ detection circuit to measure the timing mismatch between reference injection and phase detection path.

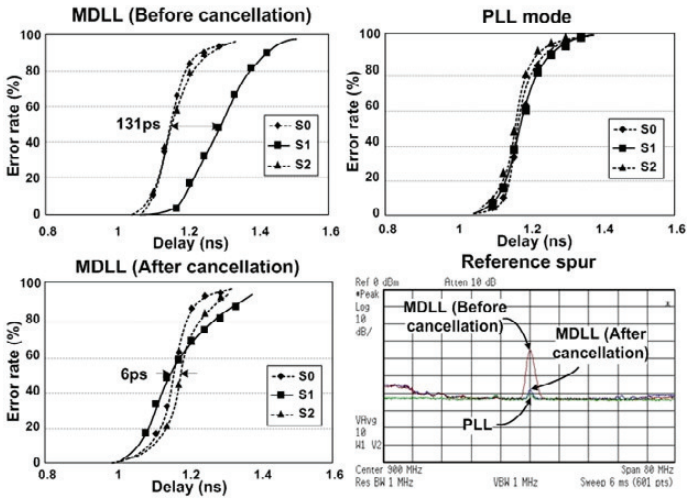

Figure 19.2.4: Measured error rate using the in-situ timing mismatch detection circuit (in MDLL mode before and after spur cancellation, and in PLL mode). PLL and reference spur for an 800MHz clock using a 100MHz reference.

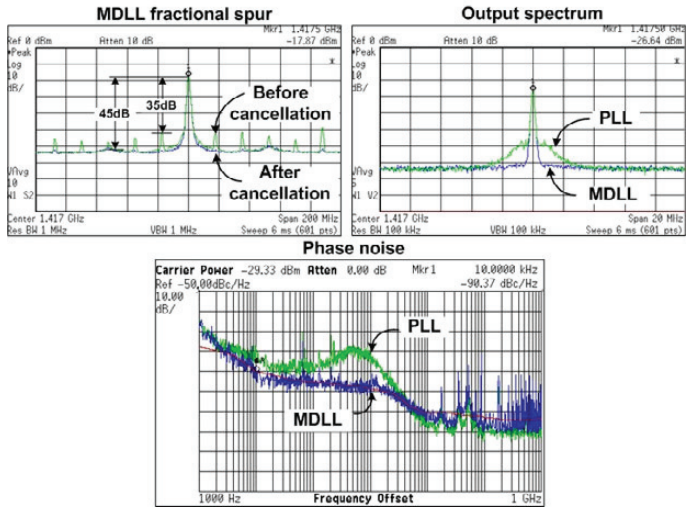

Figure 19.2.5: Output spectrum and phase noise at 1.4175GHz (N=16.2).

	This Work	[6] ISSCC'15	[1] ISSCC'14	[3] ISSCC'12
Architecture	MDLL	Soft IL-PLL	MDLL	IL-PLL
Process	65nm	65nm	65nm	65nm
Output frequency /Range (GHz)	1.4175 /(0.2–1.45)	1.5222 /(0.8–1.7)	1.651 /(1.6–1.9)	0.581 /(0.58– 0.611)
Ref. frequency (MHz)	87.5	380	50	32
Power (mW)	8	3	3	10.5
Intg. RMS jitter (ps)	2.8 (0.39%) (10kHz – 10MHz)	3.6 (0.55%) (1kHz – 100MHz)	1.4 (0.23%) (30kHz – 30MHz)	8 (0.46%) (100Hz – 40MHz)
FoM * (dB)	-222	-224	-232	-211
Area (mm^2)	0.054	0.048	0.4	0.083

*FoM=20log(σ/1s)+10log(P/1mW)

Figure 19.2.6: Performance comparison with other state-of-the-art fractional-N inductor-less frequency synthesizers.

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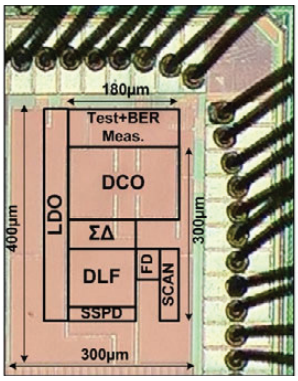

		PLL	MDLL
Technology		CMOS 65nm, 1.2V	
Output frequency		Integer: 1.4GHz Fraction: 1.4175GHz	
Frequency range		0.2–1.45 GHz	
DCO type		5-stage ring oscillator	
In-band PN (dBc/Hz @100kHz)	Integer	-92	-108
	Fraction	-87	-96
Integ. RMS jitter (10kHz-10MHz)	Integer	8.1ps	2ps
	Fraction	11.7ps	2.8ps
Power (mW)	DCO	4.5	
	Total	8.0	
FOM (dB)	Integer	-212.8	-225
	Fraction	-209	-222
Area	Core	180μm x 300μm	
	Total	300μm x 400μm	

Figure 19.2.7: Chip micrograph and result summary.

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