An 8-bit Analog-to-Digital Converter based on the Voltage-Dependent Switching Probability of a Magnetic Tunnel Junction

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Abstract

In this work, we have experimentally demonstrated for the first time, an Analog-to-Digital Converter (ADC) based on the unique voltage-dependent switching probability of a Magnetic Tunnel Junction (MTJ). The switching probability was calculated by applying repetitive voltage pulses and measuring the resolved MTJ states in each sampling time window. Temperature sensitivity and MgO breakdown issues were minimized by optimizing the voltage pulse width. Circuit level techniques were utilized to improve the ADC linearity and increase the input voltage range. The proposed ADC achieves an 8-bit resolution with excellent linearity at 30 and 85°C.

Introduction

Analog-to-digital converters (ADCs) are critical building blocks in a wide variety of applications such as medical devices, automotive, smart grid, wireless sensor networks, smartphones, smart buildings, and embedded control systems. Significant research progress has been made towards improving the ADC's energy-efficiency, resolution, and sampling speed in advanced CMOS technologies [1]. Traditional CMOS based ADCs can be classified into several different architectures: namely, successive approximation, flash, sigma-delta, pipelined, and time-interleaved. Meeting the demand of today's electronic systems in the face of aggressive transistor scaling has proven to be a challenge as designers have to grapple with device level issues such as process variation, threshold voltage instability, noise, and limited voltage headroom. In this work, we show the feasibility of a new class of ADC based on the voltage-dependent switching probability of a Magnetic Tunnel Junction (MTJ). MTJ technology has matured to the point where commercial STT-MRAM chips are currently being developed. This work aims at leveraging and complimenting on-going development efforts in MTJ technology for non-memory mixed-signal applications. The new ADC has the potential to achieve a compact area, simpler design, and reliable operation as compared to its CMOS counterpart.

MTJ-based Analog-to-Digital Converter

Spin Transfer Torque (STT) switching phenomenon in an MTJ is subject to thermal fluctuation noise which gives rise to a switching probability that is a strong function of the applied voltage (V_{MTJ}). This can be seen in Fig. 2 where the switching probability of a single MTJ device is plotted against different voltages for different pulse widths [2-4]. The main idea of this work is to utilize the unique voltage-to-probability transfer characteristic of an MTJ for converting an analog voltage (V_{MTJ}) to a digital code.

Fig. 3 shows the block diagram and operating principle of the proposed MTJ-based "probabilistic" ADC. It consists of a single MTJ, a sample and hold circuit, a bidirectional pulse generator to perturb the MTJ in either anti-parallel or parallel direction, a sense amplifier to determine the MTJ state (0 or 1), and a counter to calculate the number of times the MTJ has resolved to a '1' state. The operation example in Fig. 3 (bottom) illustrates the conversion from an analog input voltage, to a random bit stream, and finally to a digital code. The number of '1's in the bit stream is tallied for a fixed sampling window to generate the digital output count. A longer sampling window will produce a smoother and accurate probability curve at the expense of a longer sampling time.

The measurement setup to verify the basic ADC operation is shown in Fig. 4. Details of the MTJ device fabricated for this experiment is given in Fig. 1. Output signals from two high speed signal generators are combined and provided to the MTJ. A data acquisition board is used for reading out the MTJ state. To precisely control the temperature of the MTJ, a film resistance heater attached to the back side of the MTJ is driven by a software-controlled power supply. A thermocouple is used to monitor the MTJ temperature, enabling a feedback loop with an accuracy less than 1°C. All equipment are connected to the main computer using GPIB cables for automated testing.

The measured switching probability curves for 128 and 2,048 bits averaged per sample, under 30 and 85°C, are shown in Fig. 5. One of the most important parameters to optimize is the pulse width. A narrow and tall pulse is desired for minimizing temperature sensitivity as it ensures that the MTJ is in the precessional switching regime (rather than the thermal activated regime). On the other hand, a wide and small pulse is desired for preventing MTJ breakdown issues. We chose a pulse width of 5ns which balances these two design constraints. As expected, taking the average of 2,048 bits gives a smoother and more accurate probability curve than the 128 bit case. Temperature sensitivity was acceptably low.

Linearity is an important figure-of-merit for ADCs. The worst case Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) versus the number of bits averaged per sample are shown in Fig. 6. Here, we assumed a 5-bit resolution. A target DNL of 1 LSB can be met by averaging 2,048 or more random bits. However, the INL cannot be improved just by increasing the number of bits averaged. This is due to the inherent non-linearity of the MTJ stemming from the S-shape switching probability curve.

Improving Linearity and Input Voltage Range

To improve the linearity of the ADC further, we adopted the digital calibration technique widely used in CMOS ADCs [5, 6]. The technique can calibrate out any systematic non-linearity in the sensing element (e.g. amplifier, VCO, or MTJ). Fig. 7 shows the implementation and basic operation. During calibration mode, the MTJ's non-linearity is characterized by applying a slow ramp voltage generated by a digital-to-analog converter to the MTJ. The quantization noise in the sampled data is then filtered out using a moving average filter, and the results are stored in a Look-Up Table (LUT). During normal ADC operation, the raw output of the MTJ is corrected using the LUT mapping table. Fig. 8 confirms that the worst case INL is improved from -1.5 / +1.53 LSB to -0.71 / +0.72 LSB while the worst case DNL stays within -1 / +1 LSB spec.

As mentioned earlier, the voltage-to-probability transfer curve has a narrow input voltage range (~100mV) which limits the resolution of the MTJ-based ADC to about 5-bits. To enhance the input range of the ADC, we propose a new circuit technique described in Figs. 9, 10 where the MTJ's bottom terminal voltage (i.e., V_{OFFSET}) is dynamically varied according to the input voltage. This is equivalent to shifting the probability curve in the horizontal direction in a way that maximizes the sensing region. The detailed operating principle is as follows. First, the optimal V_{OFFSET} is found by incrementing the V_{OFFSET} from 0V to V_{DD} in $V_{IN,DYN}$ steps to determine the Most Significant Bits (MSBs). After this initial step, we fix the V_{OFFSET} to the optimal value and perform a fine ADC conversion to obtain the Least Significant Bits (LSBs). A resistive divider and an analog buffer are required to support this operation. Fig. 11 shows that the input range is increased by 8 times, from 128mV (5-bit resolution) to 1024mV (8-bit resolution). By combining the digital calibration and the input range enhancement techniques, the proposed MTJ-based ADC achieves a DNL within -1 / +1 LSB and an INL within -0.88 / +0.87 LSB as shown in Fig. 12. The ADC performance before and after applying each technique, is summarized in Fig. 13.

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References: [1] B. Murmann, "ADC Performance Survey 1997-2014" [2] H. Zhao, IEEE TMAG, 2012. [3] S. Yuasa, IEDM, 2013. [4] W.H. Choi, IEDM, 2014. [5] J. Kim, TCAS-I, 2010. [6] J. Daniels, VLSI Circuits Symp., 2010.

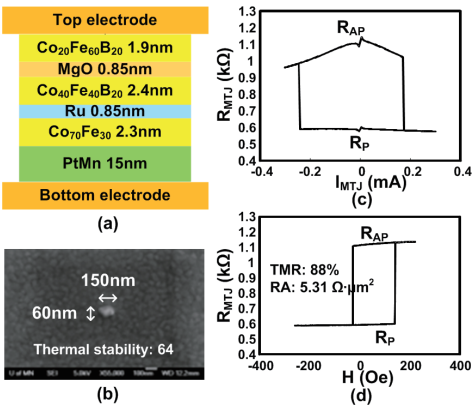

Fig. 1. CoFeB/MgO MTJ used in our experiments. (a) Vertical structure, (b) SEM image, (c) R-I, and (d) R-H hysteresis curves.

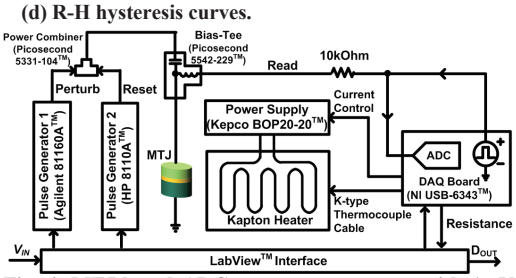

Fig. 4. MTJ-based ADC measurement setup with 1mV voltage resolution and <1°C temperature accuracy.

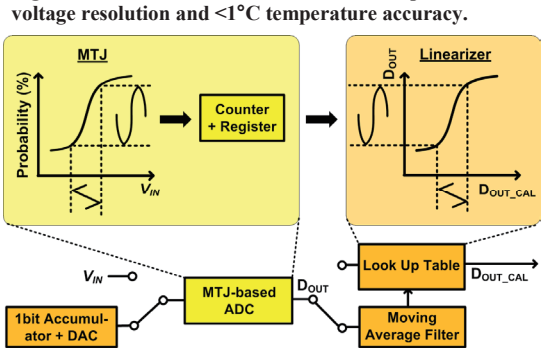

Fig. 7. Compensating for MTJ non-linearity using digital calibration [5, 6].

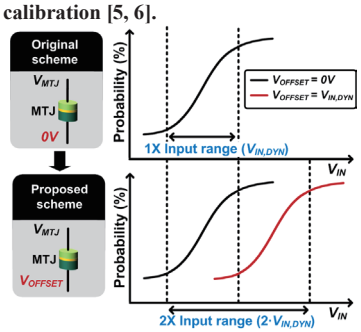

Fig. 9. Illustration of proposed input range enhancement technique.

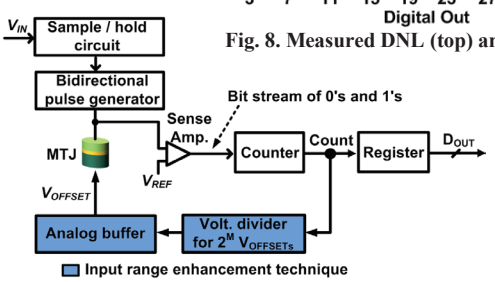

Fig. 10. Block diagram of MTJ-based ADC with input range expanding circuits. A voltage divider and an analog buffer control the MTJ bottom node voltage.

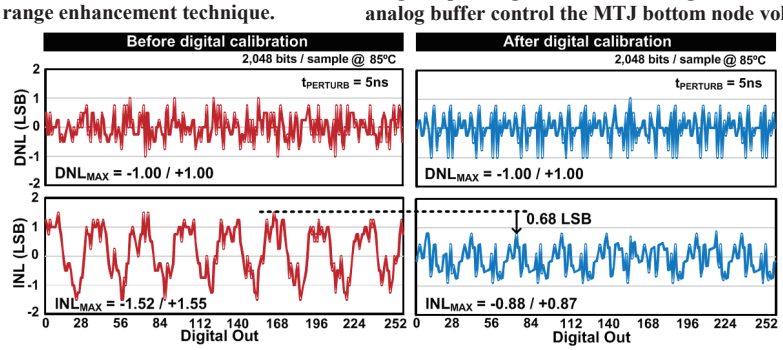

Fig. 12. Measured DNL (top) and INL (bottom) before and after digital calibration using the proposed input range enhancement technique.

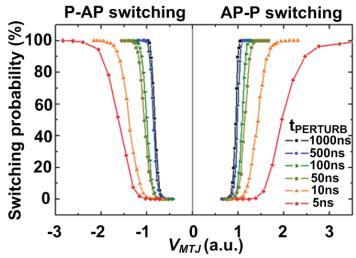

Fig. 2. Measured MTJ switching probability versus applied voltage [2].

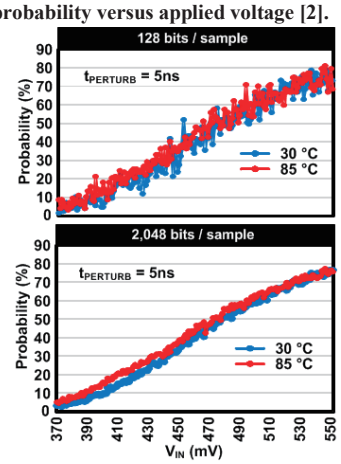

Fig. 5. Measured switching probability curve for 128 and 2,048 bits averaged per sample at 30 and 85°C.

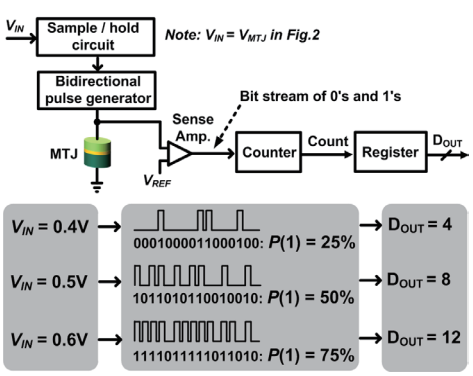

Fig. 3. Block diagram and operating principle of the proposed MTJ-based ADC.

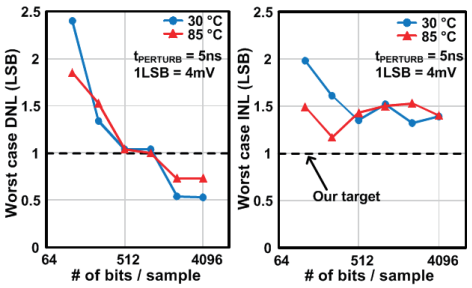

Fig. 6. Worst case DNL and INL for a 5-bit ADC resolution (i.e., 1 LSB=4mV) measured under two different temperatures (30, 85°C).

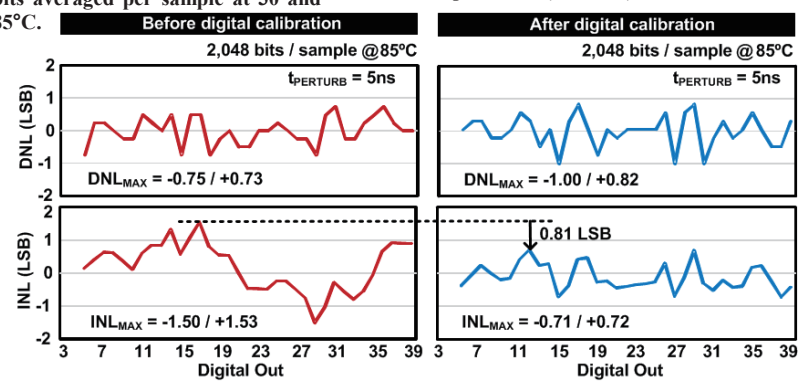

Fig. 8. Measured DNL (top) and INL (bottom) before and after digital calibration.

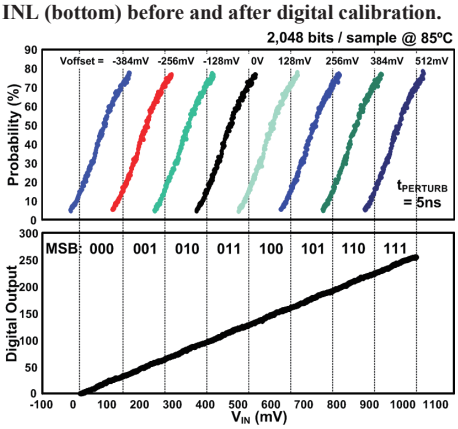

Fig. 11. Measured probability and corresponding digital output achieving an 8x wider input voltage range.

2,048 bits / sample

	Input range	30 °C DNLMAX (LSB)	30 °C INLMAX (LSB)	30 °C Bits	85 °C DNLMAX (LSB)	85 °C INLMAX (LSB)	85 °C Bits
Original MTJ-based ADC	128mV (X1)	0.74	1.32	5	0.75	1.53	5
+ Digital calibration	128mV (X1)	1.00	0.76	5	1.00	0.72	5
+ Digital calibration + Input range enhancement	1024mV (X8)	1.00	0.84	8	1.00	0.88	8

Fig. 13. ADC performance summary table.