

# A 0.4-1.6GHz Spur-Free Bang-Bang Digital PLL in 65nm with a D-Flip-Flop Based Frequency Subtractor Circuit

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## Abstract

A 0.4-1.6GHz spur-free bang-bang PLL (BBPLL) is demonstrated in a 65nm CMOS process where a standard D-flip/flop (DFF) based frequency subtractor is used in lieu of a conventional divider, for down-converting the feedback clock frequency. The inherent first-order noise-shaping property allows the proposed frequency subtraction circuit to mitigate spur-noise issues found in conventional digital BBPLLs. The fabricated BBPLL including a 10bit ring-DCO circuit has an in-band phase noise of -97dBc/Hz at 100kHz and an integrated RMS jitter (from 20kHz to 2MHz) of 2.8ps while consuming 2.7mW at 1.6GHz and occupying 0.019mm<sup>2</sup>. The PLL circuit has an FoM of -226.7dB.

## Introduction

Time-to-digital converters (TDC) and digitally controlled oscillators (DCO) are crucial building blocks in digital PLLs (DPLLs) since their time and frequency resolution determine the overall phase noise performance. While it is relatively straightforward to achieve a fine DCO frequency resolution by lowering the DCO's digital-to-frequency conversion gain, the design of a fine time resolution TDC circuit typically requires other sophisticated circuits such as Vernier delay lines, time amplifier, and noise-shaping circuits, which dissipate a large portion of PLL power affecting the jitter-power FoM. Recently, bang-bang phase and frequency detector (BBPFD) based PLLs (BBPLLs) [1-3] have been gaining interest for low power SoC's and high speed communication circuits due to their simple circuitry and favorable phase noise performance.

While existing BBPLLs are capable of generating output clocks with good in-band phase noise performances, they suffer from large spur noise due to the limit cycle behavior of BBPLL originating from the strong nonlinearity of the BBPFD. To resolve this issue, several circuit solutions have been proposed so far: for example, a separate proportional path with low latency and controllable gain, and a reference clock delay dithering circuit [4] were used. In this paper, we present a BBPLL with a novel D-flip-flop based frequency subtractor, which reduces the spur noise while quantizing the frequency difference between the reference and feedback clocks, with its inherent first-order noise shaping behavior.

## Spur-Free BBPLL with Frequency Subtractor

Fig. 1 shows the block diagrams of the conventional and proposed BBPLLs. In both design, the reference clock ( $CK_{REF}$ ) is divided by a pre-divider ( $P$ ) and then, its phase and frequency are compared with that of the feedback clock ( $CK_{FB}$ ). Conventionally, a frequency divider ( $M$ ) on the feedback path down-converts the PLL output clock frequency. In this work, we replace the frequency divider with a standard DFF-based frequency subtractor. The proposed frequency subtractor not only works as a frequency down conversion circuit (i.e. same purpose as the conventional divider), but also improves the noise performance by suppressing the spurs with its inherent noise-shaping property. It also improves the in-band phase noise by effectively reducing the feedback dividing ratio.

Fig. 2 illustrates two different usage scenarios of a DFF circuit. When the  $CK_{REF}$  frequency ( $f_{REF}$ ) is equal to or higher than the Nyquist rate (i.e.  $2f_{FB}$ ), the DFF circuit works as a digital sampler. In this case, the DFF output frequency ( $f_{OUT}$ ) is simply a quantized version of  $f_{FB}$ . When  $f_{REF}$  is lower than the Nyquist rate, however, the DFF works as a frequency subtractor. It can be seen in Fig. 2 (right) that the period of the DFF output clock ( $CK_{OUT}$ ) becomes equivalent to the time it takes for the faster  $CK_{REF}$  to pass, catch up and overtake the slower  $CK_{FB}$  again as shown in Fig. 2, right. Here, note that the number of  $CK_{REF}$  cycles that fit inside a single  $CK_{OUT}$  cycle

is larger than the number of  $CK_{FB}$  cycles by exactly 1 (assuming no quantization error for now). Under a locked condition, the frequency difference between  $CK_{REF}$  and  $CK_{FB}$  can be expressed as  $f_{REF} - f_{FB} = f_{REF}/P$  where  $P$  is the pre-divider ratio in Fig. 1, thereby generating a PLL output frequency ( $f_{FB}$ ) of  $f_{REF} \times (P-1)/P$ . An optional divider can be inserted in the feedback path (i.e.  $/8$  in Fig. 3) to further multiply the PLL output frequency. The output frequency can be changed by using different  $P$  values. Quantization error in the frequency subtractor output can be filtered out using the first-order noise-shaping property by allowing the DFF to run continuously.

Fig. 3 shows the block diagram of the proposed all-digital BBPLL implemented in a 65nm LP process. To compare the PLL performance with a conventional BBPLL from the same chip, we also implemented another version where the DFF is simply replaced by a standard divider circuit with the dividing ratio of 3 (i.e.  $f_{DIFF} = f_{FB}/3$ ) which produces the same PLL output frequency (i.e.  $f_{PLL} = f_{REF} \times \{8 \times (P-1)/P\}$  where  $P=4$ ). A digital loop-filter (DLF) is implemented with coarse and fine gain control bits for achieving a wide and fine programmable loop gain. A 10bit ring-DCO with 1024x unit capacitor banks is designed for fine frequency control.

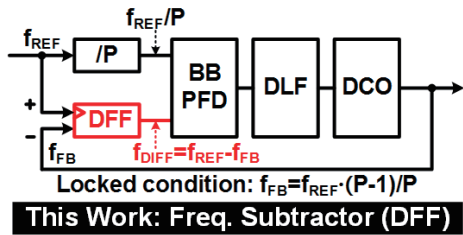
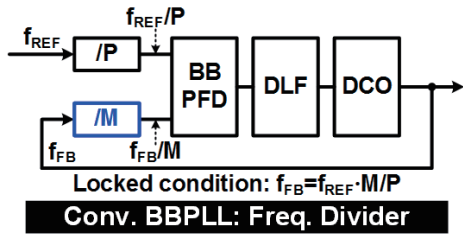
The inherent first-order noise-shaping behavior of the DFF-based frequency subtractor is illustrated in Fig. 4. When the input frequency difference lies between  $f_{REF}/4$  and  $f_{REF}/3$ , the sampled (quantized) DFF output clock frequency ( $f_{DIFF}$ ) alternates between  $f_{REF}/4$  and  $f_{REF}/3$  between each samples owing to the noise-shaping behavior. Fig. 5 shows the simulated frequency ratio between the reference clock and the DFF output clock. When the reference clock frequency  $f_{REF}$  is fixed at 266.667MHz, the simulated frequency ratio alternates between 3 and 4 (or 4 and 5) for a feedback clock frequency lower (or higher) than 200MHz. This phenomenon is due to the noise-shaping behavior of the frequency subtractor when the ratio between  $f_{FB}$  and the input frequency difference (i.e.  $f_{REF} - f_{FB}$ ) is a non-integer value.

## DCO Implementation and BBPLL Test Results

Fig. 6 shows the 10bit ring-DCO circuit with distributed fine-tuning capacitor elements. To achieve a fine frequency resolution, drain junction of a minimum sized PMOS is used as a unit capacitor [2]. The unit capacitors are then distributed and connected to the internal nodes of the 5 stage ring-oscillator to achieve a linear DCO gain. To achieve a fine frequency resolution (by lowering the DCO gain) while ensuring a wide DCO output frequency range, 16x unit ring-oscillator stages are connected in parallel and enabled after calibrating the initial frequency.

Both the conventional and proposed BBPLLs were implemented in the same 65nm test-chip for comparison. Fig. 7 shows the measured BBPLL output power spectra at 1.6GHz clearly showing a lower spur level for the proposed BBPLL. Fig. 8 shows the measured PLL phase noise at 1.6GHz. The measured in-band phase noise of the proposed BBPLL is -97dBc/Hz which is 9dB lower than that of the conventional design which is due to the 1/3 lower feedback dividing ratio. The integrated RMS jitter for a frequency offset range from 20kHz to 2MHz is 2.8ps which is 5.1ps lower than that of the conventional work. The chip micrograph with a summary table is shown in Fig. 9. The proposed BBPLL consumes 2.7mW at 1.6GHz and occupies 0.019mm<sup>2</sup>. Fig. 10 shows a comparison table with state-of-the-art digital PLLs. The PLL's FoM based on the measured jitter and power consumption is -226.7dB.

**References** [1] J. Hong, ISSCC, pp.240-24, Feb. 2012. [2] N. August, ISSCC, pp.246-247, Feb. 2012. [3] J. Liu et al., ISSCC, pp.268-269, Feb. 2014. [4] A. Rylyakov, ISSCC, pp.94-95, Feb. 2009. [5] Z. Ru, VLSI, pp.C194-C195, Jun. 2013. [6] D. Tasca, ISSCC, pp.88-89, Feb. 2011.



- ✓ Spurious-free bang-bang digital PLL
- ✓ Lower in-band PN vs. /M (@ equiv.  $M=P-1$ )

Fig. 1. Conventional and proposed bang-bang digital PLL circuit. This work uses a DFF-based frequency subtractor in lieu of a divider for the feedback clock frequency down conversion.

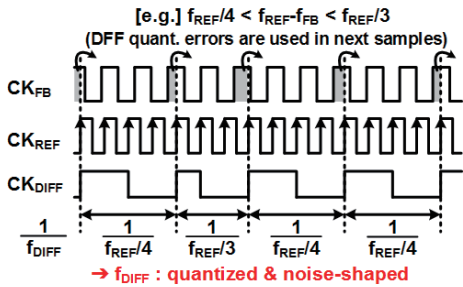


Fig. 4. Noise-shaping behavior of the proposed DFF-based frequency subtractor.

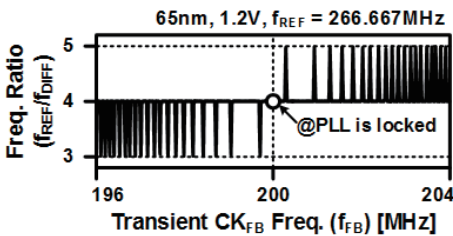


Fig. 5. Simulated frequency ratio (i.e.  $f_{REF}/f_{DIFF}$ ) when  $f_{REF}$  is fixed and  $f_{FB}$  is swept.

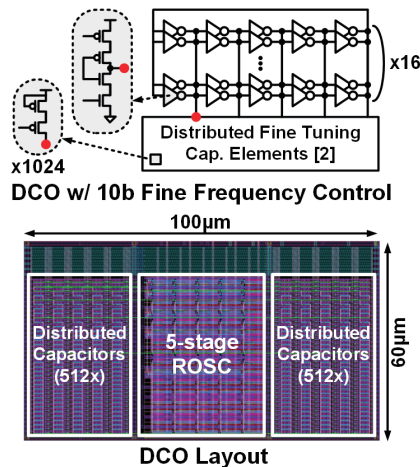


Fig. 6. Ring-oscillator DCO circuit and layout with 10bit fine control bits.

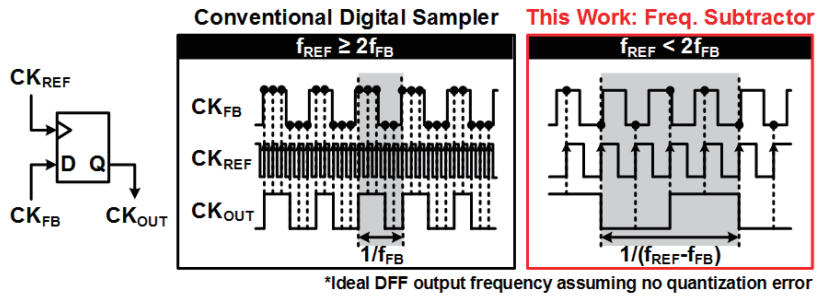
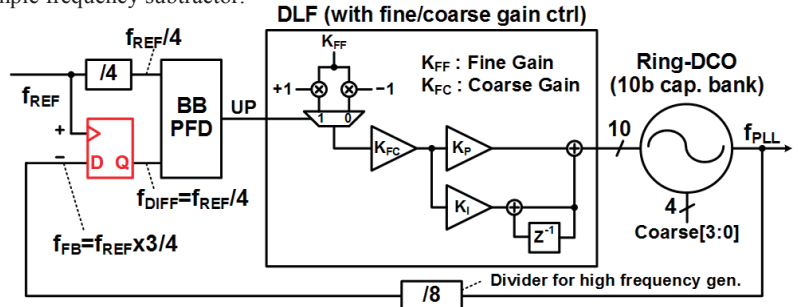


Fig. 2. A standard DFF works as a digital sampler ( $f_{REF} \geq 2f_{FB}$ ) or a frequency subtractor ( $f_{REF} < 2f_{FB}$ ) depending on the input frequencies. In this work, we utilize the DFF as a simple frequency subtractor.



**\*For 1-to-1 performance comparison, we also implemented another version where the D-flip-flop is replaced with a conventional /3 divider.**

Fig. 3. Block diagram of the proposed bang-bang all-digital PLL circuit generating an output clock frequency,  $f_{PLL} = f_{REF} \times \{8 \times (P-1) / P\}$  where  $P=4$ .

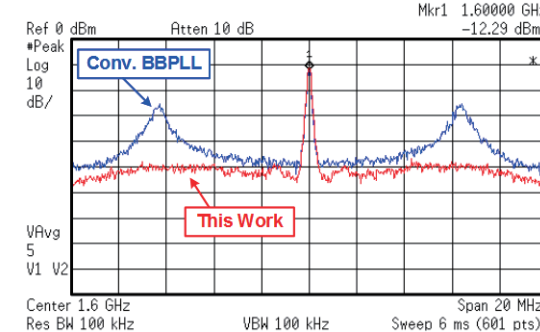


Fig. 7. Measured PLL output spectra at 1.6GHz.

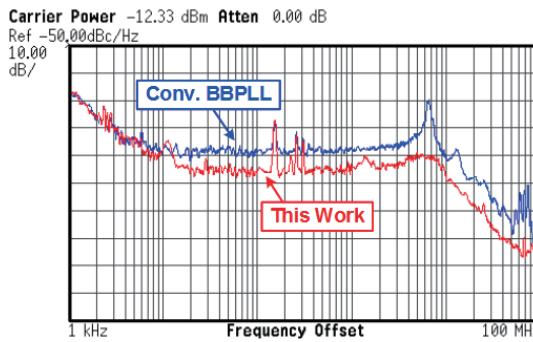
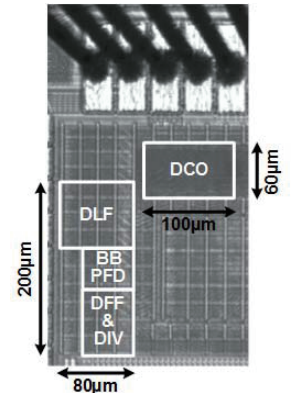


Fig. 8. Measured PLL phase noise at 1.6GHz.



Process	65nm CMOS
Supply	1.2V
PLL	Integer-N BBPLL
DCO	10b Ring-OSC
Freq.	0.4-to-1.6GHz
Power	2.7mW @ 1.6GHz
Area	0.019mm <sup>2</sup>
In-band P. Noise	-97dBc/Hz (Conv: -88dBc/Hz)
Spur Level	-90dBc/Hz (Conv: -70dBc/Hz)

Fig. 9. Chip micrograph and summary table.

	Process	DCO	Freq.	Power	Area [mm <sup>2</sup> ]	In-Band Phase Noise	RMS Jitter [20k to 2M]	FoM*
[5] VLSI'13	65nm	LC	11.8GHz	6.0mW	0.150	-100dBc/Hz	0.215ps	-245.6dB
[6] ISSCC'11	65nm	LC	3.3GHz	4.5mW	0.220	-101dBc/Hz	0.42ps	-241.0dB
[1] ISSCC'12	32nm	Ring	1.5GHz	2.5mW	0.012	-89dBc/Hz	8.8ps	-217.1dB
[2] ISSCC'12	22nm	Ring	0.4GHz	0.8mW	0.017	-100dBc/Hz	5.9ps	-225.6dB
[3] ISSCC'14	20nm	Ring	1.23GHz	2.5mW	0.012	-90dBc/Hz	11.5ps	-214.8dB
This Work	65nm	Ring	1.6GHz	2.7mW	0.019	-97dBc/Hz	2.8ps	-226.7dB

\*FoM = 10 · log<sub>10</sub> [(Jitter<sup>2</sup>/1s) · (Power/1mW)]

Fig. 10. Comparison with state-of-the-art digital PLLs.