High Frequency AC Electromigration Lifetime Measurements from a 32nm Test Chip

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Abstract

A test circuit for studying Electromigration (EM) effects under realistic high frequency AC stress was implemented in a 32nm High-k Metal Gate (HKMG) process. Four different stress patterns (DC, pulsed DC, square AC and real AC) can be generated using on-chip circuits. Local heaters are used to raise the die temperature to >300˚C for accelerated testing. Experiment results over 52.7 hours show no AC stress induced failures under 325˚C, 1.5V (driver supply) at 200 MHz and 900 MHz. However, the pre-AC stress had an impact on the DC EM distribution.

Introduction

EM is the main back-end-of-line (BEOL) reliability concern in which metal atoms gradually migrate at elevated temperatures, creating voids and extrusions that manifest as abrupt or progressive changes [1] in wire resistance. There has been a renewed interest in EM due to the increased current density, excess Joule heating, and higher switching speeds. EM lifetime under DC current is usually orders of magnitude shorter than that under AC current because the net transport is zero in the latter case. Traditional studies have thus focused on DC EM and its impact on power grid integrity, although the inherent redundant paths make power grids highly resilient to EM events. In contrast, AC EM in signal wires will have a direct impact on the speed and functionality of interconnects. To study high frequency AC EM statistics in more detail, we designed and tested an EM test array in a 32nm HKMG process containing local heaters and active circuits that can provide realistic AC stress signals with frequencies up to ~1GHz.

EM Test Array Design

Fig. 1 shows the four different stress modes implemented in our test array. Bird's eye view diagram of the EM wire is shown in Fig. 2. The input and output of the wire is driven from both sides by tri-state inverters while the output is connected to next stage via a third tri-state inverter. Wires are connected in a daisy chain fashion so that EM-induced frequency shift can be measured. Using this configuration, the four stress modes in Fig. 1 can be applied: namely, DC, pulsed DC, square AC and real AC. Square AC current, similar to the definition of AC current used in related works [2,3], is a bidirectional square-wave current with a fixed amplitude. Real AC current, which to the best of our knowledge has never been used for EM studies, refers to the output current of an inverter driving a long interconnect. An on-chip voltage-controlled oscillator (VCO) generates the stress clock for the pulsed DC, square AC and real AC modes. The length and width of the EM wire are 200μm and 50nm, respectively. A single M1-to-M2 via is placed at both ends of the EM wire to form an upstream and downstream current path as illustrated in Fig. 2. A total of 60 wires are implemented in each chip. During stress mode, the individual wires are isolated from each other and are stressed separately. One key benefit of our test array over previous serial testing methods is that all 60 wires in a chip can be stressed simultaneously which reduces the test time by 60x.

Local Heater Design and Temperature Control

One of the key requirements for the EM test array is the ability to increase the temperature of the EM wires to >300˚C for accelerated testing while keeping the active circuits relatively cool. Unlike previous BEOL-only works where the entire wafer could be heated up in an oven, our circuit based approach requires a PCB based setup (with cables and connectors) which will melt when exposed to excessive heat. In addition, the active circuit needs to run at lower temperatures to prevent aging and leakage issues. To this end, we placed on-chip metal gate heaters underneath the EM wires while moving the peripheral circuitry away from the heater core, as shown in Fig. 4. Each heater is 17.5μm wide and 300μm long. A total of nine heater strips were combined into three independently-controllable heater groups to reduce IO pin count while keeping enough flexibility to create a uniform temperature. Fig. 5 shows thermal-electric simulation results wherein the heat core temperature was maintained uniform by applying different voltages to each heater group.

To verify that the actual chip temperature reaches the target value, we use the so called Temperature Coefficient of Resistance (TCR) method described in Fig. 3 wherein the linear relationship between resistance and temperature is utilized to estimate the actual chip temperature. We chose to measure the heater resistance rather than the EM wire resistance since the heater resistance can be easily read out without having to interrupt the high temperature stress. The heater resistance was first measured at low temperatures (from 0 to 100˚C) in a temperature controlled chamber to obtain the TCR curve. During stress mode, a script based software monitors the chip temperature every 1 second and then adjusts the heater voltage according to the target temperature/resistance (shown in the right part of Fig. 6). To eliminate the possibility of any EM-induced failures in the heaters themselves, the software periodically switches the direction of the heater current.

Test Methodology and EM Data

Fig. 6 illustrates the overall test flow implemented entirely in software. The EM wire temperature was raised to 325ºC using local heaters while the stress current was provided by tri-state inverters operating at 1.5V. Resistance values from all 60 wires in the chip were read out every 10 minutes. The 4-terminal Kelvin method shown in Fig. 7 was used for accurate resistance measurements. To suppress leakage current in the switches, the temperature target was lowered to 100ºC prior to measuring the resistance value. After the resistance of all EM wires are measured, the chip temperature was raised back to 325ºC. Although we had the option of measuring frequency of the EM wire chain, front-end aging and leakage issues at elevated temperatures prevented us from collecting good data.

Fig. 8 shows resistance traces for all 60 wires under 900 MHz real AC and pure DC. Although the VCO can run much faster, we chose a conservative stress frequency of 900 MHz to avoid any possible distortion in the stress input signal. EM failures were only observed for the DC stress under the given condition. Both abrupt and progressive failures were observed as shown in Fig. 9. Abrupt failures that account for 56-65% of the wires have an earlier time-to-failure and a wider distribution as compared to progressive failure. Temporary healing [4] was observed in some wires exhibiting abrupt failure (Fig. 9, upper). Fig. 10 shows the time-to-failure distributions of abrupt, progressive and combined failure modes. Here, we use 10% change in resistance as the EM criteria. The empirical EM model in [5] was adopted to fit our experimental data. Since no EM failure occurred for square AC and real AC, we applied DC stress on chips that already underwent AC stress to see if there's any impact on the EM distribution curve [2]. Fig. 11 shows DC EM (and 200 MHz pulsed DC) resistance traces for chips that underwent 52.7 hours of 200 MHz square AC pre-stress, 200 MHz and 900 MHz real AC pre-stress, in addition to chips with no pre-stress. The time-to-failure for pulsed DC was significantly longer (~2.5x) than that of pure DC due to the 50% duty cycle and lower Joule heating. Square AC had negligible impact on DC EM whereas real AC resulted in a subtle shift in both abrupt and progressive failure distributions which marginally increased the time-to-failure. These counterintuitive results suggest that traditional AC EM models based on forward and backward current densities may not be adequate for capturing real AC effects (including circuit level effects) at high frequencies.

References [1] S. Lee, IRPS, pp.107-114, 2006. [2] R. Shaviv, IRPS, pp.EM.3.1-6, 2011. [3] K. Lee, IRPS, pp. 6B.3.1-4, 2012. [4] A.W. Hunt, APL, pp.2541-2543, 1997. [5] R.G. Filippi, IRPS, pp.444-451, 2009.

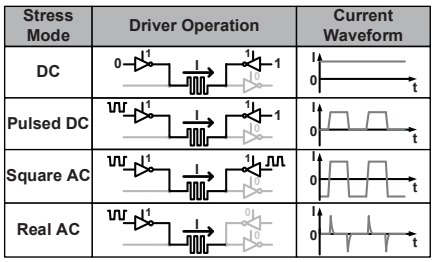

Fig. 1. Four supported EM stress current patterns using on-chip circuits: DC, pulsed DC, square AC and real AC.

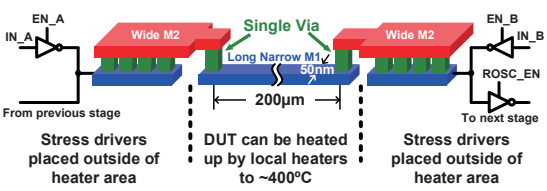

Fig. 2. EM DUT used in our experiment. Stress current is applied to a minimum width M1 wire with single via placed on both sides.

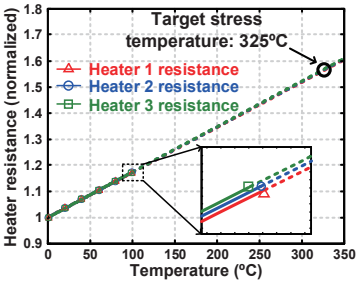

Fig. 3. Temperature coefficient of resistance (TCR) measured from actual test chip.

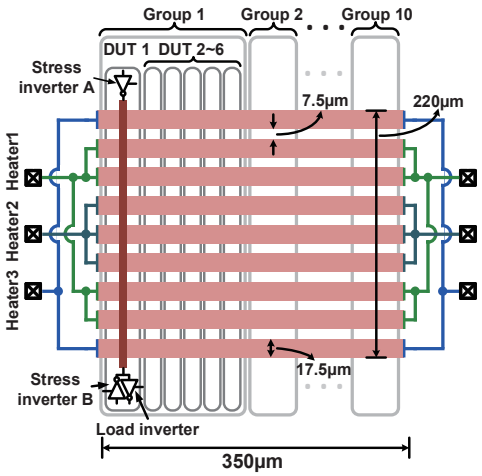

Fig. 4. Test chip floorplan showing 3 individually-controlled local heaters and 6x10 EM metal wires.

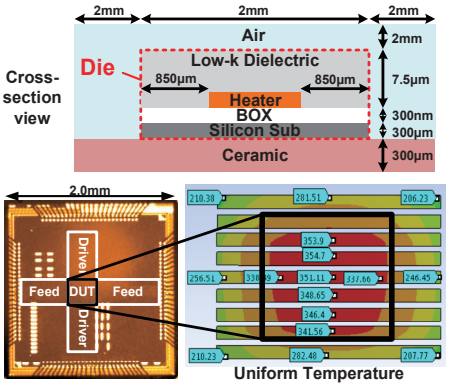

Fig. 5. Die photo and temperature sim. results.

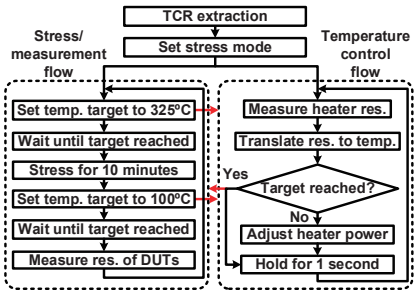

Fig. 6. Software flow for automatic EM measurements and temperature control.

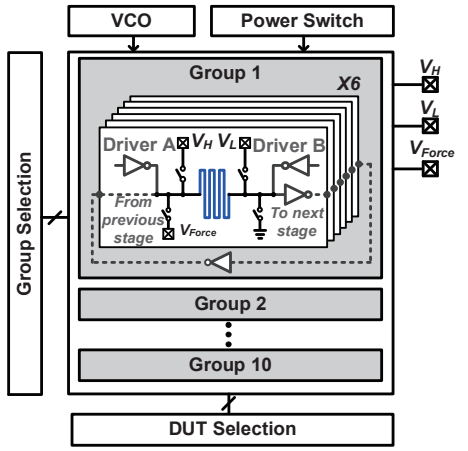

Fig. 7. Full chip schematic showing 4-terminal Kelvin resistance measurement circuit.

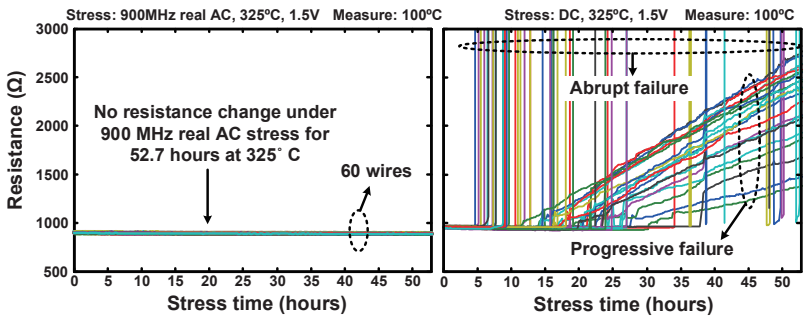

Fig. 8. Resistances traces under real AC (left, 900MHz) and DC (right) stress.

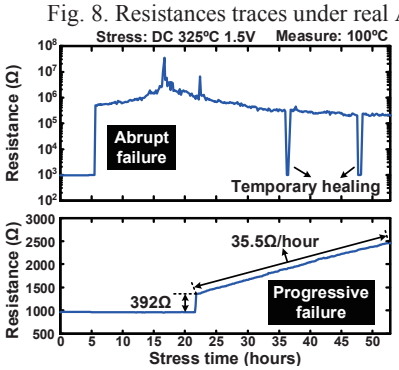

Fig. 9. Abrupt and progressive failure resistance traces measured from chip.

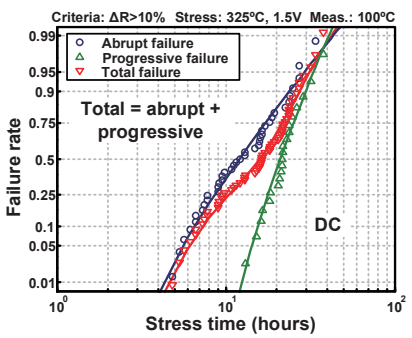

Fig. 10. Abrupt and progressive failure EM statistics under DC stress.

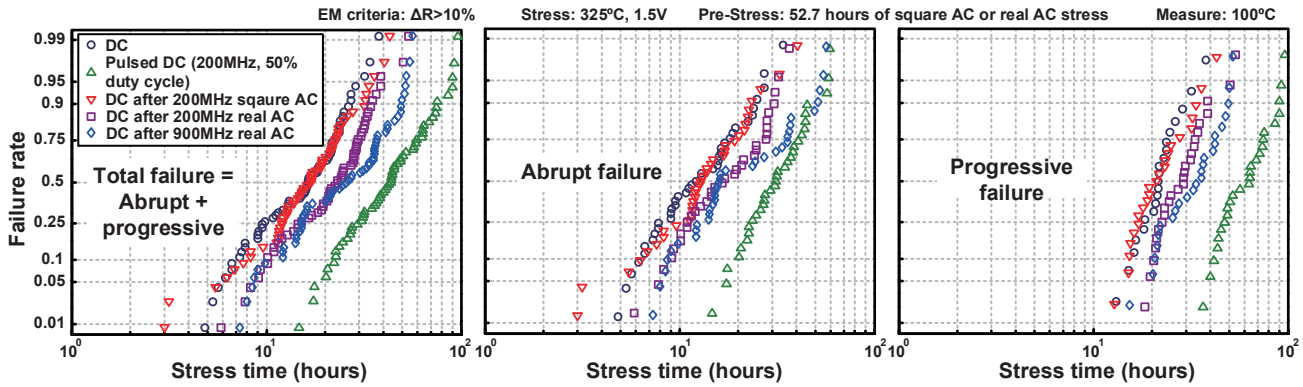

Fig. 11. Comparison between DC, pulsed DC (200MHz), DC after square AC (200MHz) and DC after real AC (200MHz and 900MHz). AC stress was applied for 52.7 hours. Time-to-failure distributions for combined (left), abrupt (middle) and progressive (right) failures.