The Dependence of BTI and HCI-Induced Frequency Degradation on Interconnect Length and Its Circuit Level Implications

Xiaofei Wang, Student Member, IEEE, Qianying Tang, Student Member, IEEE, Pulkit Jain, Member, IEEE, Dong Jiao, Member, IEEE, and Chris H. Kim, Senior Member, IEEE

Abstract—The dependence of bias temperature instability (BTI) and hot carrier injection (HCI)-induced frequency degradation on interconnect length has been examined for the first time. Experimental data from 65-nm test chips show that frequency degradation due to BTI decreases monotonically for longer wires because of the shorter effective stress time, while the HCI-induced component has a nomenclature relationship with interconnect length due to the combined effect of increased effective stress time and decreased effective stress voltage. Simple aging models are proposed to capture the unique BTI and HCI behavior in global interconnect drivers. A closed-loop simulation methodology that takes into consideration the interplay between the frequency degradation and the stress parameters (such as stress duration and stress voltage) is used to determine the optimal repeater count and sizing in practical interconnect circuits.

Index Terms—Bias temperature instability (BTI), circuit aging, circuit reliability, frequency degradation, hot carrier injection (HCI), interconnect, signal buses.

I. INTRODUCTION

INTERCONNECTS used in clock networks, signal buses, network-on-chips, memory wordlines/bitlines, and high-speed I/Os are critical components in modern ICs. CMOS devices in interconnect drivers experience a complex time-varying voltage stress, which is a function of the interconnect load. Therefore, performance degradation of interconnect drivers due to reliability mechanisms such as bias temperature instability (BTI) and hot carrier injection (HCI) depends on the length and width of an interconnect wire. BTI is considered as the primary reliability concern in modern CMOS processes and occurs when a device is biased in strong inversion mode [1]–[4]. Once a device is turned off, the degradation caused by previous stress periods starts to recover immediately. Despite the scaling of supply voltage in advanced technologies, HCI remains to be an important reliability concern especially toward the end of a product lifetime owing to the 4–5x larger time exponent [5]–[8]. Moreover, interconnect drivers (for example, clock drivers) have a higher activity factor and larger average current driven compared with random logic gates, making HCI a greater concern.

BTI and HCI mechanisms have different sensitivities to the operation Conditions, which depend on the interconnect configuration. Moreover, sheet resistance and parasitic capacitance of long wires have not been scaling favorably in advanced processes, which could lead to interconnect dominated paths having drastically different aging behavior compared with logic dominated paths in the future. Although there have been previous works showing the impact of fanout load on transistor aging [9]–[13], almost no attention has been paid to the aging behavior in interconnect drivers for long RC wires. A deeper insight into interconnect driver aging will enable a more complete picture of system level aging and allow us to build interconnect circuits that are more tolerant to device aging.

For the first time, this paper presents measurement results highlighting the dependence of BTI and HCI-induced aging on wire length [14]. Our previous all-in-one silicon odometer framework [12] was adopted to separate the BTI and HCI contributions with picosecond-order resolution and microsecond-order measurement interrupts. Measurement data from a 65-nm test chip shows that BTI-induced degradation decreases monotonically for longer interconnect length while HCI exhibits a nonmonotonic dependency on interconnect length. Based on a detailed circuit level analysis, simple aging models incorporating interconnect parameters are proposed for estimating BTI and HCI-induced degradation in interconnect drivers. These models show good agreement with measured data. Several real-world examples are provided that demonstrate the practicality of the proposed models in the context of interconnect driver design.

II. INTERCONNECT ODOMETER DESIGN

The top level block diagram of the interconnect odometer test chip is shown in Fig. 1. Four ROSC configurations with different interconnect lengths of 0, 250, 500, and 1000 μm were implemented. Transistor dimensions of each ROSC stage are \((W/L)_{pMOS} = 6/0.06\ \mu m\) and \((W/L)_{nMOS} = 3/0.06\ \mu m\) regardless of the interconnect length. Although this configuration may not represent an interconnect circuit optimized for speed, it allows us to separate out the impact of interconnect length on frequency degradation. Among the four ROSCs,
one undergoes BTI stress only, one undergoes both BTI and HCI stress, and the other two are remained unstressed serving as a frequency reference point. Each stressed oscillator is paired up with its unstressed counterpart, and fed into a beat-frequency detection system through multiplexers. On-chip power gates provide fast local stress voltage switching in the nanosecond order while a voltage controlled oscillator generates an ac stress frequency.

A. Beat-Frequency Detection Technique

The beat frequency odometer system in Fig. 2 measures the percentage change in the stress ROSC frequency. We include a brief explanation of the beat frequency odometer system for convenience but further details can be found in [11]. The output of the reference ROSC is used as clock of the D flip-flop (DFF) to sample the stressed ROSC output. The initial frequency of the reference ROSC \( f_{\text{ref}} \) is set using trimming capacitors to be slightly higher than that of the stressed ROSC \( f_{\text{stress}} \). The DFF output toggles from low to high whenever the rising edge of the two ROSC outputs overlap. In other words, the output of the DFF exhibits the beat frequency \( f_{\text{beat}} \) defined as \( f_{\text{beat}} = f_{\text{ref}} - f_{\text{stress}} \). A counter is implemented at the output of the DFF to record the number of reference ROSC periods corresponding to the beat period.

The count is registered after each stress period, and the frequency shift in the stress ROSC can be conveniently calculated using straightforward algebraic equations shown in Fig. 2.

The main highlight of the beat frequency odometer system is that it provides extremely high-resolution frequency shift measurements (>0.01%) with microsecond-order measurement interruption, which eliminates the unwanted BTI recovery effects. A detail comparison of various ROSC-based frequency degradation measurement techniques can be found in our previous all-in-one odometer paper [12].

B. Separately Monitoring BTI and HCI

The BTI and HCI contributions were separately measured by adopting the all-in-one odometer concept shown in Fig. 3 [12]. In stress mode, the top ROSC is gated off from the supply with the bottom ROSC driving the inputs and outputs of both ROSCs. Using this configuration, the transistors in the top ROSC experience the same BTI stress condition as those in the bottom ROSC but with negligible HCI degradation. Note that electromigration and Joule heating effect in the wires was negligible due to the small average current and rms current according to the 65-nm process used for the test chip and therefore the frequency degradation is purely due to the transistor aging. In measurement mode, the frequency degradations of the two stressed ROSCs are measured using two silicon odometer beat frequency detection systems. The HCI-induced aging can be then obtained by subtracting out the BTI component (top ROSC in Fig. 3) from the combined BTI + HCI effect (bottom ROSC in Fig. 3).
C. Layout Details

The layout of a ROSC pair with a per-stage interconnect length of 1000 μm is shown in Fig. 4. A stressed ROSC and its fresh counterpart are placed right next to each other symmetrically to minimize any systematic variation due to layout mismatches, voltage gradients, and temperature differences. Minimum width M2 wires were laid out in a serpentine manner to fit the long interconnect in the given die area. To minimize any coupling effect occurring at the end of each metal segment, double-shielded wires with minimum metal-to-metal spacing was used. We understand this may increase the capacitive loading of the signal interconnect compared with a typical interconnect circuit. However, our analysis shows that by parameterizing circuit parameters such as wire capacitance, wire resistance, and the driver’s equivalent resistance values, we can build universal aging models applicable to a wide range of interconnect designs across different technologies and operating conditions. Further details on this point can be found in Section IV. The die photo and key features of the 65-nm interconnect odometer test chip are shown in Fig. 5.

III. TESTCHIP RESULTS

A. ROSC Aging Measurements

We first present experimental data from the test chip in Fig. 6 showing the general behavior of HCI and BTI degradation from ROSCs without any long interconnects between the inverter stages. As expected, BTI shows a positive dependence on temperature, while HCI has a slightly negative dependence on temperatures, which is mainly due to the reduced drain current resulting from increased phonon scattering [Fig. 6(a)]. BTI is at best weakly dependent on the frequency as shown in Fig. 6(b), while HCI degradation increases at higher frequencies due to the higher switching activity. Fig. 6(c) shows that both aging mechanisms worsen at higher stress voltages with HCI displaying a stronger voltage dependence. Both BTI and HCI degradations show good agreement with simple power law models (i.e., \( t^n \)) using fitted power law exponents \( n \), which are denoted in the figure. BTI is the primary aging contributor at early stress times while HCI with its four to six times larger power law exponent surpasses BTI at longer stress times, which results in a cross over point between the two trend lines.

Having confirmed the general behavior of HCI and BTI through repeated tests, we carried out stress experiments on the ROSCs with long interconnects. Fig. 7 shows the BTI and HCI degradation versus stress time for different interconnect configurations. To our surprise, under an identical stress condition, the ROSC with no interconnect shows the worst BTI degradation, while the ROSC with an interconnect length of 500 μm had the worst HCI degradation. The time it takes for HCI to overtake BTI (i.e., crossover time) decreases by almost three orders of magnitude as the interconnect length is increased from 0 to 1000 μm as shown in Fig. 8(b) under a stress condition of 2.4 V, 300 MHz at 85 °C. This trend can be attributed to the lower BTI and higher HCI [until around 500 μm according to Fig. 7 (right)] for ROSCs with longer interconnect lengths. In the following sections, we further examine the unexpected BTI and HCI trends shown in Fig. 7, which clearly indicates a difference in their wire length dependencies.

B. Interconnect Length Versus BTI Aging

The BTI-induced frequency shifts after 19 h of stress at 2.4 V are shown in Fig. 9 for different interconnect lengths. BTI aging decreases monotonically with longer interconnects for all three stress conditions. This can be explained by the longer signal transition time in longer wires, which translates into a shorter time in which the transistors are actually exposed to a full BTI stress. Simulated waveforms in Fig. 10 show a longer slew rate for longer wires. The results summarized in the table confirms a \( 6.2 \times \) longer transition time \( (t_r = t_{r_s} + t_F) \) and a 9.6% reduction in the effective stress duty cycle \( (t_L/\tau) \) as
The wire length is increased from 0 to 1000 μm for a driver size of \((W/L)_{pMOS} = 6/0.06 \text{ μm}\) and \((W/L)_{nMOS} = 3/0.06 \text{ μm}\). Note that PBTI in nMOS is negligible in this 65-nm process as it does not employ high-k metal-gate process. However, the general behavior will be exacerbated in the presence of PBTI as the duty cycle for the nMOS is also reduced for longer interconnects. Fig. 9 also reveals a weaker dependency on interconnect length for lower ac stress frequencies. This can be attributed to the smaller fraction of time spent for signal transition at lower input frequencies, which makes the duty cycle less sensitive to the interconnect length as shown in the simulations for different ac stress periods in Fig. 11.

C. Interconnect Length Versus HCI Aging

The effect of HCI in Fig. 12 shows a nonmonotonic relationship with wire length. This is somewhat counter-intuitive but can be explained using the following two reasons.

1) A driver with a longer wire has a smaller peak current due to the voltage division effect between the wire resistance and the driver’s equivalent resistance, as shown in Fig. 13. In other words, the effective stress voltage \(V_{eff}\) that dictates the amount of HCI decreases with a longer interconnect. Additional simulation results in Fig. 14 confirm that the peak discharging current \(I_{peak}\) through the nMOS decreases with longer interconnect due to the aforementioned voltage division effect. For the simulation, we use a driver size of \((W/L)_{pMOS} = 6/0.06 \text{ μm}\) and \((W/L)_{nMOS} = 3/0.06 \text{ μm}\) and a distributed RC wire model to obtain accurate results. The reduction of the peak current has a similar effect as having a lower effective stress voltage and therefore leads to a smaller frequency shift. Note that the peak current may actually increase for wire lengths from 0 to 200 μm due to the fast input slew rate that causes the nMOS to turn off before it enters the saturation mode.

2) A longer wire makes the current pulse wider due to the larger wire capacitance, which has the effect of increased effective stress time \(t_{eff}\) compared with a shorter wire. A longer current pulse width shown in Fig. 13 is equivalent to an increased HCI stress time, which leads to increased HCI degradation for longer interconnects [15]. The combined effects of 1) and 2), coupled with their different sensitivities on the frequency degradation, result in the nonmonotonic relationship between HCI-induced frequency shift and interconnect length.
IV. AGING MODELS FOR INTERCONNECT DRIVERS

As we saw in the previous sections, frequency degradation due to BTI and HCI depends on the transition time and bias condition, which are both strong functions of the interconnect load. However, none of the existing circuit aging models incorporate interconnect related parameters for estimating BTI and HCI-induced degradation. In this section, we propose analytical models applicable to global interconnect drivers, which agree well with the experimental results in Section III. The general approach for modeling the frequency degradation in global interconnects is described below.

Step 1: The frequency degradation of an interconnect dominated path is less sensitive to the device aging compared with a logic dominated path due to the time invariant interconnect RC delay. We account for this difference by introducing a sensitivity factor $\alpha$.

Step 2: The amount of BTI and HCI aging depends on the effective stress time and effective stress voltage that vary with interconnect length. Existing BTI and HCI models with modified stress time and stress voltage are used to derive the final model.
Section IV-A describes the above step 1) where we will first analyze the sensitivity factor and derive its mathematical expression. In Section IV-B and IV-C, we perform step 2) where the final analytical BTI and HCI models for interconnect drivers are derived.

A. Sensitivity Factor

Delay degradation of an interconnect dominated-path is less sensitive to the transistor parametric shift compared with its logic-dominated counterpart. This can be observed from the HSPICE results in Fig. 15 where a device $V_t$ shift of 30% translates into a 12% frequency degradation for a ROSC with a 1000 $\mu$m interconnect per stage, whereas the degradation for a ROSC with no interconnects is 15%. This effect can be easily captured in our model by introducing a sensitivity factor $\alpha$ defined as the ratio between the % frequency degradation of an interconnect dominated path and that of a logic dominated path for the same amount of device aging

$$\left(\frac{\Delta f}{f}\right)_{\text{interconnect}} = \alpha \left(\frac{\Delta f}{f}\right)_{\text{logic}}. \quad (1)$$

For a given interconnect resistance ($R_W$), interconnect capacitance ($C_W$), load capacitance ($C_L$), equivalent driver resistance before ($R_{eq}$) and after stress ($\Delta R_{eq} = R'_{eq} - R_{eq}$), and the inverter stage number $N_{stage}$, the ROSC period can be calculated as

$$\tau = 2N_{stage} \left[ R_{eq} (C_W + C_L) + R_W \left(\frac{C_W}{2} + C_L\right) \right]. \quad (2)$$

The % frequency degradation can then be expressed as

$$\left(\frac{\Delta f}{f}\right)_{\text{interconnect}} = \frac{\Delta R_{eq} (C_W + C_L)}{R'_{eq} (C_W + C_L) + R_W \left(\frac{C_W}{2} + C_L\right)}. \quad (3)$$

Note that $R_W$ and $C_W$ of a wire can be simply calculated from the sheet resistance and metal capacitance parameters.
can be written as

\[
\frac{\Delta f}{f} = \alpha \frac{V_{th}}{V_{th}} \exp(\frac{E_d}{K T}) m \cdot \exp(\frac{E_d}{K T}) f \cdot [1 - B(21m_n) f]^{1 - B(21m_n) f}
\]

\[
\frac{\Delta f}{f} = \alpha \frac{V_{th}}{V_{th}} \exp(\frac{E_d}{K T}) m \cdot \exp(\frac{E_d}{K T}) f \cdot [1 - B(21m_n) f]^{1 - B(21m_n) f}
\]

\[
\frac{\Delta f}{f} = \alpha \frac{V_{th}}{V_{th}} \exp(\frac{E_d}{K T}) m \cdot \exp(\frac{E_d}{K T}) f \cdot [1 - B(21m_n) f]^{1 - B(21m_n) f}
\]

\[
\frac{\Delta f}{f} = \alpha \frac{V_{th}}{V_{th}} \exp(\frac{E_d}{K T}) m \cdot \exp(\frac{E_d}{K T}) f \cdot [1 - B(21m_n) f]^{1 - B(21m_n) f}
\]

The percentage frequency degradation for a logic only path can be written as

\[
\frac{(\Delta f)}{f} \text{ logic} = \frac{\Delta R_{eq} C_L}{R_{eq} C_L} = \frac{\Delta R_{eq}}{R_{eq}}
\]

Using (3) and (4), the expression of \( \alpha \) can be derived as

\[
\alpha = \frac{(\frac{\Delta f}{f})_{\text{interconnect}}}{(\frac{\Delta f}{f})_{\text{logic}}}
\]

\[
= \frac{\Delta R_{eq} (C_L + C_L)}{R_{eq} (C_L + C_L) + R_W (C_L + C_L)} \Delta R_{eq}
\]

\[
= \frac{R_{eq} (C_L + C_L)}{R_{eq} (C_L + C_L) + R_W (C_L + C_L)} \frac{R_{eq} (C_L + C_L)}{R_{eq} (C_L + C_L) + R_W (C_L + C_L)}
\]

\[
= \frac{R_{eq} (C_L + C_L)}{R_{eq} (C_L + C_L) + R_W (C_L + C_L)}
\]

The above sensitivity factor will be applied to the BTI and HCI models proposed in Section IV-B and IV-C.

**B. BTI Aging Model for Interconnect Drivers**

While the detailed physics for BTI are still under debate, the following two models are generally considered for BTI-induced degradation: the reaction-diffusion model, which follows a power law time dependence \( \propto t^n \), and the trapping-detrapping model, which follows a logarithmic time dependence \( \propto \log(2t + 1) \). Our experimental data shows a good agreement with the power law dependence under different stress conditions and hence we report the time exponent values in this paper.

BTI aging is a function of device on time. Hence, in the context of an interconnect driver, it can be expressed using the cycle time parameter \( t_L / \tau \), where \( t_L \) and \( \tau \) are shown in Fig. 10. Employing the models in [16] and [17] with dynamic stress modeling methodology in [18] adopted, the deviation of BTI from the ideal 50% duty cycle case can be expressed using \( (50% - t_L / \tau)^f \), where \( f \) is determined empirically. The overall BTI induced frequency shift can be expressed as

\[
\frac{(\Delta f)}{f} = \left( \frac{(\Delta f)}{f} \right)_{\text{BTI}} \left( 1 - B \left( \frac{50% - t_L / \tau}{\tau} \right)^f \right)
\]

\[
= A(V_{str} - V_T)^{-0.5} e^{(-\frac{V_{str}}{E_d})} e^{(-\frac{V_{str}}{E_d})^n}
\]

\[
\cdot \left[ 1 - B \left( \frac{21m_n}{\tau} \right)^f \right].
\]

Here, \( \gamma \) is the voltage acceleration factor and \( E_d \) is the temperature activation energy. Both parameter values are reaction characteristics related coefficients obtained from silicon results under different stress voltage and temperature conditions. \( V_{str} \) is the stress voltage, \( V_T \) is threshold voltage, \( t_L \) is the BTI stress time of a logic only path, \( n \) is the BTI time exponent, \( \tau \) is the transition time, and \( \tau \) is the period of ac stress cycle. \( A, B, \) and \( f \) are the empirical parameters found to be \( 3.3 \times 10^{-4} \), 5.0, and 0.70 in the 65-nm technology used for this paper. The transition time \( \tau \) is interconnect RC dependent, which can be simply denoted as using the textbook Elmore model

\[
t_L = R_{eq} (C_W + C_L) + R_W \left( \frac{C_W}{2} + C_L \right).
\]

Using the sensitivity factor from Section IV-A, the overall BTI frequency degradation for long interconnects can be derived as

\[
\frac{(\Delta f)}{f} = \alpha \frac{(\Delta f)}{f}_{\text{BTI}}
\]

\[
= \frac{R_{eq} (C_W + C_L)}{R_{eq} (C_W + C_L) + R_W (C_W + C_L)}
\]

\[
= \frac{(V_{str} - V_T)^{-0.5} e^{(-\frac{V_{str}}{E_d})} e^{(-\frac{V_{str}}{E_d})^n}}{1 - B \left( \frac{21m_n}{\tau} \right)^f}.
\]
Arrhenius dependency:

\[
\left( \frac{\Delta f}{f} \right)_{\text{HCI}} = \frac{C}{V_{\text{str}} - V_t} e^{\left( \frac{E_b}{kT} \right)} \left( \frac{V_{\text{eff}}}{U_0} \right)^m \tag{9}
\]

where \( C, D, \) and \( m \) are the empirical parameters, \( t_{\text{eff}} \) is the effective HCI stress time, which is directly related to the signal transition time, and \( V_{\text{eff}} \) is the effective drain to source voltage during stress. The experimental and simulation results in Section III show that both the effective stress voltage and effective stress time depend on the interconnect RC load. As noted earlier, a long interconnect causes the output signal voltage to be divided between the interconnect resistance \( R_W \) and the transistor drain-to-source \( (V_{ds}) \) while charging and discharging. Therefore, the effective HCI stress voltage can be approximated as

\[
V_{\text{eff}} = \frac{R_{\text{eq}}}{R_{\text{eq}} + R_W} V_{\text{str}} \tag{10}
\]

where \( R_{\text{eq}} \) is the equivalent driver resistance, \( R_W \) is the interconnect resistance, and \( V_{\text{str}} \) is the HCI stress voltage in a path without interconnect.

Under the assumption that the HCI stress time is proportional to the transition time, the effective stress time considering interconnect impact can be expressed as

\[
t_{\text{eff}} = \frac{R_{\text{eq}} (C_W + C_L) + R_W \left( \frac{C_W}{2} + C_L \right)}{R_{\text{eq}} C_L} t \tag{11}
\]

Here, \( t \) is the time a device in a logic dominated path is under HCI stress. Finally, the HCI-induced frequency degradation can be derived using the sensitivity factor introduced in Section IV-A.

\[
\left( \frac{\Delta f}{f} \right)_{\text{HCI}_{\text{interconnect}}} = \alpha \left( \frac{\Delta f}{f} \right)_{\text{HCI}}
\]

\[
= \frac{R_{\text{eq}} (C_W + C_L) + R_W \left( \frac{C_W}{2} + C_L \right)}{V_{\text{str}} - V_t} \cdot \frac{C}{V_{\text{str}} - V_t} e^{\left( \frac{E_b}{kT} \right)} \left( \frac{V_{\text{eff}}}{U_0} \right)^m \tag{12}
\]

The results from (8) and (12) are overlaid onto the measured data in Figs. 9 and 12 showing good agreement with actual hardware data. This verifies that the equations based on the various interconnect parameters are capable of modeling the monotonic behavior of BTI and nonmonotonic behavior of HCI for a wide range of interconnect lengths. Note that both models capture the voltage and temperature dependencies using the voltage acceleration factor \( \alpha \), \( D \) and activation energy \( E_a \), \( E_b \), respectively. The models with parameters used are summarized in Fig. 16.

V. DESIGN METHODOLOGY AND CIRCUIT IMPLICATIONS

In this section, we present a closed-loop modeling methodology that uses the aforementioned circuit aging models for accurate prediction of interconnect performance degradation. The impact of interconnect geometry on the overall performance degradation was also examined. Finally, we show a case study of a global interconnect path design, which uses the proposed closed-loop design methodology to determine the optimal repeater count and sizing considering BTI and HCI effects.

A. Closed-Loop Aging Calculation for Interconnect Paths

For logic dominated paths, the delay degradation can be simulated by simply plugging in parameters such as stress volt-
Fig. 19. Dependence of (a) BTI and (b) HCI-induced frequency shift on interconnect width and length.
and metal layer. Since the interconnect resistance $R_W$ and capacitance $C_W$ can be expressed using these interconnect geometrical parameters, we can apply the proposed methodology to a wide range of interconnect designs (e.g., clock network, global bus, memory, and I/O) across different process technologies. To demonstrate the practicality of our approach, we provide an example wherein the impact of interconnect wire’s side plates while considering different metal layers of this technology are also listed on the same figure for reader’s reference.

Since the length dependency was already discussed extensively in Section III, here we briefly comment on the width dependency of BTI and HCI degradation. Fig. 19(a) shows that a buffer driving a wider wire results in a lesser amount of BTI degradation. This is due to the increased signal delay, which causes the effective BTI stress time ($t_L$ in Fig. 10) to go down. Contrary to the BTI results, HCI-induced frequency degradation increases with a wider wire due to the higher effective stress voltage ($V_{eff}$ in Fig. 13), as shown in Fig. 19(b). Note that the aging analysis provided in this section must be considered in conjunction with metrics such as performance and power consumption, which are perhaps the primary design considerations.

C. Interconnect Path Design With Aging Consideration

To show the application of the proposed aging models on real circuits, this section describes a methodology for estimating the optimal number of repeaters and the sizing of each repeater. To reduce the overall delay of a global interconnect path, signal wires are typically broken into shorter segments separated by repeaters. The total propagation delay of the signal path can be expressed as

$$t_d = N \left( R_W \left( \frac{l}{N} C_W + C_L (1 + t_{int}) \right) + R_W \left( \frac{l}{N} C_W + C_L \right) \right).$$

Here, $t_{int}$ is the delay of an unloaded buffer, $l$ is the total wire length, and $N$ is the number of repeaters inserted. For a fixed number of repeaters, the transistor delay [first term in (13)] becomes a larger portion of the overall propagation delay for an interconnect path with smaller drivers. This means that an interconnect path with numerous small drivers are more susceptible to aging effects compared to that with a few large drivers. This behavior is verified through the simulations results in Fig. 20(a), which shows larger delay degradation for an interconnect path with smaller drivers. From the figure, we can clearly observe that a driver size of $W_P/W_N = 10/5 \mu m$ achieves the minimum delay for a fresh circuit while $W_P/W_N = 12/6 \mu m$ is required for minimum delay in the presence of device aging. We also varied the number of repeaters while fixing the driver size to study its impact on overall frequency degradation. The results given in Fig. 20(b) show worse delay degradation for an interconnect path with a larger number of repeaters. This can be attributed to the transistor delay dominating the overall path delay as the number of repeaters is increased. Our results based on the stress condition denoted in Fig. 20(b) also show that the optimal number of repeaters is 12 when aging is considered versus 14 when aging is not considered.

VI. CONCLUSION

This paper explores, for the first time, the detailed aging behavior of interconnect paths. The degradation in interconnect performance caused by BTI and HCI in the driver circuit
exhibits a strong dependency on the interconnect RC parameters. This dependence must be thoroughly understood to build accurate aging models applicable to interconnect designs in advanced technologies. In this paper, we first demonstrated a 65-nm interconnect odometer test vehicle capable of accurately measuring the frequency degradation of signal paths with different interconnect lengths. Our previous all-in-one odometer concept was adopted to separately measure BTI and HCI aging. The measurement interrupt was kept below 3 μs to avoid any unwanted BTI recovery. Experimental results show that the frequency degradation caused by BTI decreases with increasing interconnect length, while the HCl-induced degradation peaks at around 500 μm. This difference in the interconnect dependencies were explained using circuit simulations that account for the effective stress time and stress voltage during signal transitions. Simple circuit aging models were developed and compared against the measured data. We next proposed a closed-loop modeling methodology, which precisely captures the interplay between the interconnect RC parameters and the change in stress condition. Finally, a case study of the closed-loop model was shown where the delay shift for a practical interconnect path was minimized using optimal number of buffers.

REFERENCES


Dong Jiao (S’09–M’12) received the B.S. degree from Tsinghua University, Beijing, China, in 2006, and the M.S. and Ph.D. degrees in electrical engineering from the University of Minnesota, Minneapolis, MN, USA, in 2006, 2009 and 2011, respectively.

He was an Intern with Seagate in 2008 and Samsung Semiconductor Inc., from 2010 to 2011. He joined Samsung Semiconductor Inc., in 2011, working on circuit design techniques for reliability and PVT variation in advanced technology nodes. Since 2012, he has been with Google Inc. His current research interests include on-chip variation, reliability, and power integrity for mixed-signal ICs and SRAM design.

Chris H. Kim (M’04–SM’10) received the B.S. and M.S. degrees from Seoul National University, Seoul, Korea, and the Ph.D. degree from Purdue University, West Lafayette, IN, USA.

He spent a year with Intel Corporation, where he performed research on variation-tolerant circuits, on-die leakage sensor design, and crosstalk noise analysis. He joined the Faculty of Electrical and Computer Engineering with the University of Minnesota, Minneapolis, MN, USA, in 2004, where he is currently an Associate Professor. He has authored and co-authored more than 100 journal and conference papers and has served as the Technical Program Committee Chair for the 2010 International Symposium on Low Power Electronics and Design (ISLPED). His current research interests include digital, mixed-signal, and memory circuit design in silicon and non-silicon (organic TFT and spin) technologies.

Prof. Kim is the recipient of an NSF CAREER Award, a McKnight Foundation Land-Grant Professorship, a 3M Nontenured Faculty Award, DAC/ISSCC Student Design Contest Awards, IBM Faculty Partnership Awards, an IEEE Circuits and Systems Society Outstanding Young Author Award, ISLPED Low Power Design Contest Awards, and an Intel Ph.D. Fellowship.