nature nanotechnology

LETTERS

PUBLISHED ONLINE: 7 SEPTEMBER 2015 | DOI: 10.1038/NNANO.2015.197

Solution-processed carbon nanotube thin-film complementary static random access memory

Michael L. Geier[1], Julian J. McMorrow[1], Weichao Xu[2], Jian Zhu[1], Chris H. Kim[2], Tobin J. Marks[1,3] and Mark C. Hersam[1,3]*

Over the past two decades, extensive research on single-walled carbon nanotubes (SWCNTs) has elucidated their many extraordinary properties[1–3], making them one of the most promising candidates for solution-processable, high-performance integrated circuits[4,5]. In particular, advances in the enrichment of high-purity semiconducting SWCNTs[6–8] have enabled recent circuit demonstrations including synchronous digital logic[9], flexible electronics[10–14] and high-frequency applications[15]. However, due to the stringent requirements of the transistors used in complementary metal–oxide–semiconductor (CMOS) logic as well as the absence of sufficiently stable and spatially homogeneous SWCNT thin-film transistors[16–18], the development of large-scale SWCNT CMOS integrated circuits has been limited in both complexity and functionality[19–21]. Here, we demonstrate the stable and uniform electronic performance of complementary p-type and n-type SWCNT thin-film transistors by controlling adsorbed atmospheric dopants and incorporating robust encapsulation layers. Based on these complementary SWCNT thin-film transistors, we simulate, design and fabricate arrays of low-power static random access memory circuits, achieving large-scale integration for the first time based on solution-processed semiconductors.

Typically, complex large-area circuits based on solution-processed semiconductors employ only unipolar logic[22,23], which dissipates significantly more power than CMOS circuits based on enhancement mode p-type and n-type thin-film transistors (TFTs), further limiting large-scale integration. A variety of demonstrations of simple CMOS circuits such as inverters and ring oscillators have used materials such as III–V nanowires[24], polymers[25] and hybrid carbon nanotube/oxide combinations[14,20], but these circuits have all been limited in scale and complexity. Consequently, the foundational elements of modern-day computing, such as CMOS static random access memory (SRAM), have not yet been demonstrated with solution-processed TFTs. In this Letter, we perform a statistical analysis of large-area arrays of both p-type and n-type SWCNT TFTs to quantify their spatial non-uniformity and temporal degradation as a function of ambient exposure, and demonstrate a process that stabilizes and homogenizes the advantageous electronic properties necessary for CMOS logic circuit operation. With statistically significant data sets gathered from hundreds of SWCNT TFTs fabricated over large areas, accurate TFT models are developed that subsequently enable the simulation, design and fabrication of complex integrated CMOS SRAM circuits.

The predictability and stability of TFT electronic properties are essential to the design, fabrication and operation of large-scale integrated circuits. Previous studies have shown that adsorbed O_2 is a strong p-type dopant for SWCNTs[26,27] and that exposure of SWCNT transistors to ambient conditions leads to deleterious shifts in threshold voltage V_T (ref. 28). To control adsorbed atmospheric dopants, device structures and fabrication methods similar to previous p-type and n-type SWCNT TFTs[21,29] were modified to encapsulate the doped SWCNT channel networks as shown in Fig. 1. After fabricating unencapsulated SWCNT TFTs, the devices were vacuum annealed for 1 h at 230 °C to remove residual adsorbed species. The TFTs were then spin-coated with photoresist (Shipley S1813) in an N_2 atmosphere glovebox without exposure to ambient atmosphere, resulting in p-type SWCNT TFTs. The photoresist serves multiple purposes concurrently, including acting as a p-type dopant, intermediate encapsulant and atomic layer deposition (ALD) growth seeding layer for the p-type SWCNT TFTs. After photolithographically exposing the channels of the n-type SWCNT TFTs, the substrate was again vacuum annealed for 1 h at 230 °C. The exposed SWCNT TFTs were then n-type doped by spin-coating benzyl viologen in an N_2 atmosphere glovebox without exposure to ambient atmosphere. In addition to n-type doping the SWCNTs, the benzyl viologen layer simultaneously serves as the seeding layer for conformal ALD growth of the final encapsulation layer of 50-nm-thick Al_2O_3. The combination of dopant material layers and conformal ALD results in effective encapsulation for both p-type and n-type SWCNT TFTs. Further details on the materials and fabrication methods are provided in Supplementary Sections 1 and 2.

The electronic transport properties of the SWCNT TFTs with and without Al_2O_3 encapsulation layers were characterized under ambient conditions by repeatedly measuring individual TFTs over the course of several hours, as well as sampling more than 800 TFTs and testing each one once for a similar elapsed testing time. The gate–source voltage (V_{GS}) ranged from $V_{GS} = 0$ V to $|V_{DD}|$ (where V_{DD} is the supply voltage), which is the relevant operating voltage window of transistors in CMOS logic circuits. The transfer curves for encapsulated TFTs, measured after initial exposure to air and after 7 h of repeated testing in ambient atmosphere, are shown in Fig. 2a. For both encapsulated p-type and n-type SWCNT TFTs, enhanced or stable electronic properties are observed over the 7 h testing period. Figure 2b, in contrast, presents the response of unencapsulated p-type SWCNT TFTs, which shows significant deterioration of device metrics such as the I_{on}/I_{off} current ratio, where I_{on} is defined as the drain–source current (I_{DS}) at $V_{GS} = |V_{DD}|$, and I_{off} is defined as I_{DS} when $V_{GS} = 0$ V. Over 5 h, the I_{on}/I_{off} current ratio for both unencapsulated p-type and n-type SWCNT TFTs decreases by about three orders of magnitude, whereas the encapsulated devices show stable or enhanced I_{on}/I_{off} ratios (Fig. 2c,d).

[1]Department of Materials Science and Engineering, Northwestern University, Evanston, Illinois 60208, USA. [2]Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, Minnesota 55455, USA. [3]Department of Chemistry, Northwestern University, Evanston, Illinois 60208, USA. *e-mail: m-hersam@northwestern.edu

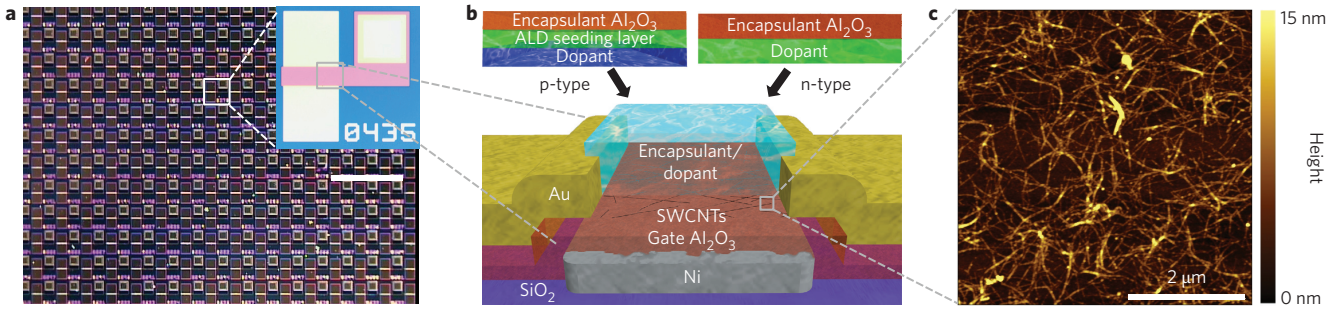

Figure 1 | Complementary SWCNT TFT structures. a, Optical micrographs of the fabricated SWCNT TFT device with a channel width of 150 μm and length of 50 μm (inset) and an array of SWCNT TFTs. Scale bar, 1 mm. **b**, Schematic cross-section of a SWCNT TFT fabricated with a SiO_2/Si substrate, local Ni (25 nm) gate, Al_2O_3 (10 nm) gate dielectric, Cr/Au (1 nm/50 nm) source–drain bottom contacts and >99% semiconducting SWCNT thin films. For p-type SWCNT TFTs, the remaining layers are the p-type dopant (~1.3 μm Shipley S1813 photoresist), an ALD seeding layer (benzyl viologen) and a final encapsulation layer (50 nm Al_2O_3). For the n-type SWCNT TFTs, the top layers consist of n-type dopant (~100 nm benzyl viologen) and the final encapsulation layer (50 nm Al_2O_3). **c**, Atomic force micrograph of the random network SWCNT morphology in the TFT channel with a linear density of ~10 SWCNTs per μm.

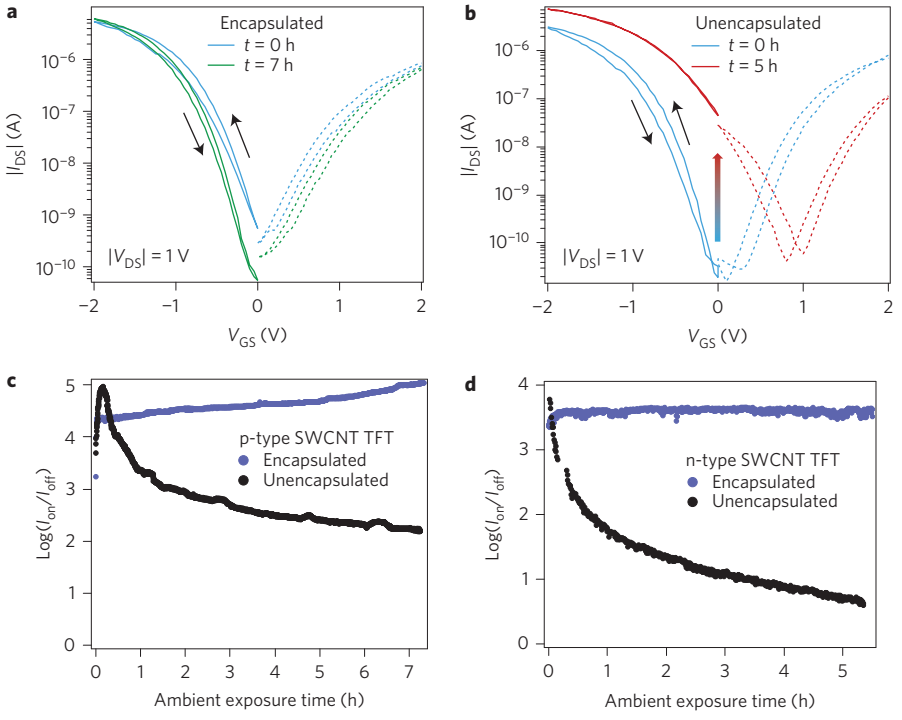

Figure 2 | Time stability of SWCNT TFT electrical properties. a, Log-linear transfer (I_{DS}–V_{GS}) curves for encapsulated p-type (solid lines) and n-type (dashed lines) SWCNT TFTs measured after initial exposure to atmosphere (blue) and after 7 h of ambient exposure (green) at $|V_{DS}| = 1$ V. **b**, Log-linear transfer (I_{DS}–V_{GS}) curves for unencapsulated p-type (solid lines) and n-type (dashed lines) SWCNT TFTs measured after initial exposure to atmosphere (blue) and after 5 h of atmospheric exposure (red), with the change in I_{off} indicated by the arrow (red/blue). **c**,**d**, $Log_{10}(I_{on}/I_{off})$ of p-type (**c**) and n-type (**d**) SWCNT TFTs as a function of ambient exposure time for repeated transfer measurements of a single encapsulated (purple) and unencapsulated (black) SWCNT TFT, where I_{on} is defined as $|I_{DS}|$ at $|V_{GS}| = 2$ V and I_{off} is defined as $|I_{DS}|$ at $V_{GS} = 0$ V.

Encapsulation also improves the spatial homogeneity of the SWCNT TFT device metrics, as shown in Fig. 3. In this case, large numbers of TFTs are probed over large areas such that each TFT is measured only once within the operating voltages defined above. Figure 3a,b shows the $\log_{10}(I_{on}/I_{off})$ distributions for p-type and n-type encapsulated and unencapsulated SWCNT TFTs. Both p-type and n-type encapsulated SWCNT TFTs exhibit high $\log_{10}(I_{on}/I_{off})$, with average values of 3.49 ± 0.15 (p-type) and 3.48 ± 0.53 (n-type) for more than 800 SWCNT TFTs. In contrast, unencapsulated TFTs have low $\log_{10}(I_{on}/I_{off})$ average values of 1.82 ± 0.38 (p-type) and 1.39 ± 0.77 (n-type) and possess long tails and high standard deviations in their $\log_{10}(I_{on}/I_{off})$ distributions. The tails in these distributions can be at least partially explained by time-dependent changes in the unencapsulated devices (Supplementary Fig. 3). Importantly, the present I_{on}/I_{off} ratios for encapsulated SWCNT TFTs are suitable for CMOS circuit operation, whereas unencapsulated TFTs are highly variable and therefore unsuitable for large-area CMOS circuit integration.

The observed decrease in I_{on}/I_{off} current ratios of unencapsulated SWCNT TFTs is attributed to the dynamic evolution of specific charge transport metrics. For p-type SWCNT TFTs, the increase in subthreshold swing is the primary source of the deterioration

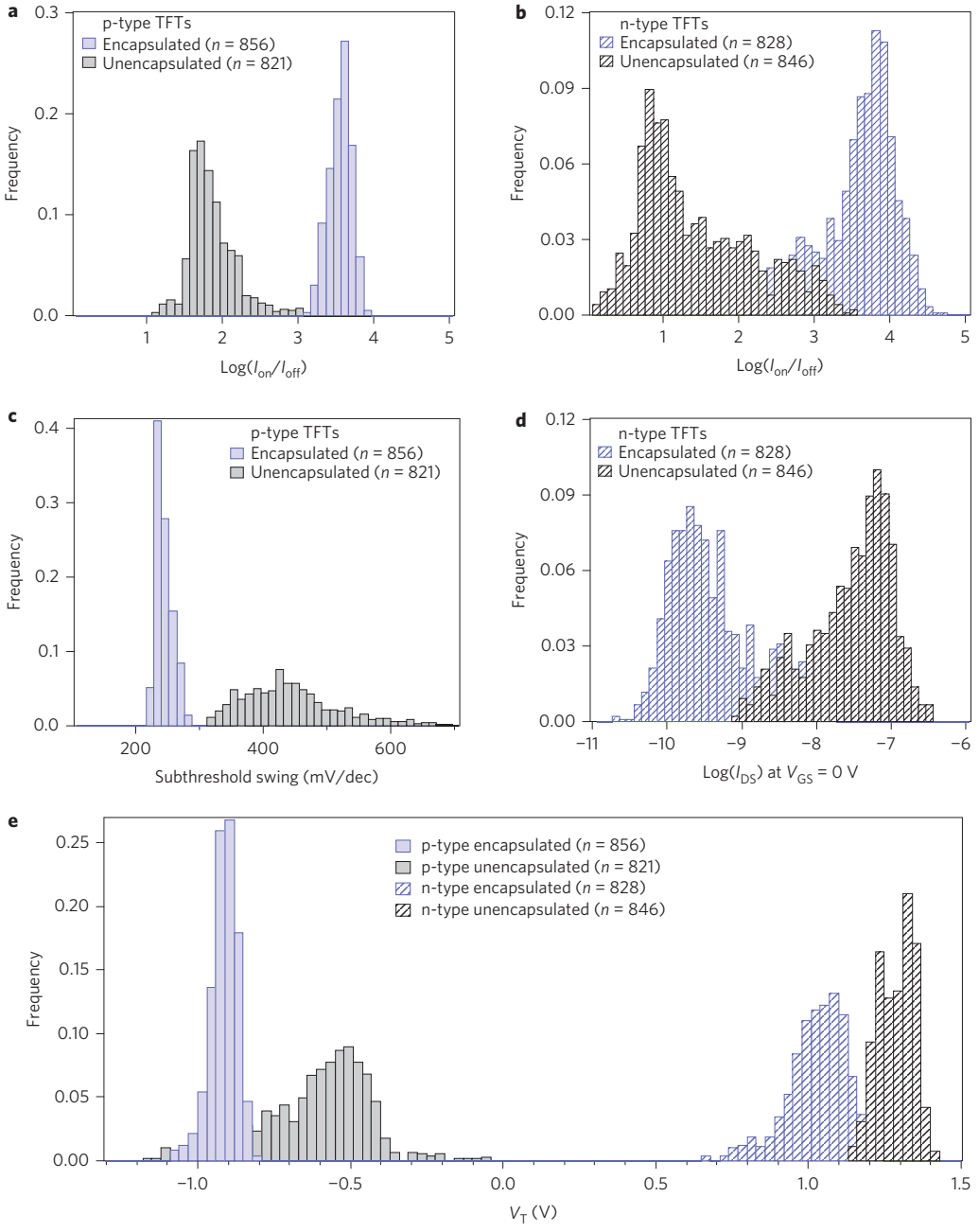

Figure 3 | Large sample statistics of SWCNT TFT electronic properties for $|V_{DS}| = 1$ V. a,**b**, $Log_{10}(I_{on}/I_{off})$ for encapsulated (purple) and unencapsulated (black) p-type and n-type SWCNT TFTs. **c**, Subthreshold swing for encapsulated (purple) and unencapsulated (black) p-type SWCNT TFTs. **d**, $Log_{10}(I_{DS})$ when $V_{GS} = 0$ V for encapsulated (purple) and unencapsulated (black) n-type TFTs. **e**, Threshold voltage for encapsulated (purple) and unencapsulated (black) p-type (solid) and n-type (striped) SWCNT TFTs. *n*, number of devices tested.

in functionality. In contrast, the encapsulated p-type SWCNT TFTs shown in Fig. 3c exhibit low and narrowly distributed subthreshold swings of 236 ± 13 mV per decade, unlike the unencapsulated TFTs, which exhibit high and broadly distributed subthreshold swings of 483 ± 146 mV per decade. Degradation in subthreshold swing is likely due to interfacial charge trapping. Specifically, for p-type SWCNT TFTs, the presence of oxygen and water in backgated devices has been shown to create charge trapping electrochemical reactions[30], which is consistent with the degradation observed in unencapsulated p-type SWCNT TFTs. For n-type SWCNT TFTs, the increase in I_{DS} at $V_{GS} = 0$ V is the main cause of the decreased I_{on}/I_{off} ratio. Figure 3d shows the distribution of $\log_{10}(I_{DS})$ at $V_{GS} = 0$ V, where encapsulated n-type SWCNT TFTs have an average $\log_{10}(I_{off})$ of −9.42 ± 0.60 while unencapsulated TFTs have an average $\log_{10}(I_{off})$ of −7.60 ± 0.56. This approximately two orders of magnitude increase accounts for the majority of the decreased I_{on}/I_{off} ratio for unencapsulated n-type SWCNT TFTs and indicates enhanced p-type transport for unencapsulated n-type SWCNT TFTs that results from the diffusion of p-type atmospheric dopants through the benzyl viologen layer. Overall, the decrease in the unencapsulated p-type SWCNT TFT I_{on}/I_{off} ratio and increase in I_{DS} at $V_{GS} = 0$ V for unencapsulated n-type SWCNT TFTs imply increased p-type doping over time, consistent with the accumulation of atmospheric dopants[28].

Shifts in the threshold voltage (V_T) also contribute to the deterioration of I_{on}/I_{off} ratios over the CMOS operating voltage window.

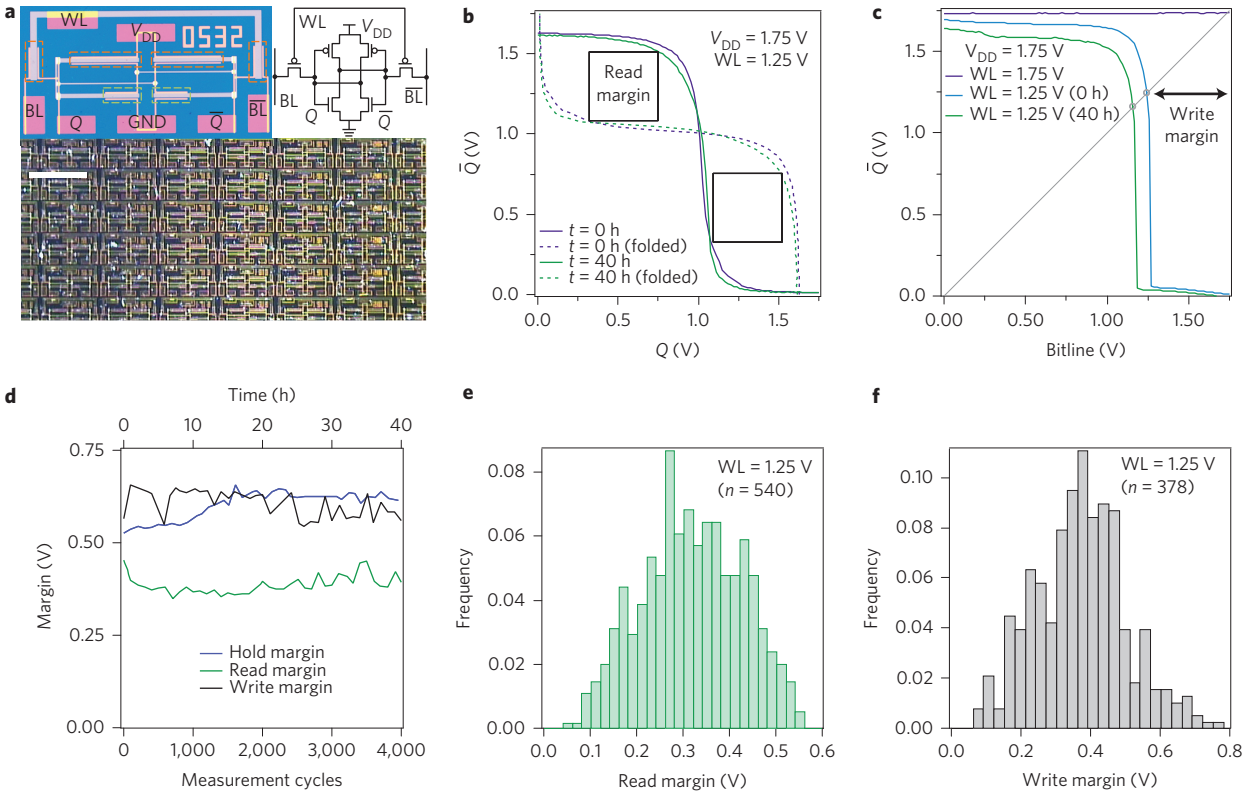

Figure 4 | SWCNT CMOS SRAM circuit characterization. a, Optical micrograph of a fabricated SWCNT CMOS SRAM cell and corresponding circuit diagram (inset image size, 1 × 0.6 mm) showing the p-type SWCNT TFTs (orange dashed boxes) and n-type SWCNT TFTs (green dashed boxes), as well as an optical micrograph of the large-area array of SWCNT CMOS SRAM cells. Scale bar, 1 mm. **b**, Read margin measurements (solid lines) and folded read margin measurements using inverted axes (dashed lines) for the initial measurement (purple) and after 40 h (4,000 cycles) of continuous ambient testing (green). **c**, Hold operation for the wordline (WL) voltage set to V_{DD}, showing no write event (purple), and write operation for the wordline voltage set to 1.25 V for initial (blue) and after 40 h (4,000 cycles) of continuous ambient testing (green) with the intersection $\bar{Q}$ = bitline (BL) (grey). **d**, Read, write and hold noise margin stability testing for SWCNT CMOS SRAM cells over 40 h (4,000 cycles) of ambient testing. **e**,**f**, Histograms of read margin (**e**) and write margin (**f**) for hundreds of individual SWCNT CMOS SRAM cells.

V_T is calculated by linearly extrapolating from the point of maximum transconductance, and the encapsulated SWCNT TFT threshold voltages are more symmetric about $V_{GS} = 0$ V than those for unencapsulated TFTs, which are shifted towards more positive voltages (Fig. 3e). In particular, the average V_T for encapsulated p-type SWCNT TFTs is -0.93 ± 0.05 V, while the average V_T for unencapsulated p-type SWCNT TFTs is -0.62 ± 0.18 V. Similarly, the average V_T for encapsulated n-type SWCNT TFTs is 1.01 ± 0.10 V, while the average V_T for unencapsulated n-type SWCNT TFTs is 1.26 ± 0.06 V. Overall, the encapsulated p-type and n-type SWCNT TFTs have threshold voltage magnitudes near 1 V, while those of unencapsulated TFTs are both shifted ~0.3 V towards more positive voltages, leading to unbalanced transfer characteristics in the symmetric operating voltage window of CMOS circuits. Previously reported CMOS-based circuits have been fabricated on single aligned SWCNTs[31] that use a contact metal doping strategy (Sc and Pd), but these devices have suffered from asymmetric threshold voltages. The encapsulated CMOS transistors demonstrated here are more symmetric around 0 V and suggest a strategy for achieving symmetric V_T in more aggressively scaled devices.

The consistency of the device metric statistics for encapsulated SWCNT TFTs enables the development of transistor models that facilitate the simulation, design and implementation of more complex CMOS circuits. To demonstrate the efficacy of this approach, CMOS SRAM circuits were fabricated from large-area arrays of SWCNT TFTs. Figure 4a presents an optical micrograph of an array of CMOS SRAM cells, as well as a detailed image of a single CMOS SRAM cell with its corresponding circuit diagram (inset). The SRAM cell is composed of two cross-coupled CMOS inverters forming a latch circuit and two individual p-type access SWCNT TFTs tied to bitlines and wordlines. To ensure proper operation of the circuit, the relative transistor sizes of the pull-up, pull-down and access transistors were optimized based on simulations informed by SWCNT TFT models. Details of the transistor sizes and the results of the circuit simulations are provided in Supplementary Fig. 4. Following fabrication, these devices displayed full SRAM read, write and hold capabilities at a low V_{DD} of 1.75 V, while consuming between 0.1 and 10 nW of power during static hold operations.

The key figures of merit for SRAM cells are the read, write and hold operation noise margins, which must exceed zero to be considered operational. Figure 4b shows the voltage transfer characteristics for an SRAM read operation where the wordline is set to 1.25 V, allowing cell data to be transferred out to the bitlines. For the write operation, data must be transferred from the bitlines into the cell, and Fig. 4c shows stable write operation for the same testing conditions. Figure 4c also shows the hold operation, when the wordline is set to V_{DD}, which isolates the cell from the bitlines and allows the cell to maintain its data despite the activity of the bitlines. This operation is summarized in Fig. 4d where the read margin, write margin and hold margin are shown to remain stable after a minimum of 4,000 measurement sweeps taken over 40 h at a sweep frequency of 0.1 Hz under ambient conditions.

Many of the SRAM cells have demonstrated stability over 12,000 measurement cycles and 120 h of ambient operation with a cumulative exposure of several weeks to ambient conditions. Additionally, statistical analysis of a large number of spatially distributed SRAM cells shows an average read margin of 0.32 ± 0.11 V (Fig. 4e) and write margin of 0.37 ± 0.13 V (Fig. 4f), demonstrating stable read and write operations of hundreds of SRAM cells distributed over a large area. The variability and deviation from modelled read and write margins are a direct consequence of variability in the charge transport properties of the constituent transistors. Encapsulation has greatly reduced the variability of these properties, and further reductions in variability could be gained by optimizing all fabrication procedures in a cleanroom using process equipment dedicated to the fabrication of SWCNT TFTs.

In summary, we have demonstrated a general approach for the fabrication of SWCNT TFTs with properties suitable for large-area CMOS logic circuits. By controlling adsorbed dopants and encapsulation of active materials, air-stable CMOS SWCNT TFTs are demonstrated with high temporal stability and spatial uniformity. These devices are then incorporated into circuit simulations necessary for the design and demonstration of fully functional SWCNT-based CMOS SRAM circuits over large areas. Overall, the approach described here provides a pathway for the future design and fabrication of complex solution-processable, large-area, energy-efficient CMOS logic devices. These features, when combined with recent advances in flexible and printed electronics[10–14,20], have potentially wide-ranging implications for high-performance portable and wearable electronics.

Methods

Methods and any associated references are available in the online version of the paper.

Received 31 March 2015; accepted 31 July 2015;
published online 7 September 2015

References

1. De Volder, M. F. L., Tawfick, S. H., Baughman, R. H. & Hart, A. J. Carbon nanotubes: present and future commercial applications. *Science* **339,** 535–539 (2013).
2. Jariwala, D., Sangwan, V. K., Lauhon, L. J., Marks, T. J. & Hersam, M. C. Carbon nanomaterials for electronics, optoelectronics, photovoltaics, and sensing. *Chem. Soc. Rev.* **42,** 2824–2860 (2013).
3. Tulevski, G. S. *et al.* Toward high-performance digital logic technology with carbon nanotubes. *ACS Nano* **8,** 8730–8745 (2014).
4. Sangwan, V. K. *et al.* Fundamental performance limits of carbon nanotube thin-film transistors achieved using hybrid molecular dielectrics. *ACS Nano* **6,** 7480–7488 (2012).
5. Ha, M. *et al.* Aerosol jet printed, low voltage, electrolyte gated carbon nanotube ring oscillators with sub-5 μs stage delays. *Nano Lett.* **13,** 954–960 (2013).
6. Hersam, M. C. Progress towards monodisperse single-walled carbon nanotubes. *Nature Nanotech.* **3,** 387–394 (2008).
7. Jin, S. H. *et al.* Using nanoscale thermocapillary flows to create arrays of purely semiconducting single-walled carbon nanotubes. *Nature Nanotech.* **8,** 347–355 (2013).
8. Arnold, M. S., Green, A. A., Hulvat, J. F., Stupp, S. I. & Hersam, M. C. Sorting carbon nanotubes by electronic structure using density differentiation. *Nature Nanotech.* **1,** 60–65 (2006).
9. Shulaker, M. M. *et al.* Carbon nanotube computer. *Nature* **501,** 526–530 (2013).
10. Rogers, J. A., Someya, T. & Huang, Y. Materials and mechanics for stretchable electronics. *Science* **327,** 1603–1607 (2010).
11. Sun, D.-M. *et al.* Mouldable all-carbon integrated circuits. *Nature Commun.* **4,** 2302 (2013).
12. Wang, C. *et al.* User-interactive electronic skin for instantaneous pressure visualization. *Nature Mater.* **12,** 899–904 (2013).
13. Cao, Q. *et al.* Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates. *Nature* **454,** 495–500 (2008).
14. Chen, H., Cao, Y., Zhang, J. & Zhou, C. Large-scale complementary macroelectronics using hybrid integration of carbon nanotubes and IGZO thin-film transistors. *Nature Commun.* **5,** 4097 (2014).
15. Steiner, M. *et al.* High-frequency performance of scaled carbon nanotube array field-effect transistors. *Appl. Phys. Lett.* **101,** 053123 (2012).
16. Franklin, A. D. *et al.* Carbon nanotube complementary wrap-gate transistors. *Nano Lett.* **13,** 2490–2495 (2013).
17. Franklin, A. D. *et al.* Variability in carbon nanotube transistors: improving device-to-device consistency. *ACS Nano* **6,** 1109–1115 (2012).
18. Park, H. *et al.* High-density integration of carbon nanotubes via chemical self-assembly. *Nature Nanotech.* **7,** 787–791 (2012).
19. Wang, H. *et al.* Tuning the threshold voltage of carbon nanotube transistors by n-type molecular doping for robust and flexible complementary circuits. *Proc. Natl Acad. Sci. USA* **111,** 4776–4781 (2014).
20. Kim, B. *et al.* High-speed, inkjet-printed carbon nanotube/zinc tin oxide hybrid complementary ring oscillators. *Nano Lett.* **14,** 3683–3687 (2014).
21. Lee, S. Y. *et al.* Scalable complementary logic gates with chemically doped semiconducting carbon nanotube transistors. *ACS Nano* **5,** 2369–2375 (2011).
22. Zhang, W. *et al.* A 1 V printed organic DRAM cell based on ion-gel gated transistors with a sub-10nW-per-cell refresh power. *Solid-State Circuits Conf. Dig. Tech. Papers* 326–328 (2011).
23. Myny, K. *et al.* Microprocessor on plastic foil. *IEEE J. Solid-State Circuits* **47,** 284–291 (2012).
24. Nah, J. *et al.* III–V complementary metal–oxide–semiconductor electronics on silicon substrates. *Nano Lett.* **12,** 3592–3595 (2012).
25. Sekitani, T., Zschieschang, U., Klauk, H. & Someya, T. Flexible organic transistors and circuits with extreme bending stability. *Nature Mater.* **9,** 1015–1022 (2010).
26. Derycke, V., Martel, R., Appenzeller, J. & Avouris, P. Controlling doping and carrier injection in carbon nanotube transistors. *Appl. Phys. Lett.* **80,** 2773–2775 (2002).
27. Collins, P. G., Bradley, K., Ishigami, M. & Zettl, A. Extreme oxygen sensitivity of electronic properties of carbon nanotubes. *Science* **287,** 1801–1804 (2000).
28. McClain, D. *et al.* Impact of oxygen adsorption on a population of mass produced carbon nanotube field effect transistors. *Carbon* **47,** 1493–1500 (2009).
29. Geier, M. L. *et al.* Subnanowatt carbon nanotube complementary logic enabled by threshold voltage control. *Nano Lett.* **13,** 4810–4814 (2013).
30. Aguirre, C. M. *et al.* The role of the oxygen/water redox couple in suppressing electron conduction in field-effect transistors. *Adv. Mater.* **21,** 3087–3091 (2009).
31. Ding, L. *et al.* CMOS-based carbon nanotube pass-transistor logic integrated circuits. *Nature Commun.* **3,** 677 (2012).

Acknowledgements

This work was supported by the Office of Naval Research MURI Program (N00014-11-1-0690) and the National Science Foundation (DMR-1006391, DMR-1121262 and CCF-0845605). A National Science Foundation Graduate Research Fellowship (M.L.G.) and a NASA Space Technology Research Fellowship (J.J.M.) are also acknowledged. Device fabrication was performed at the NUFAB cleanroom facility at Northwestern University.

Author contributions

M.L.G., W.X., C.H.K. and M.C.H. conceived the experiments. M.L.G. fabricated the device, performed the electrical measurements, carried out the atomic force microscopy characterization and analysed and interpreted the data with input from C.H.K., T.J.M. and M.C.H. J.J.M. designed the TFT photolithography mask and wrote the data analysis program. W.X. and C.H.K. modelled the TFTs and SRAM circuits, and designed the photolithography mask for the SRAM circuits. J.Z. sorted the semiconducting SWCNTs and quantified the purity using UV–vis spectroscopy. The manuscript was written with contributions from all authors, and all authors approved the final version of the manuscript.

Additional information

Supplementary information is available in the online version of the paper. Reprints and permissions information is available online at www.nature.com/reprints. Correspondence and requests for materials should be addressed to M.C.H.

Competing financial interests

The authors declare no competing financial interests.

Methods

SWCNT preparation and characterization. Detailed SWCNT sorting procedures are described in our previous publications[8,29]. Briefly, 45 mg SWCNTs (P2, Carbon Solutions) were added to 14.4 ml of 1% wt/vol aqueous sodium cholate (SC) and sodium dodecyl sulphate (SDS) 4:1 mixtures containing 32.5% wt/vol iodixanol, and sonicated in a horn ultrasonicator for 1 h. A mild centrifugation process (3,000 r.p.m. for 3 min) was used to remove large SWCNT aggregates and carbonaceous impurities before sorting. Next, 6 ml of this SWCNT dispersion was carefully injected below a 15 ml linear density gradient of 15–30% wt/vol iodixanol, and 0% wt/vol iodixanol solution was placed on top to fill the centrifuge tube. All solutions contained a 4:1 ratio of 1% wt/vol SC/SDS. The prepared gradients were ultracentrifuged for 14 h at 32,000 r.p.m. in an SW 32 rotor (Beckman Coulter). The enriched semiconducting SWCNTs were extracted at the top of the gradient by a piston gradient fractionator. Nominally 99% pure semiconducting SWCNTs (Supplementary Fig. 1) were used throughout the study.

TFT fabrication. Photolithography, thermal evaporation (25 nm of Ni) and lift-off in acetone were used to define local backgates. Conformal Al_2O_3 (10 nm) was deposited by ALD as the gate dielectric over the substrate using trimethylaluminium (TMA) and water at 150 °C (Savannah, Cambridge NanoTech). Gate contact vias were patterned by photolithography, followed by reactive ion etching (RIE) in an argon/CF_4 plasma atmosphere (100 W, 6 min, 40 s.c.c.m. Ar, 10 s.c.c.m. CF_4). The substrates were then transferred to a sputtering chamber (AJA Orion), where the substrate was biased under argon plasma to remove any residual surface oxide. A 30 nm layer of Ag was deposited by Ar sputtering to create a low resistance via to the Ni gate layer, followed by lift-off in acetone. Subsequent source–drain and contact pad layers were patterned by photolithography, and 1 nm/50 nm Cr/Au was deposited by thermal evaporation, followed by a lift-off in acetone. The sorted semiconducting SWCNTs were then deposited on a cellulose membrane (Millipore VMWP, 0.05 μm pore size) by vacuum filtration and rinsed thoroughly with deionized water. The cellulose membrane was dried, trimmed to the substrate size, wetted with isopropyl alcohol (IPA) to attach the membrane to the substrate by surface tension, gently stamped onto the substrate using filter paper to remove excess IPA, and finally submerged for at least 1 h in acetone to dissolve the filter membrane. Photolithography was used to cover the SWCNT TFT channel areas with Shipley S1813 photoresist. RIE in an oxygen plasma atmosphere (100 W, 15 s, 20 s.c.c.m. O_2) was subsequently used to define the TFT channel dimensions, after which the substrate was soaked in acetone for at least 1 h.

Doping and encapsulation. For p-type devices, the substrate was transferred to a nitrogen atmosphere glovebox and annealed in vacuum (30 mtorr) at 230 °C for 1 h. The p-type dopant (Shipley S1813 photoresist) was then deposited by spin-coating (3,000 r.p.m.) and annealed on a hot plate for 1 min at 115 °C inside the nitrogen glovebox. The substrate was patterned and developed in a cleanroom under ambient conditions, leaving photoresist over the p-type channels. The substrate was finally transferred to the nitrogen glovebox and again annealed in vacuum (30 mtorr) at 230 °C for 1 h.

Detailed n-type dopant preparation procedures are described in our previous publication[29]. The solution was spin-coated onto the substrate (1,000 r.p.m.), depositing ~100 nm of benzyl viologen, which was then annealed at 90 °C for 1 min in the nitrogen atmosphere glovebox. For final encapsulation, 50 nm Al_2O_3 was deposited over the substrate by ALD using TMA and water at 110 °C (Savannah, Cambridge NanoTech).

Device testing. The transfer, output, capacitance–voltage (C–V) and leakage characteristics of the TFTs were measured using a Keithley 4200-SCS system and a Cascade Microtech Summit 12000 semi-automatic ambient probe station. For TFT characteristics, all devices were measured by the native Keithley 4200 test software and analysed by a custom MATLAB script. SRAM cell measurements were performed using the semi-automatic probe station, custom Keithley 4200-SCS user test module and three external Keithley 2400 units. The testing setup was used to apply independent V_{DD}, wordline (WL), ground and sweep voltages (Q or bitline) and to measure the corresponding currents and output voltage ($\bar{Q}$).