# A Revolving Reference Odometer Circuit for BTI-Induced Frequency Fluctuation Measurements under Fast DVFS Transients

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***Abstract*—Bias Temperature Instability (BTI) under sub-microsecond DVFS transients manifests as instantaneous frequency degradation and recovery that has been predicted in past literature but has never been experimentally verified due to difficulty in obtaining high quality data. This work demonstrates a new odometer circuit specifically designed to measure the aforementioned effect. The basic idea is to use multiple fresh reference ring oscillators (ROSCs), which alternately take measurements to minimize any degradation in the reference ROSC's frequency and thereby enhancing the sampling time as well as the sampling resolution. Measurements from a 65nm test chip show excellent were taken under different voltage supply, temperature, stress time duration, and supply ramp time.**

**Keywords - BTI; revolving reference; odometer; stress; recovery; fast DVFS; guard band; on-chip monitor**

## I. INTRODUCTION

Modern processors employ power management techniques such as Dynamic Voltage and Frequency Scaling (DVFS), turbo and Near Threshold Voltage (NTV) operations, and aggressive power gating [1] for improved energy-efficiency. With the advent of integrated voltage regulators, voltage ramp-up or ramp-down times have been reduced from hundreds of microseconds (using off-chip voltage regulator module) to sub-microseconds. For example, Fig. 1 shows fast DVFS waveforms in a 22nm Intel Haswell processor enabled by multiple fully integrated voltage regulators, which can ramp voltage supply in a fraction of a microsecond [2]. Similarly, IBM's POWER8™ processor uses integrated voltage regulator module that has micro-regulators featuring sub-ns response times [3]. BTI stress and relaxation effects under such fast voltage transients can lead to unique reliability profiles that are different as compared to traditional system with either a single supply voltage or slow ramp times.

Fig. 2 illustrates what happens to circuit operating frequency during fast high-to-low and low-to-high voltage transients for a simple two level DVFS system. Let us assume that the processor is operating in a high VDD mode where BTI degradation is severe. As shown in the figure, circuit frequency decreases rapidly with time. When a fast voltage transition occurs from high VDD mode to low VDD mode, there is a

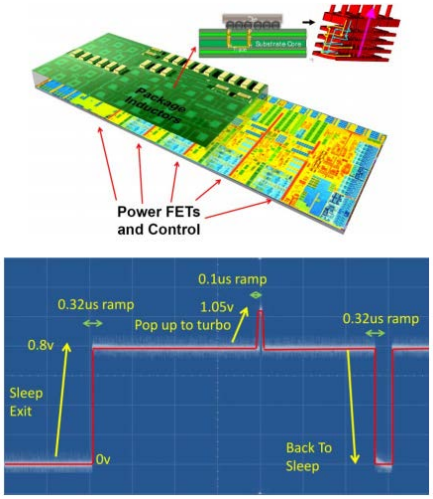



**Fig. 1. Fast DVFS with sub-microseond response times enabled by fully integrated voltage regulators in Intel's Haswell processor [2]**

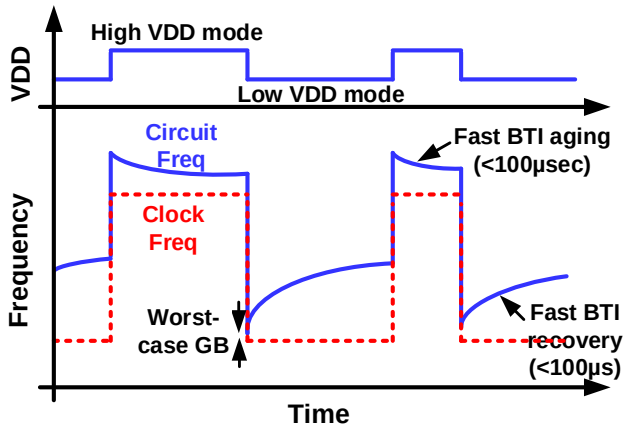



**Fig. 2. Frequency fluctuation due to fast BTI degradation and recovery under a two level DVFS scheme. GB in the figure stands for Guard Band.**

sudden drop in circuit frequency immediately after the transition due to the following three reasons; (i) the large degradation in the previous stage, (ii) the negligible amount of

recovery during the short voltage ramp period, (iii) and the higher sensitivity to degradation at low supply voltages. During the low VDD phase, the circuit frequency initially undergoes a fast recovery but will follow the new BTI degradation curve for longer stress times (not shown in Fig. 1 for simplicity). During low VDD to high VDD mode transition, the circuit frequency peaks instantaneously due to the recovery in the previous low VDD mode and then gradually reduces due to high VDD stress. During both these phases, worst-case guard-band occurs either right before or right after the high VDD to low VDD transition point. That is, the circuit frequency is lowest for the respective modes. Similarly, best case guard-band occurs during low VDD to high VDD transition, where circuit frequency is highest. It is important to know the amount of instantaneous frequency shifts due to BTI degradation and recovery under fast DVFS transients. This helps the designers determined the proper amount of frequency guard band in latest processors equipped with integrated voltage regulators.

Although there has been a theoretical analysis and modeling of the aforementioned effect [1], there has been no prior work providing silicon measurement of BTI-induced instantaneous frequency shift in a fast DVFS environment. Previous odometer circuits were not capable of continuously measuring the frequency fluctuation since they were designed for traditional stress experiments where a single data point separated by a long stress period was sufficient. In order to continuously measure the effects described in Fig. 2 from a real silicon chip, the new odometer circuit has to satisfy the following new constraints.

- The reference circuit must show negligible degradation when exposed to a high stress voltage for consecutive measurement periods.
- Sufficient on-chip memory must be available to store continuously sampled frequency shift values by the odometer circuit.

This work demonstrates a novel revolving reference odometer that can meet the above two requirements and collect high quality degradation data from real hardware. The remainder of the paper is organized as follows. Section II introduces the new odometer concept and describes the chip design. The measurement results are presented in section III. Section IV summarizes the contribution of this work.

## II. Revolving Reference Odometer

The proposed revolving reference odometer design is shown in Fig. 3, which is based on the tested-and-proven Beat Frequency Detection (BFD) technique [5, 6]. The original BFD system shown in Fig. 4 consists of two identical ring oscillators (ROSC), one stress and one fresh, with near identical frequencies. A flip flop used as phase comparator measures the frequency difference, also known as beat frequency. The final output count stored in the shift register corresponds to the number of reference ROSC periods within a single beat signal period.

In the proposed revolving reference odometer, several important changes have been made. As shown in Fig. 3, it uses eight reference ROSCs instead of one. The VDD and frequency plots show the eight reference ROSCs being fired sequentially and intermittently during measurement for three iterations to produce 24 x 8bit output counts (more iterations are possible with the addition of more on-chip memory) Temporarily storing sampled data on-chip avoids any delay for scanning out the output between successive measurements allowing consecutive samples with sub-1µs intervals to be captured. Note that the measurement time for taking a single sample is the product of ROSC period (2ns @ 1.4V) and the beat count (<150).

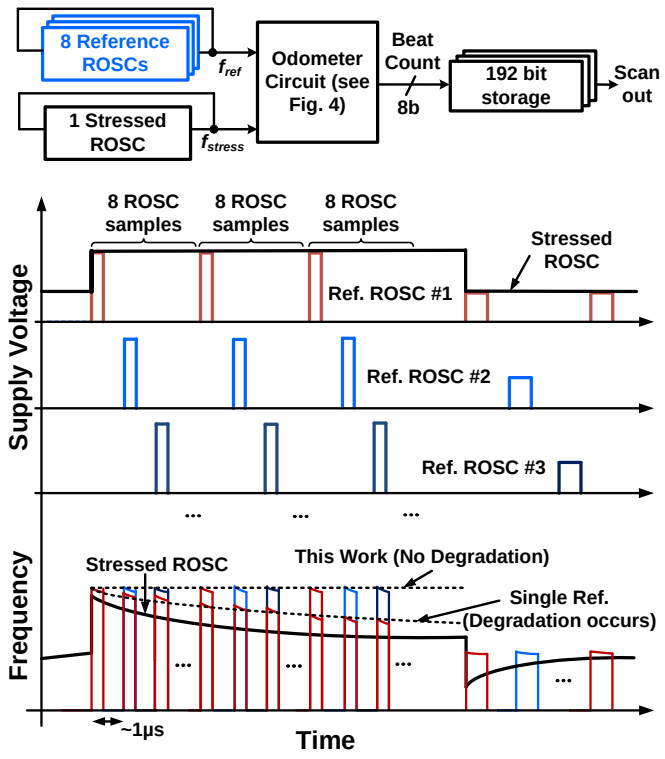



**Fig. 3. Proposed revolving reference odometer technique. Reference ROSCs are activated sequentially and intermittently to keep them fresh while subject to consecutive Vstress pulses.**

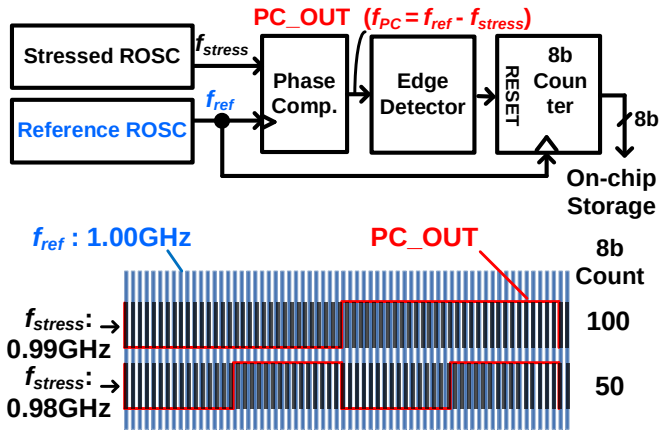



**Fig. 4. Previously proposed beat frequency odometer circuit achieves a high frequency shift precision (>0.01%) and a short (<1µs) measurement time for precise BTI measurements.**

While a single reference ROSC of the original odometer circuit would undergo considerable degradation especially when used continuously at higher VDD supply voltages,

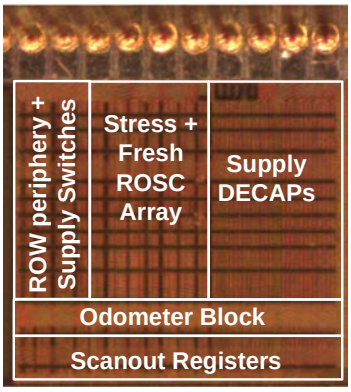
multiple revolving references produce negligible degradation making the frequency measurements more accurate. More specifically, the proposed design can measure the frequency shift within a 1µs delay between measurements, capturing the accurate value of worst-case and best-case guard band right after the supply transition. Note that unwanted aging in the reference ROSC can also be prevented in a single reference implementation by briefly turning off the reference ROSC before taking frequency measurements. However, the sampling interval must be sacrifice in this case to ensure that the reference ROSC is sufficiently recovered before taking the next measurement. We chose to implement 8 reference ROSCs considering the amount of recovery expected (>90% according to [7]), the compactness of the design, and the ease of frequency trimming. The frequency of all 8 ROSCs have to be trimmed individually using MOS capacitors connected to a ROSC stage so that the frequency difference between the reference and stressed ROSC is within 1-2% across different voltage and temperature conditions. This ensures that the frequency measurement resolution of the beat frequency technique is accurate while the supply voltage is being switched [5, 6, 7]. A higher number (e.g. 16 or 32) of reference ROSCs can be considered but this would require significant effort in finding the proper trimming configuration. Fig. 5 provides a comparison between the original odometer and proposed revolving reference odometer.

| | Previous Odometer | This Work |
|---|---|---|
| # of Stress ROSC | 1 | 1 |
| # of Ref. ROSC | 1 | 8 |
| On-chip Memory | 8 bits | 192 bits |
| Meas. Time | < 1µs | < 1µs |
| Minimum Sampling Interval | Limited by scan out time | 1µs (limited by meas. time) |
| Meas. Voltage | Nominal VDD (1.2V) | Any VDD (1.4V-0.8V) |

**Fig. 5. Comparison of previous vs. revolving reference odometer.**

## III. MEASUREMENT RESULTS

The die microphotograph and summary table of the 65nm test chip are given in Fig. 6. We measured the frequency shift in DVFS environment under different voltage and temperature condition. The measurement results are described as follows.




| Process | 65nm LP CMOS, 7M |
|---|---|
| Core / IO Supplies | 1.2V / 2.5V |
| High/Low Voltages | 2.5V, 2.0V/ 0.75V |
| DUT Type | Core devices |
| Δf Resolution | > 0.01% |
| Measure Time | < 1µs |
| Total Area | 410X380 µm$^2$ |

**Fig. 6. 65nm test chip die photo with chip summary.**

### A. *Measurement under Fast Voltage Transition*

When the supply voltage switches from low to high as shown in Fig. 7 (a), the frequency shift initially drops from 0.2% to 0.06%. This can explained using a simple equation for frequency shift

$$\frac{\Delta f}{f} = \frac{\Delta V_T}{V_{DD} - V_T} \quad (1)$$

Here, $V_T$ is the threshold voltage and $V_{DD}$ is the voltage supply. So, in a low to high transition of supply voltage, the degraded $\Delta V_T$ in the preceding high VDD mode coupled with the lower VDD manifests as a steep drop in frequency shift as seen in Fig. 7 (a). Similarly, in Fig. 7 (b), a steep jump from 0.2% to 0.7% was observed in the frequency shift after the transition.

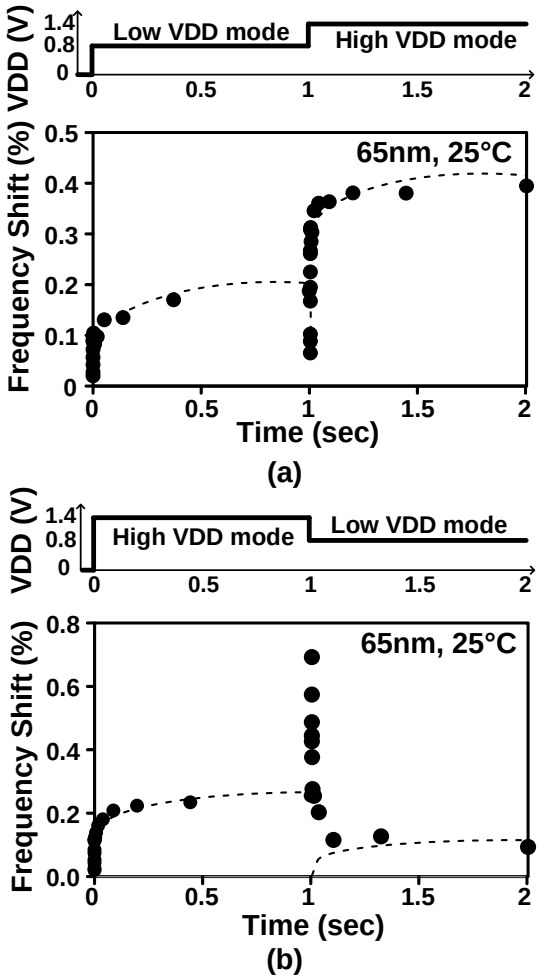



**Fig. 7. Measured frequency shift for (a) low to high voltage transition and (b) high to low voltage transition. First sample is taken within 1 microsecond of the supply voltage switching.**

Fig. 8 contrasts a series of six transitions between 1.4V/0.8V and 1.2V/0.8V at durations of 1 second each. The frequency shifts were observed to be higher for 1.4V/0.8V pair as the devices undergo more degradation and recovery at higher differential voltages as compared to 1.2V/0.8V transitions. Fig. 9 shows a comparison between multiple low voltages after transition from a 1.4V high supply voltage.

Confirming equation (1), the frequency shift jump was higher when stepping down the voltage to a lower voltage (i.e. 0.8V).

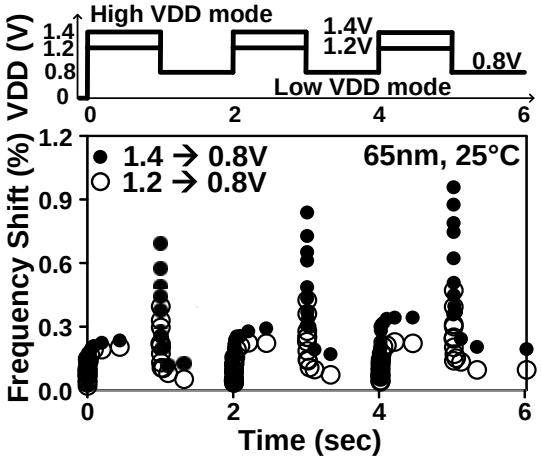



**Fig. 8. Measured frequency shift for multiple two level DVFS transitions.**

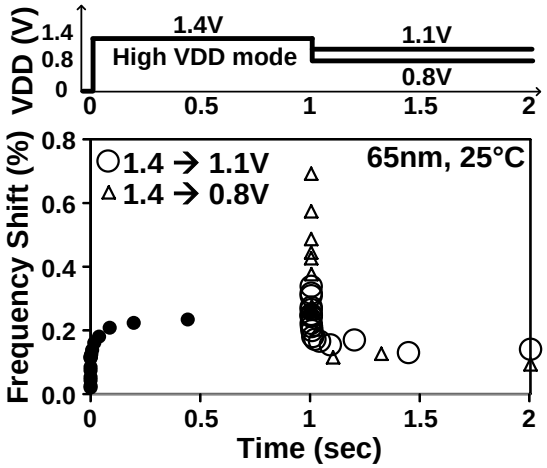



**Fig. 9. Measured frequency shift comparison for transition from 1.4V to two low voltage levels (i.e. 1.1V and 0.8V).**

*B. Temperature Effect on Frequency Fluctuation*

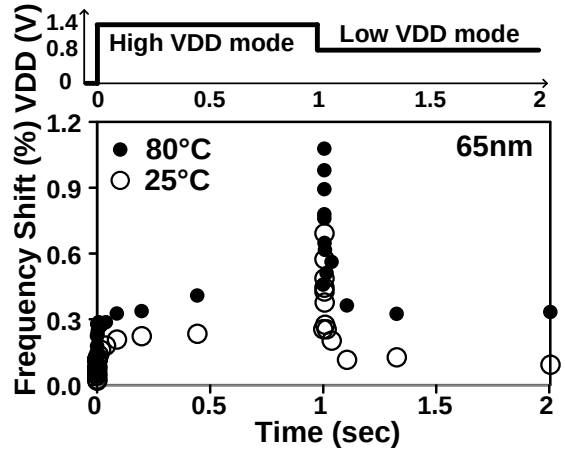



**Fig. 10. Measured frequency shift at 25ºC and 80ºC for 1.4V to 0.8V transition.**

Fig. 10 shows the temperature effect for a high voltage to low voltage transition at 25°C and 80°C. The shape of the frequency shift follows the same trend while the amount of frequency shift increases at a higher temperature due to the increased amount of BTI degradation.

*C. Long Term Stress Measurements*

Fig. 11 represents the high to low voltage transition measurement of 100,000 seconds (=26.78 hours) of stress per voltage stress. Here, the frequency shift reaches to around 4%, immediately after the devices transitioned from 1.4V to 0.8V. This is owing to the significant degradation undergone during the preceding 1.4V stress period.

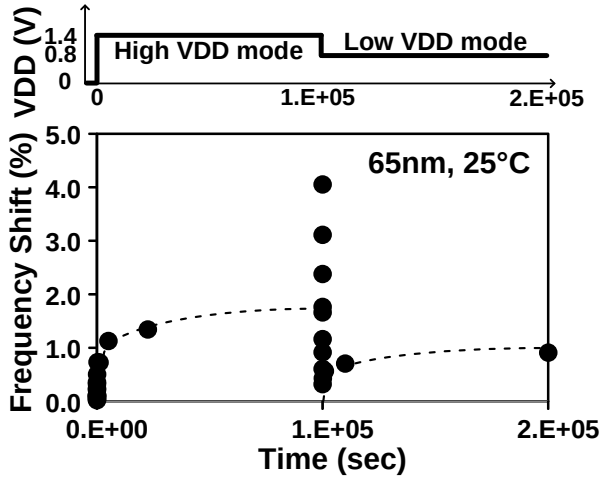



**Fig. 11. Measured frequency shift for long term ($10^5$ seconds or 27.78 hours) high VDD and low VDD periods.**

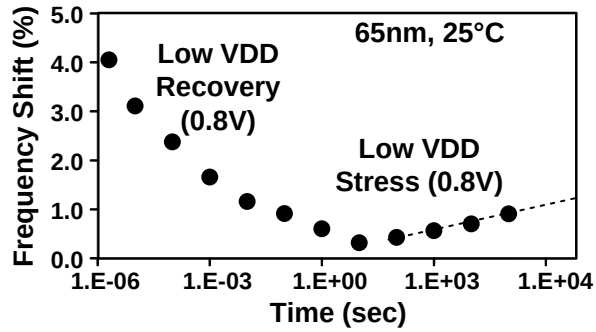



**Fig. 12. Frequency shift in the second half of Fig. 11 plotted in a semi-log scale. Frequency initially recovers but gradually worsens due to long term low VDD stress. Eventually, the frequency shift follows the new equilibrium curve corresponding to BTI degradation at 0.8V.**

Another phenomenon that was observed after the transition to a low VDD was the initial recovery following by BTI-induced long term degradation. Fig. 12 clearly demarcates the transition from a recovery dominated period (< 1 second) to the new BTI equilibrium after around 10 seconds where the degradation at 0.8V starts to dominate over the recovery. [1] discussed a similar concept using a super-position model, where it proposed the overall effect during the recovery phase is the sum of individual recovery component due to the previous stress cycle and the degradation component due to the new voltage stress that the devices is undergoing.

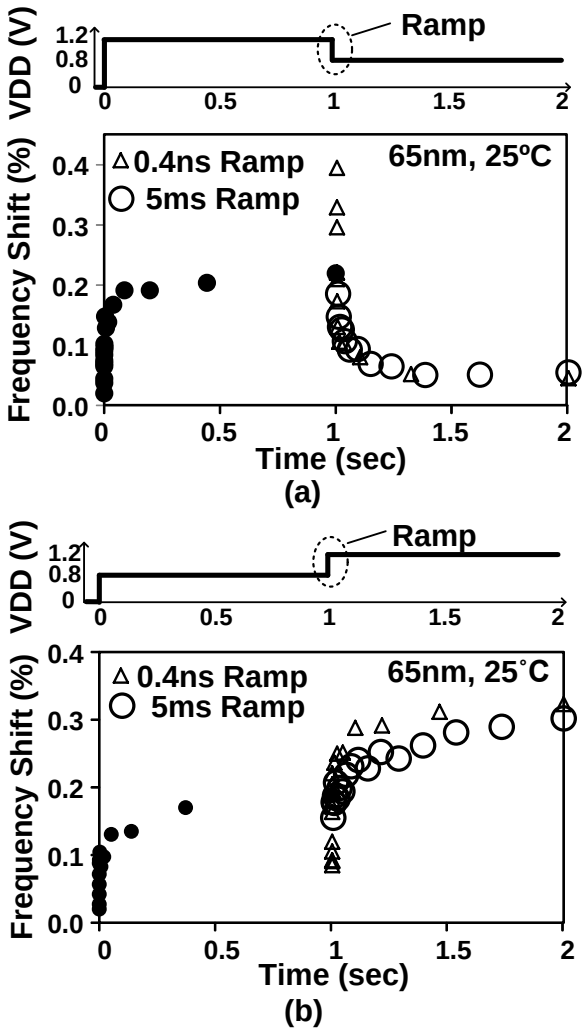



**Fig. 13. Measured frequency shift under two different supply ramp times (i.e. 0.4ns and 5ms) for (a) high to low voltage transition and (b) low to high voltage transition. The magnitude of frequency fluctuation increases with shorter ramp times.**

### *D. Measurement under Different Ramp Times*

In all the previous measurements, the test chip was subjected to an abrupt supply voltage ramp time of 0.4ns immediately followed by the first frequency measurement. To understand the impact of ramp time on the frequency fluctuation, we performed measurements under two different ramp times of 0.4ns and 5ms. Fig. 13 (a) compares the high to low supply transition for the two ramp times. We can see that a longer supply ramp dilutes the frequency shift effect that was seen in a shorter ramp time. This can be explained by the fast recovery that takes place while the supply voltage is ramped down slowly. In the extreme case, the frequency spike disappears completely as shown in Fig. 13 (a) where the frequency shift after the switching is even lower than that observed in the previous high VDD period. Fig. 13 (b) shows a similar effect for a low to high power supply transition, where the frequency shift dip observed for a 5ms ramp time was lower than that observed for a 0.4ns ramp time. These results confirm that frequency fluctuation is a concern in systems with ramp rates that are comparable to the degradation and recovery time constants (e.g. microseconds) of BTI.

## IV. CONCLUSIONS

In this work, we have demonstrated a new odometer circuit capable of continuously measuring instantaneous frequency fluctuation effects under fast DVFS transients. The proposed design contains multiple reference ring oscillators which are paired sequentially with a common stressed ring oscillator to measure the frequency degradation. This new configuration ensures that the reference circuits are kept fresh when exposed to a high stress voltage for consecutive measurement periods, allowing BTI degradation and recovery effects to be accurately measured with sampling intervals as short as a microsecond. Measurement results from a 65nm test chip indicates that an additional frequency guardband of up to 4% may be necessary to account for the instantaneous frequency shift effect in DVFS systems with sub-microsecond voltage transition times.

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