Assessing the Impact of RTN on Logic Timing Margin Using a 32nm Dual Ring Oscillator Array

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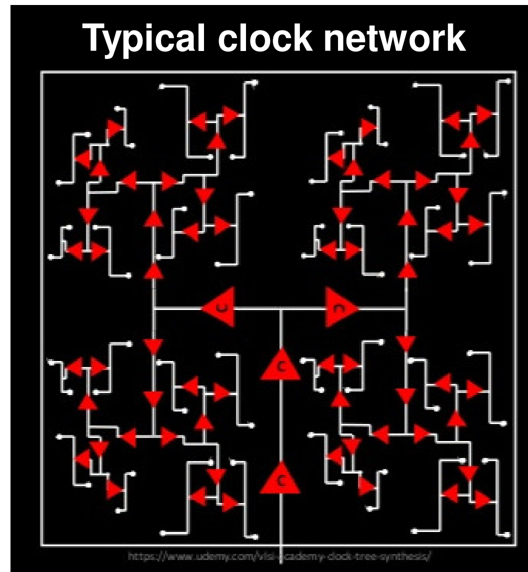
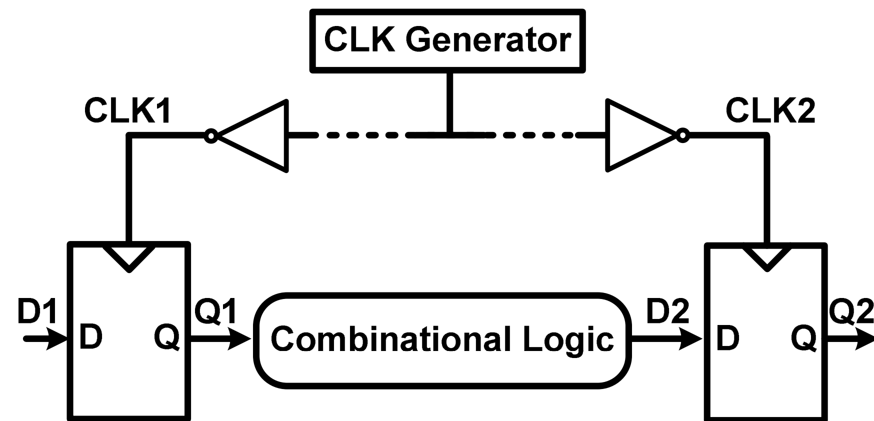
Outline of Presentation

- RTN (Random Telegraph Noise) Impact on Logic Timing
- Proposed Dual Ring Oscillator Array RTN Monitor
- 32nm Test Chip Results
- Timing Margin Analysis
- Conclusions

Introduction to Logic Timing

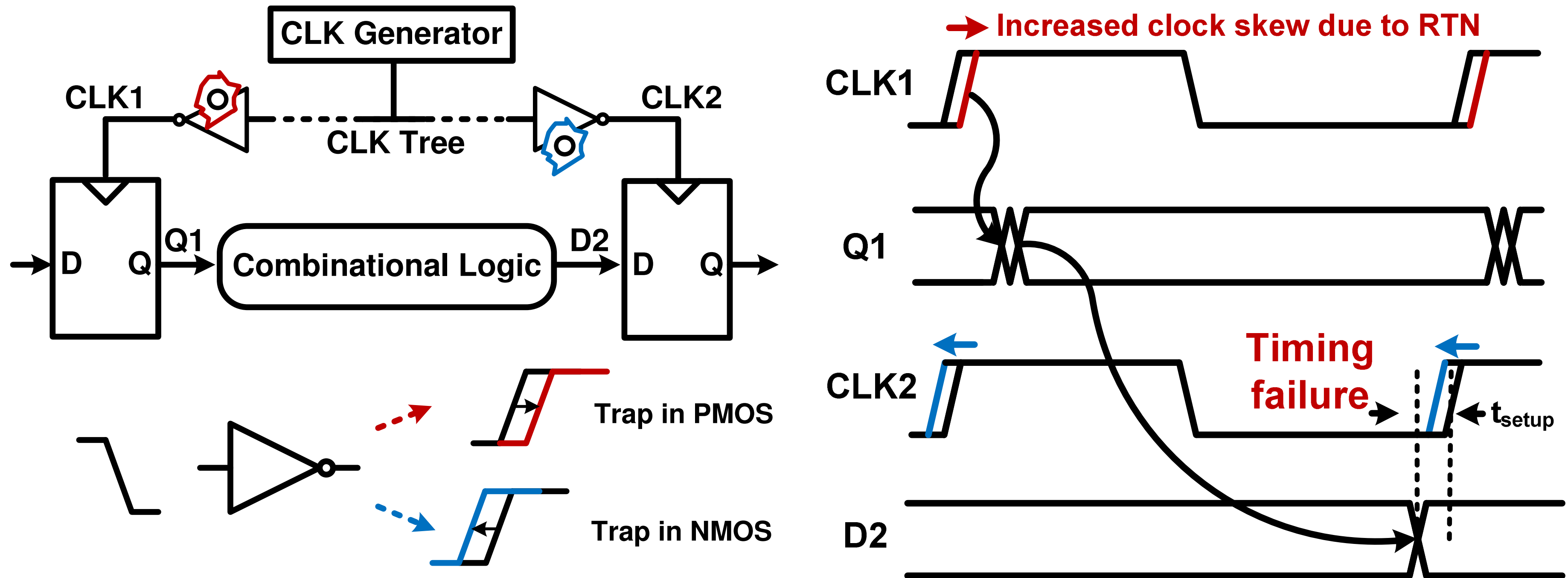


Source: VLSI Academy



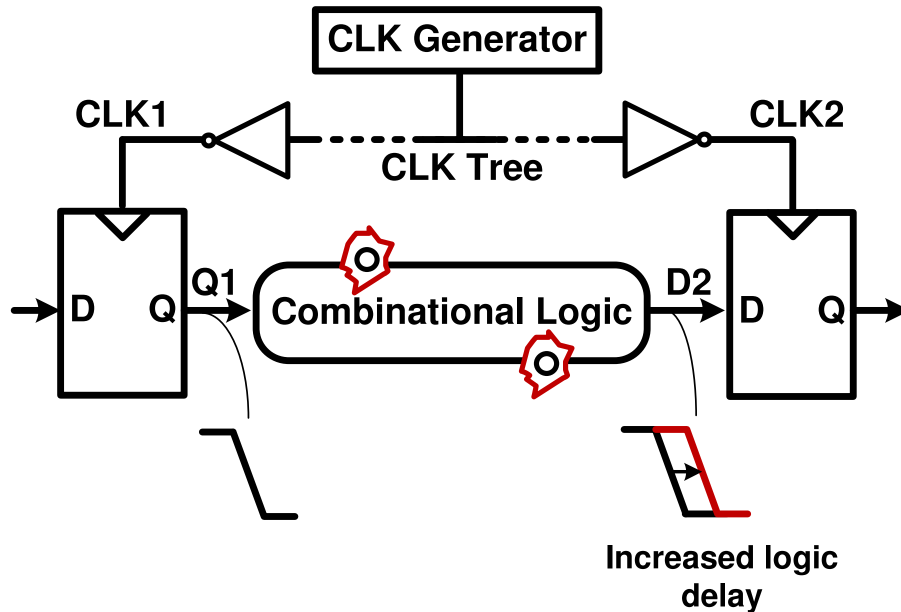
- **3 main blocks: Clock tree, combination logic, flip-flop**
- **Correct function: clock period ≥ $t_{flip\text{-}flop}+t_{logic}+t_{clk_skew}$**
  - **$t_{flip\text{-}flop}$: clock-to-Q delay + setup time**
  - **t_{clk_skew}: clock arrival time difference between two flip-flops**
  - **t_{logic}: logic delay**

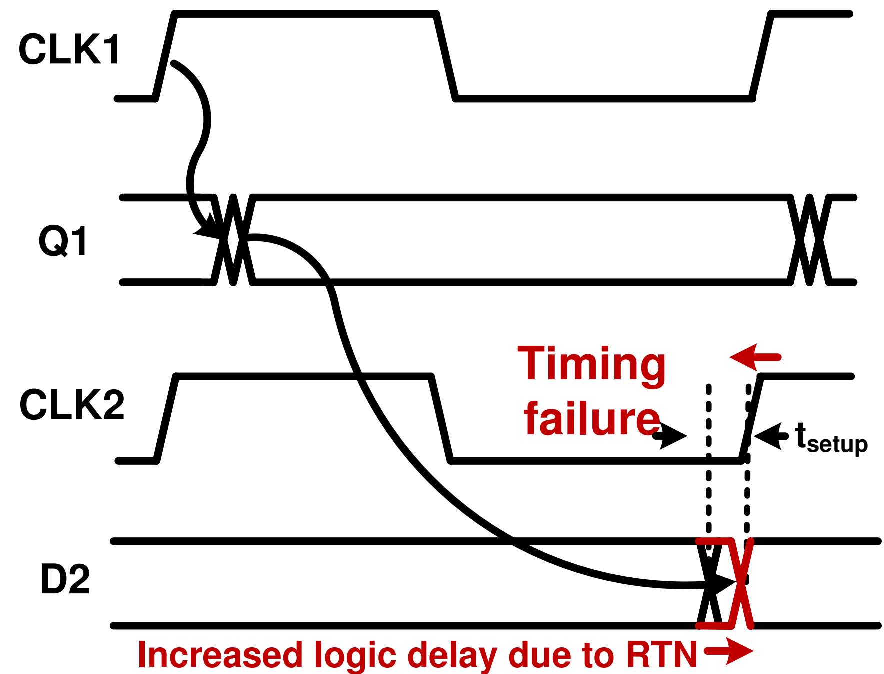
RTN Impact #1: Clock Skew



- **RTN in clock drivers induces random clock skew shifts between two divergent paths**
- **A negative clock skew (i.e. CLK2 arriving earlier than CLK1) could lead to a setup time violation**

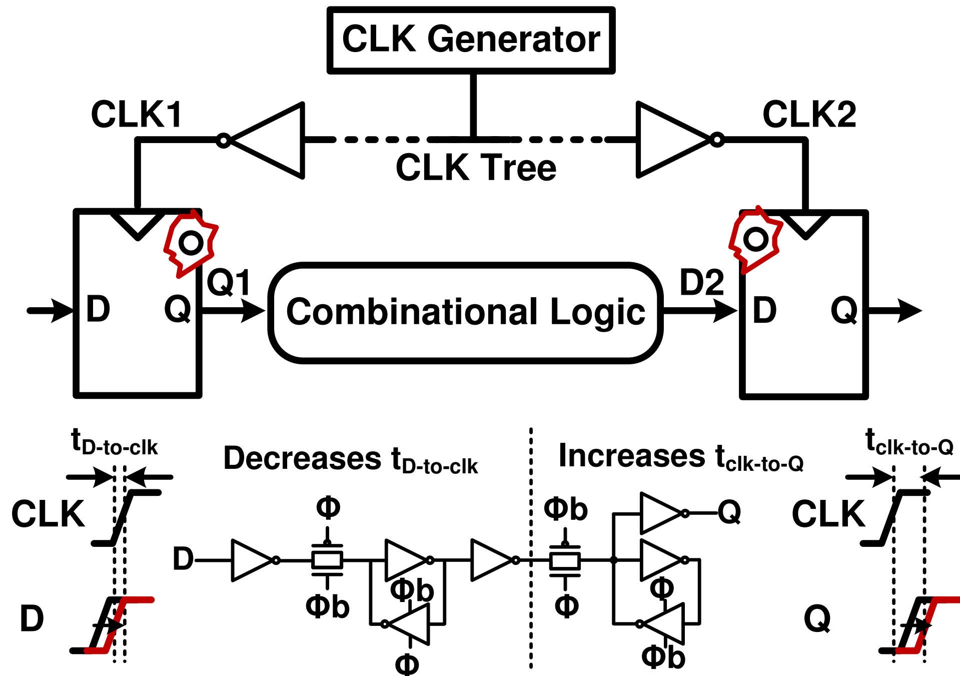
RTN Impact #2: Logic Delay

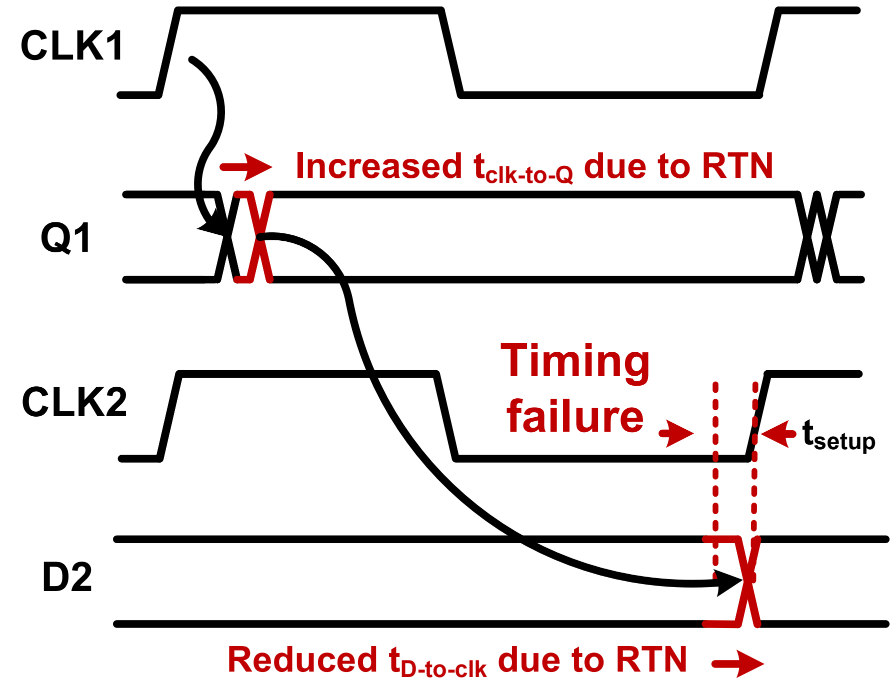




- RTN in combinational logic increases logic delay
- Setup time violation can occur

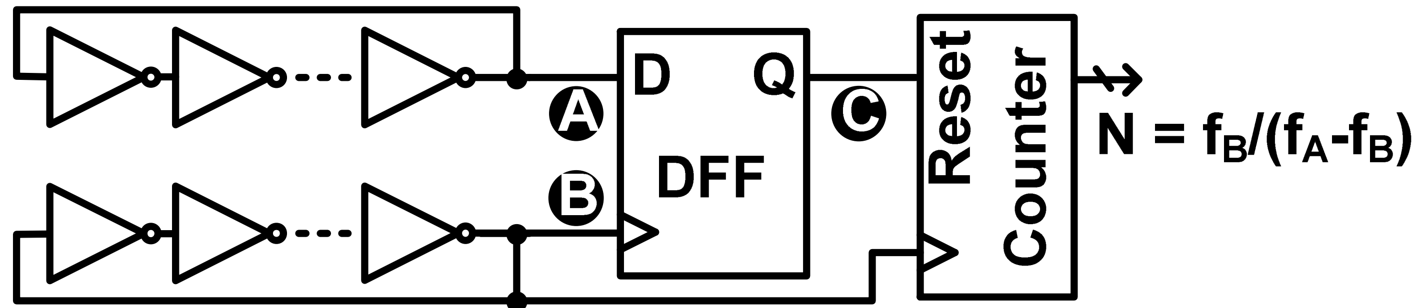
RTN Impact #3: Flip-Flop Timing

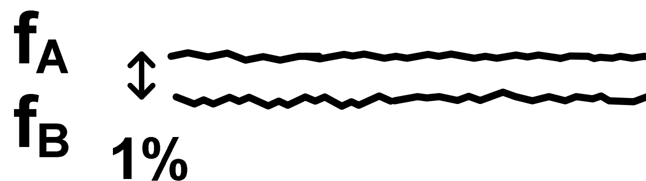


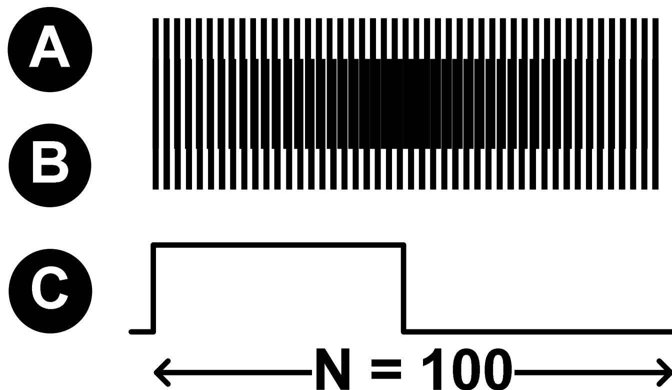


- Increased $t_{clk\text{-to-Q}}$ of first DFF and decreased $t_{D\text{-to-clk}}$ of second DFF could lead to a setup time violation

Prior Work: Beat Frequency based RTN Monitor







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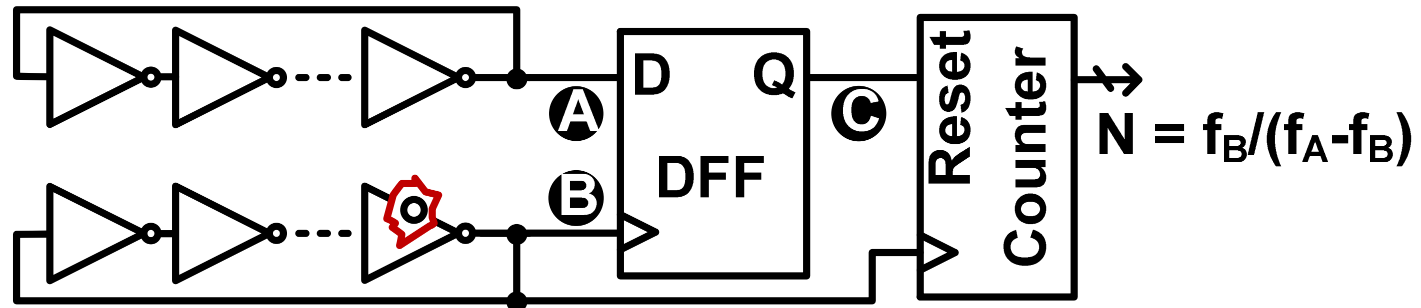

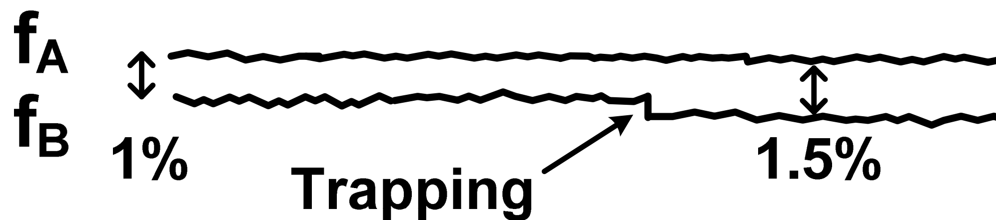

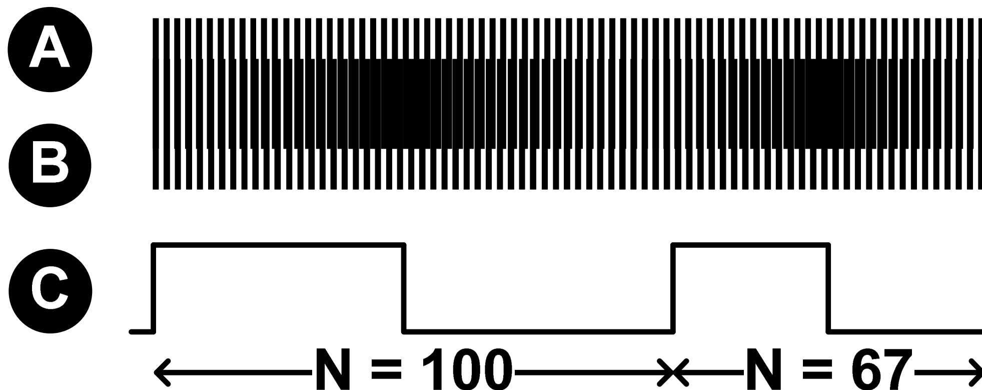

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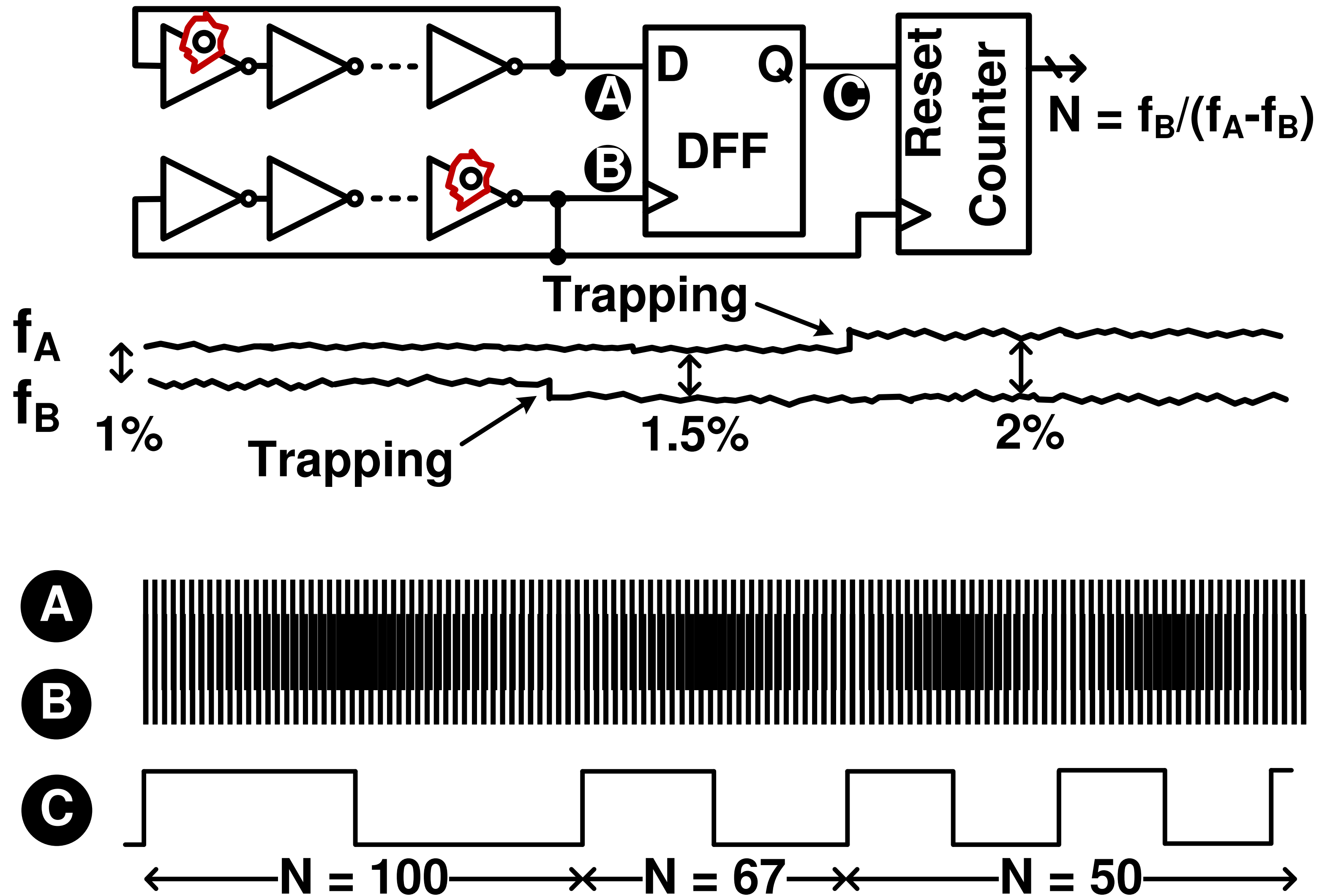

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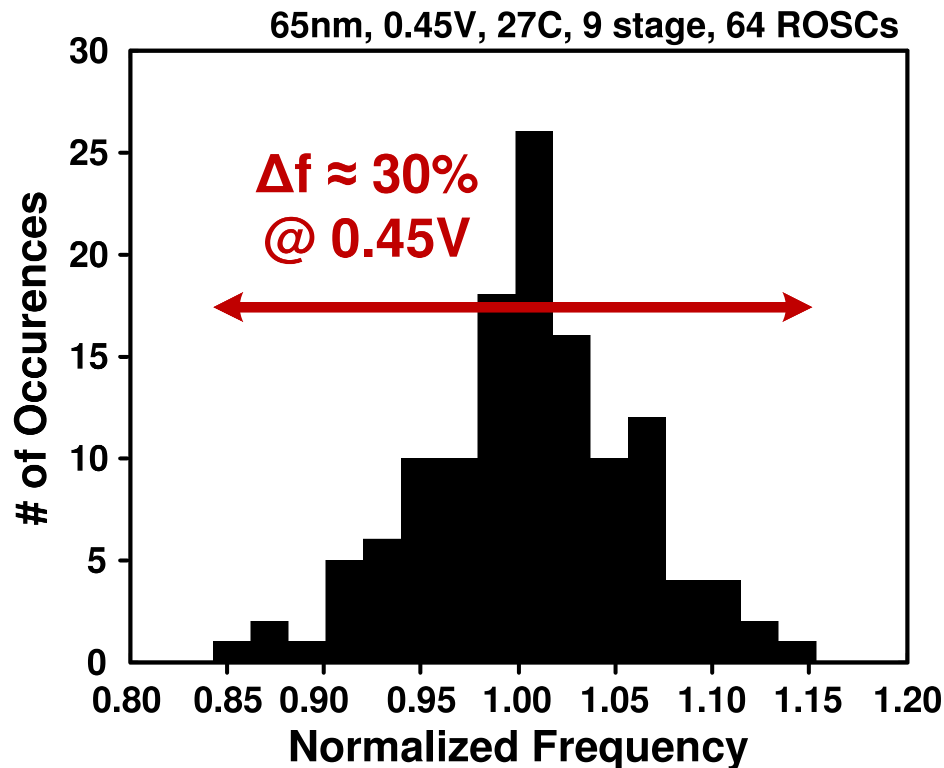
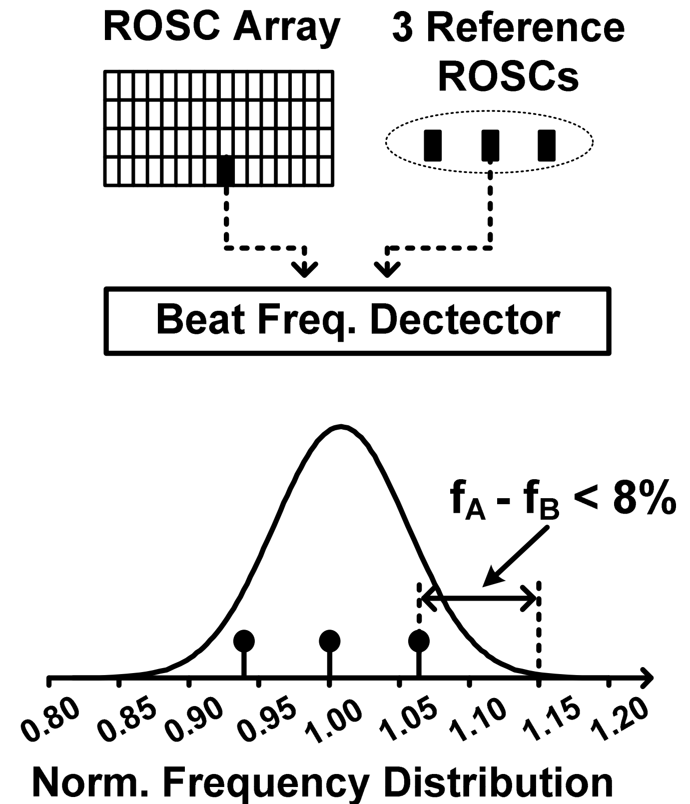
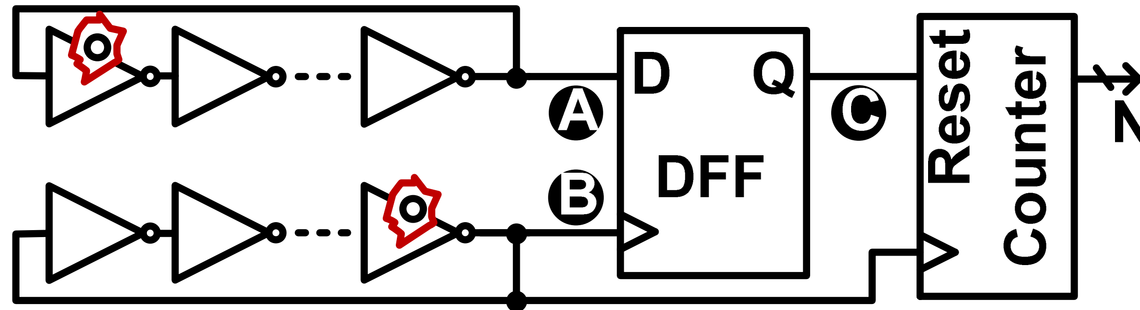
Limitations of Prior Work

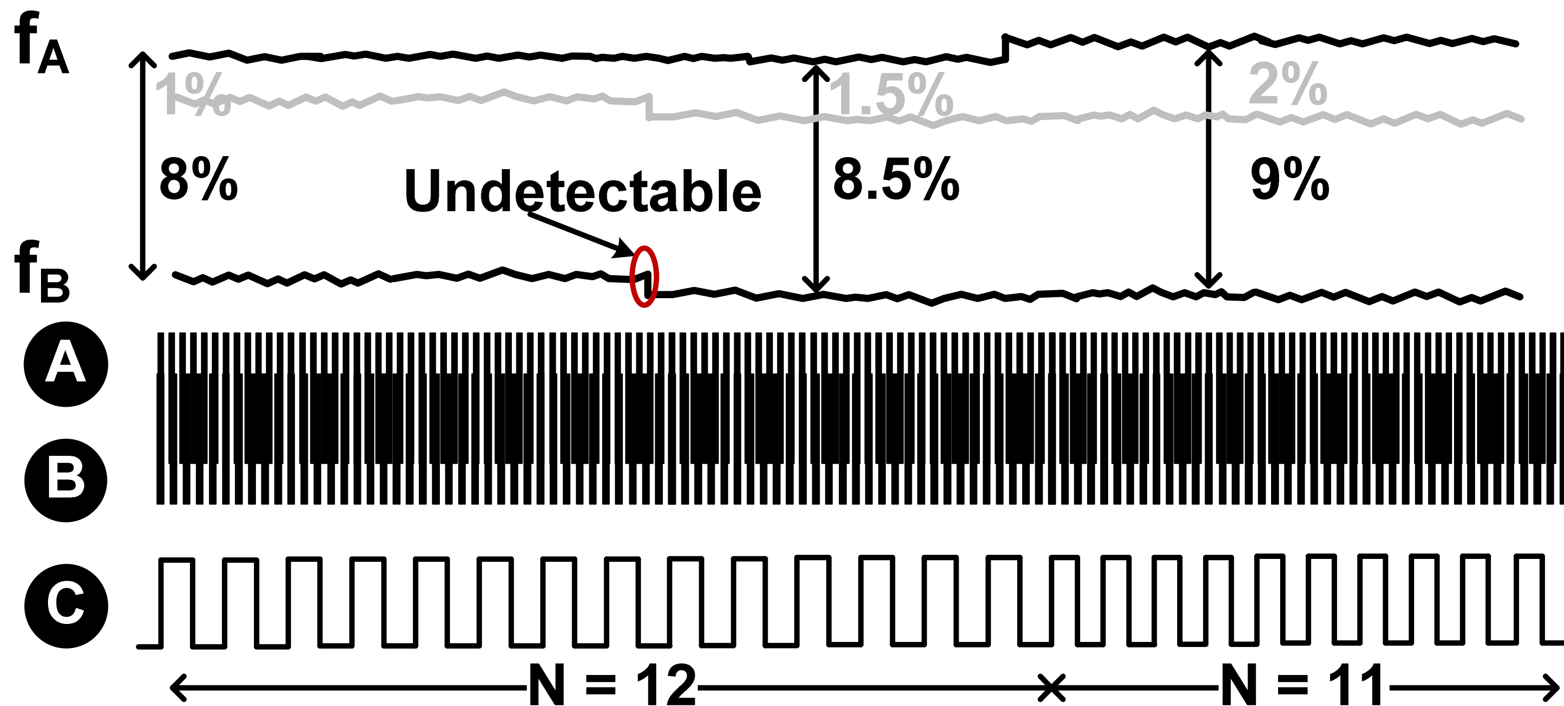




- ROSC shows a wide frequency distribution at low Vdd's
- Not every ROSC under test can achieve a high measurement resolution (Δf should be less than 1% for a frequency measurement resolution less than 0.01%)

Limitations of Prior Work





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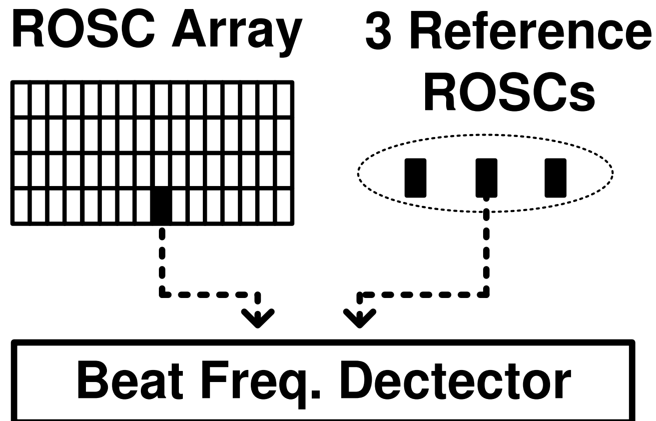
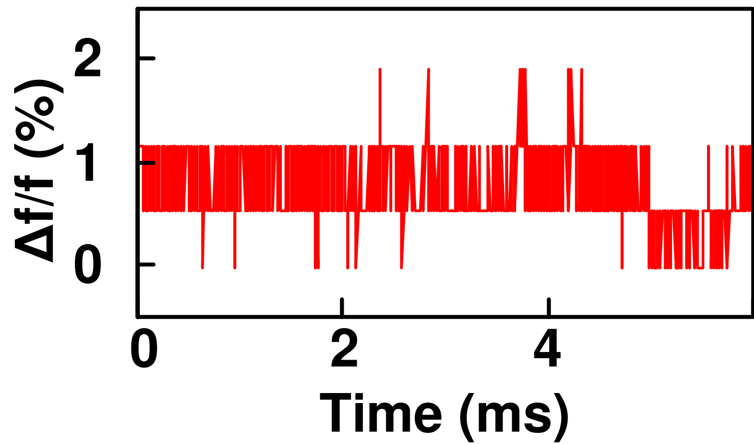
Prior Work vs. Proposed Design

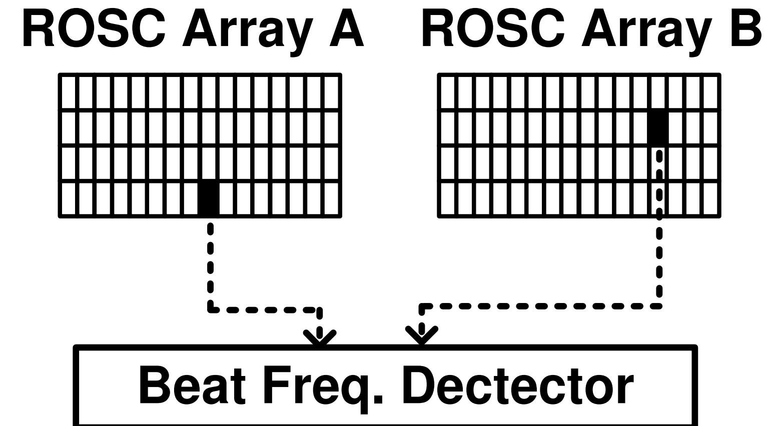
Prior Work



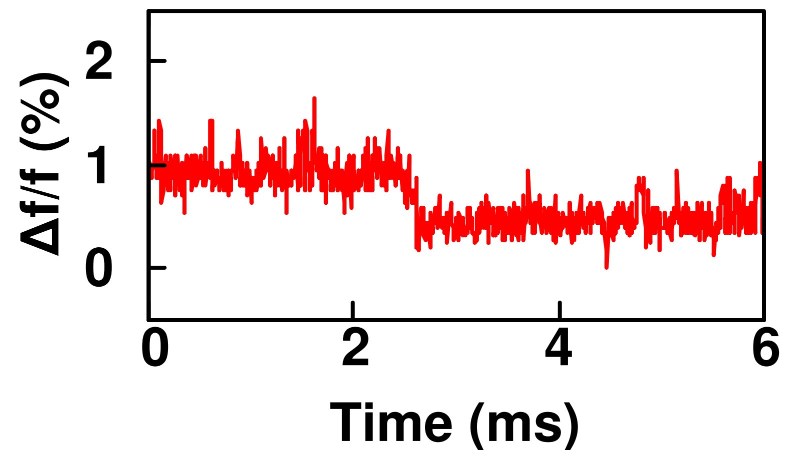
Low resolution at low Vdd



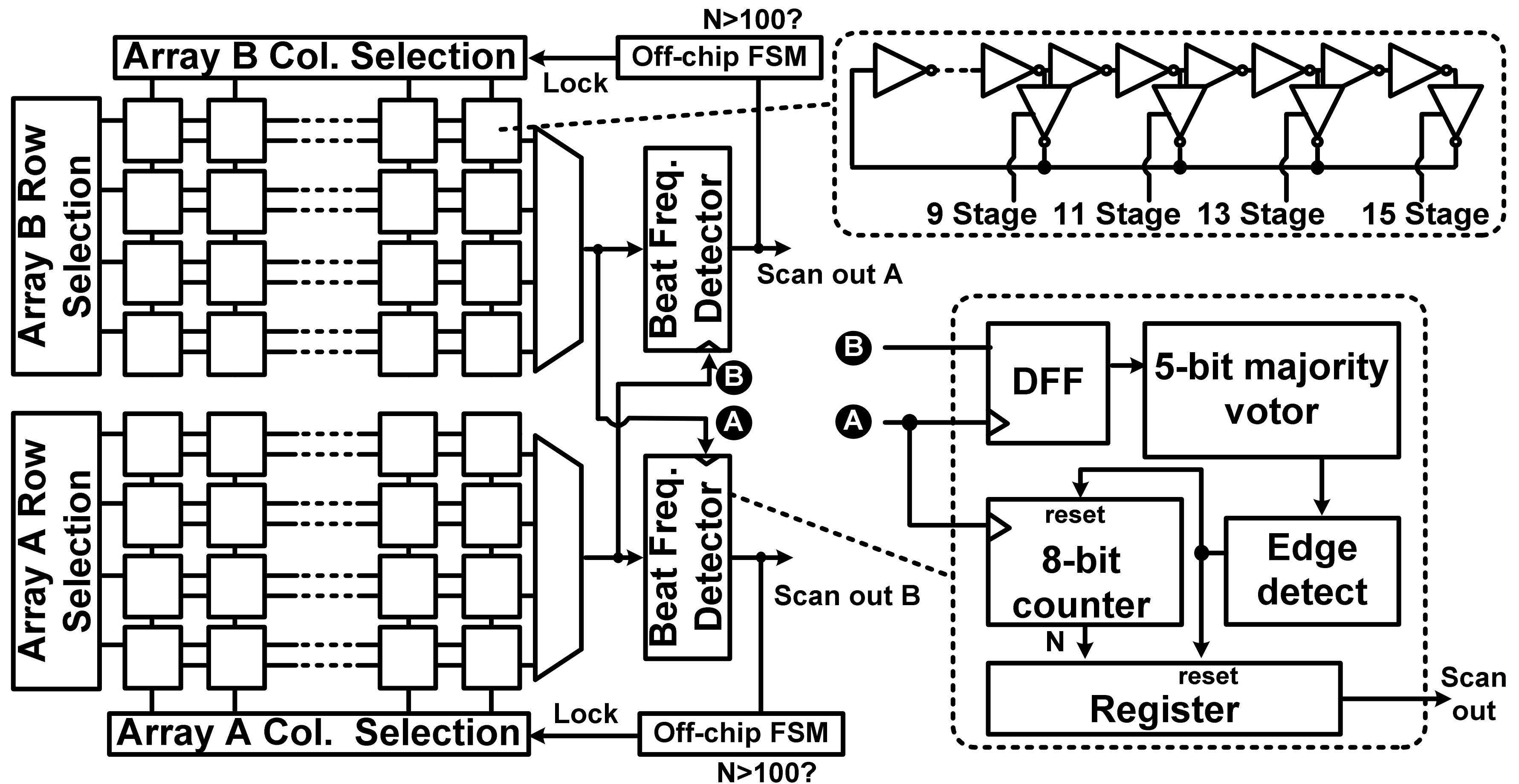
This Work



High resolution at low Vdd



Proposed Dual ROSC Array RTN Monitor



- **Pair each ROSC with a ROSC from a second array with similar frequency (i.e. Δf < 1%)**

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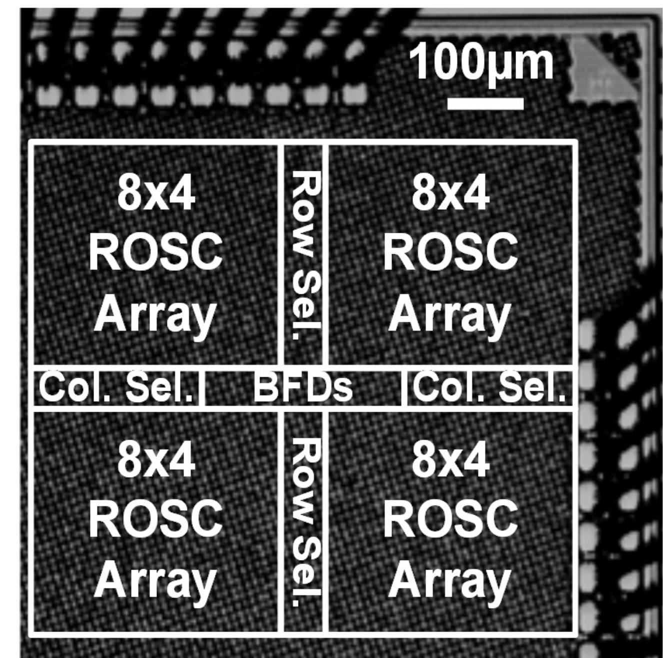
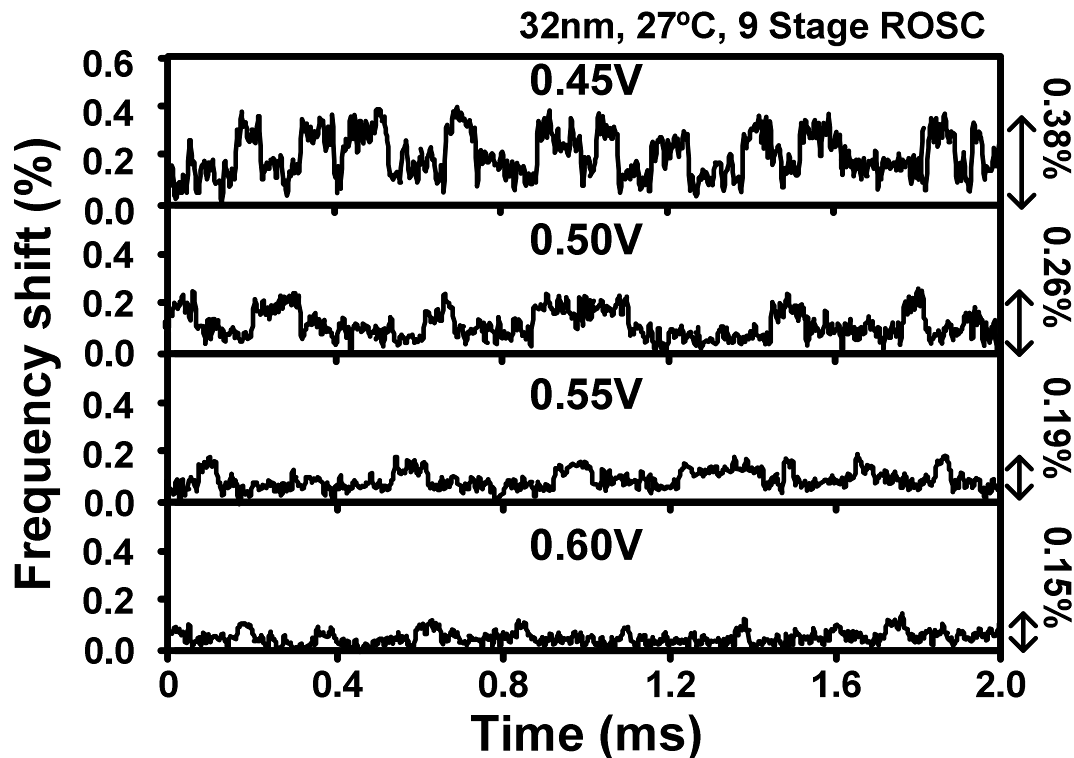
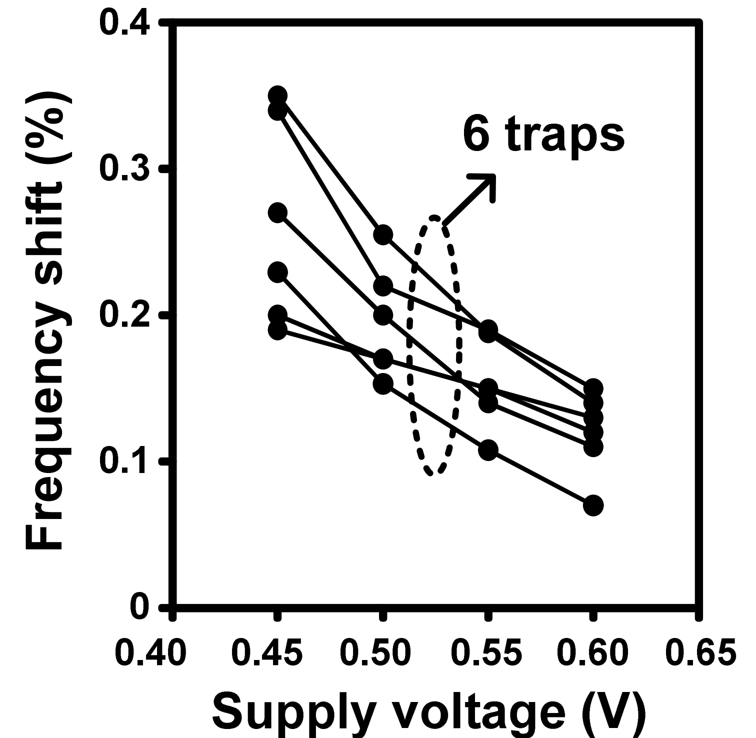


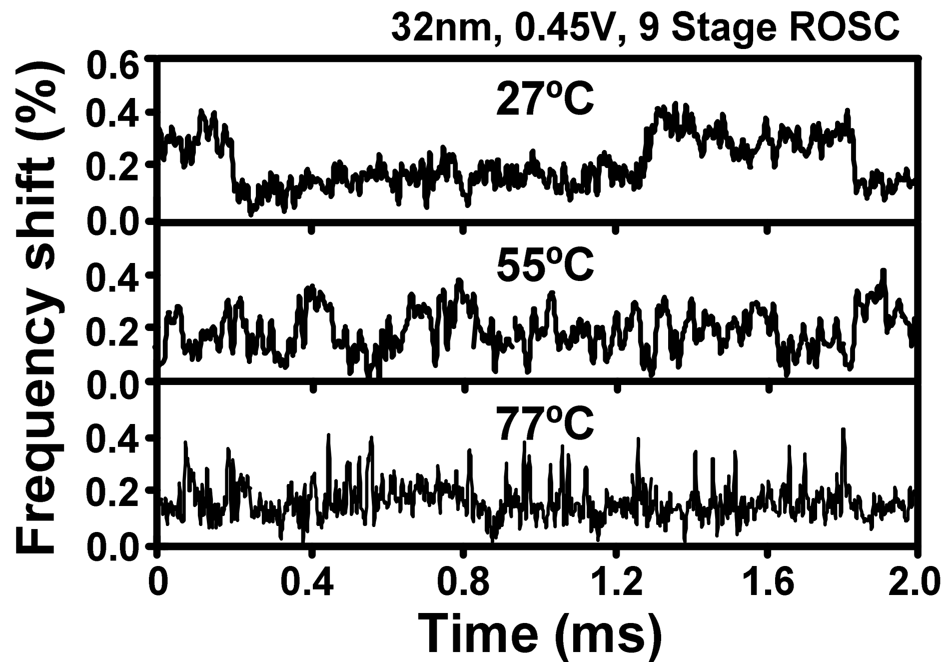
Frequency Shift vs. Supply Voltage

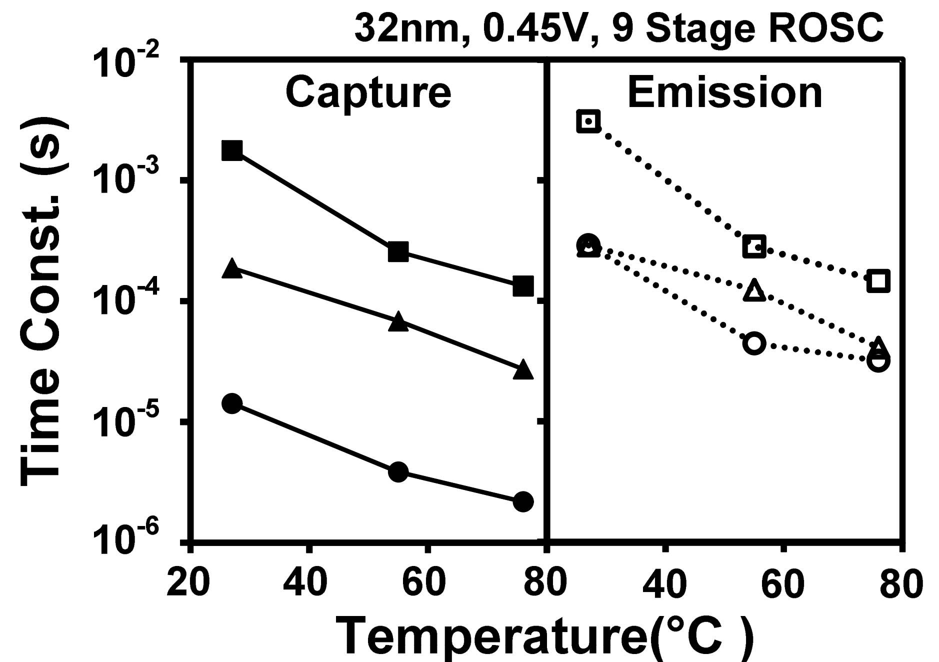




- **Frequency shift magnitude decreases at higher voltages due to lower sensitivity**

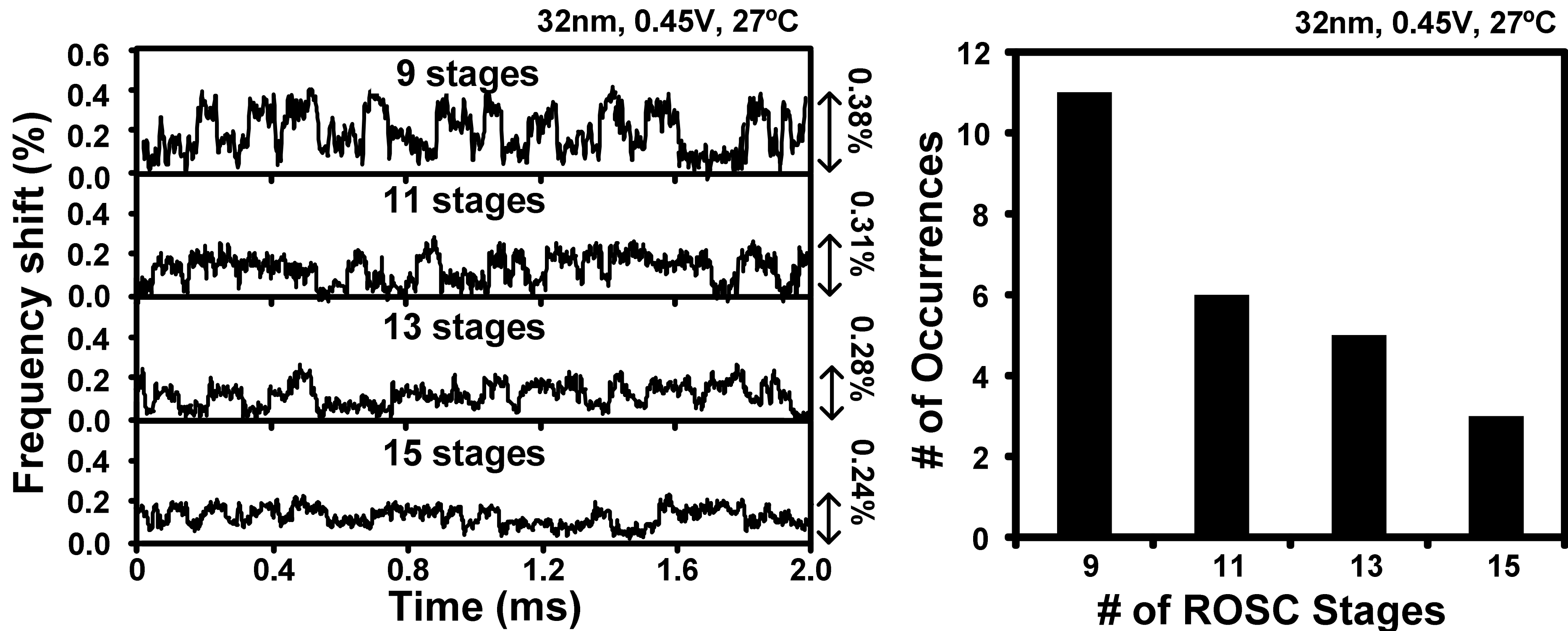
Frequency Shift vs. Temperature





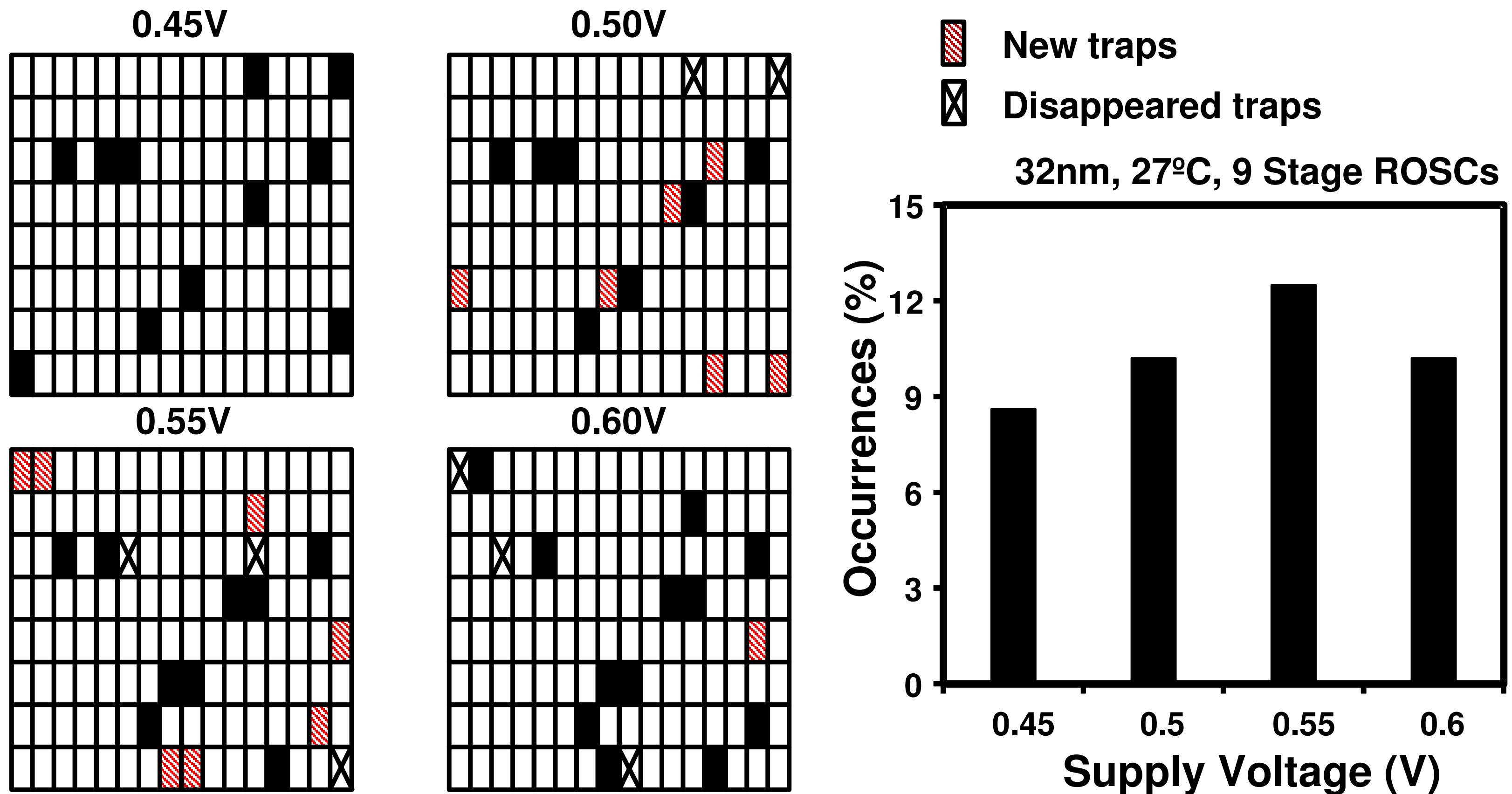
- **RTN trapping and de-trapping time constants become shorter at higher temperatures**

Frequency Shift vs. ROSC Stages



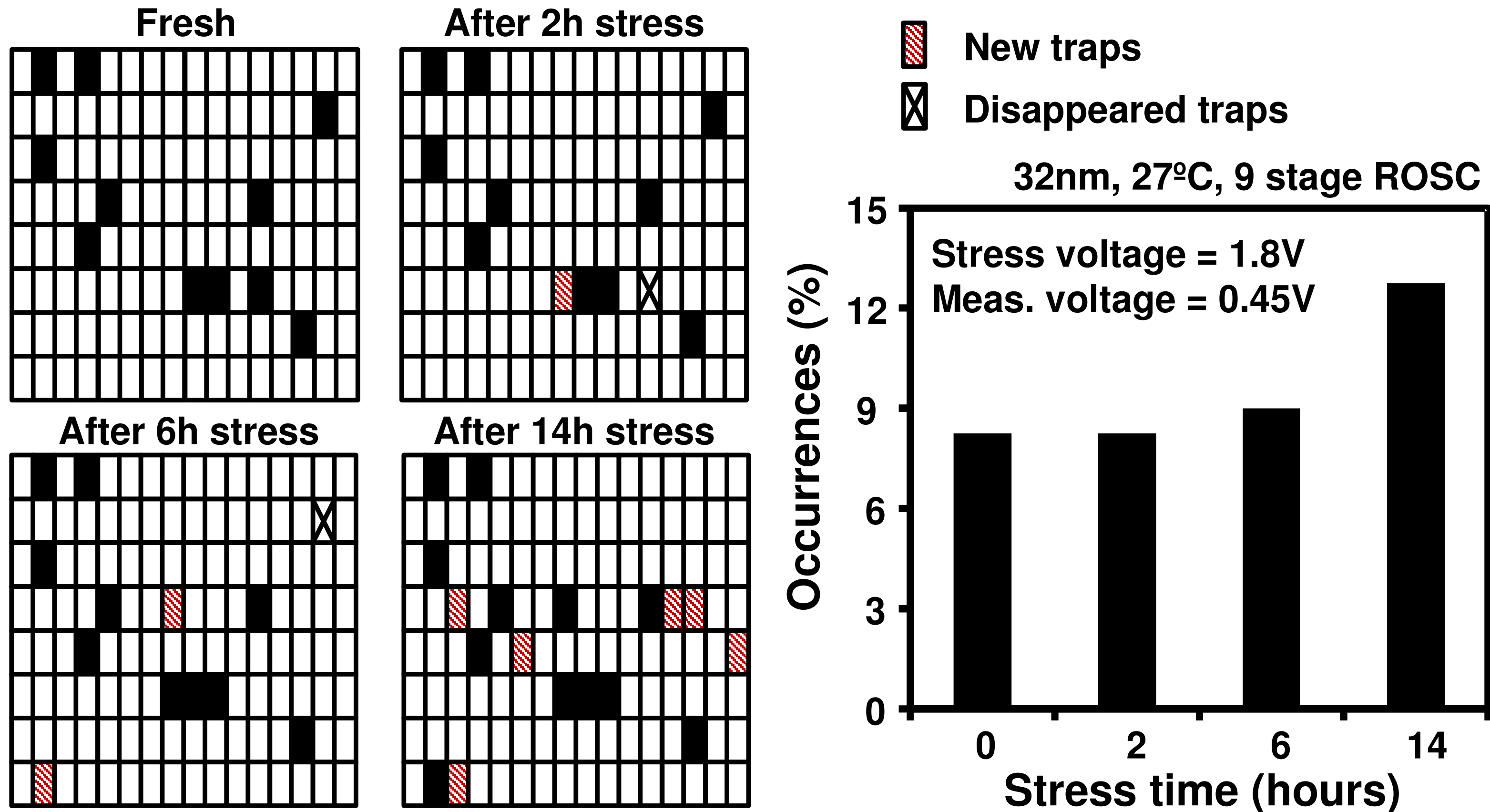
- Frequency shift magnitude decreases for longer ROSCs
- Fewer measurable RTN traps in longer ROSCs
  - More traps present but harder to detect due to averaging effect

RTN Map vs. Supply Voltage



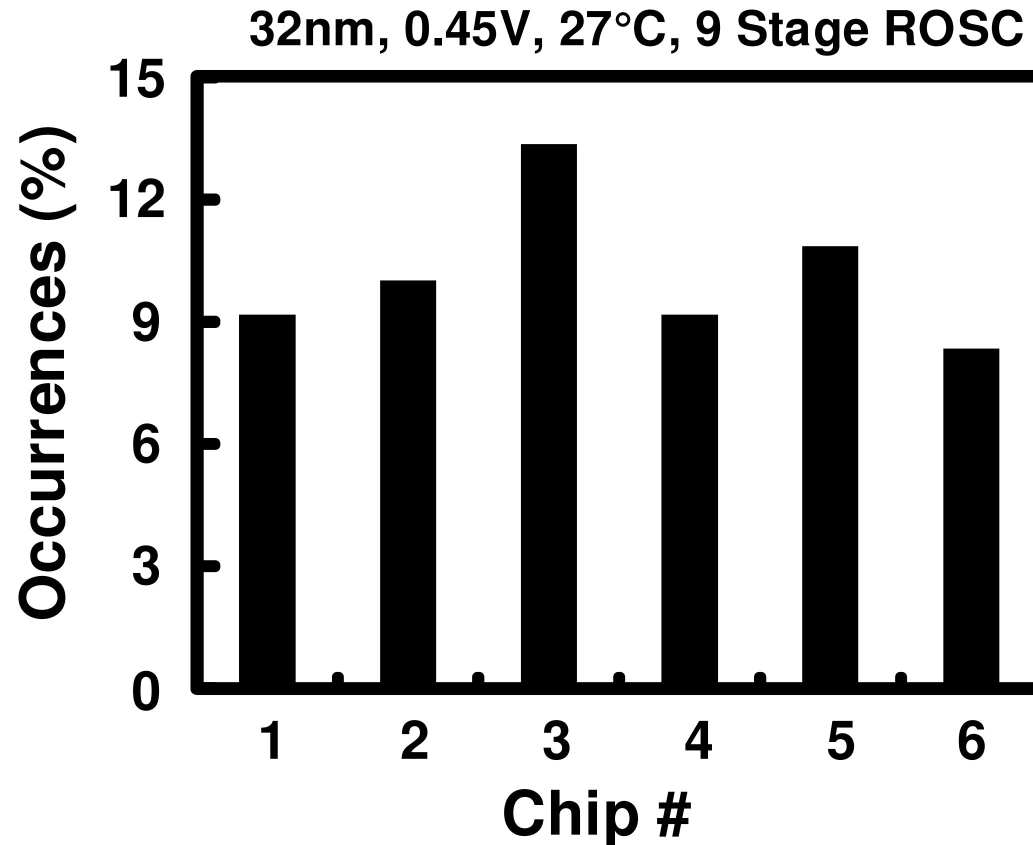
- RTN traps may appear or disappear when Vdd is changed
  - Fermi level shifts with supply voltage

RTN Map vs. Stress Time



- Higher number of RTN traps after applying BTI stress
  - Some traps disappear (possibly linked to BTI recovery)
  - New traps appear due to BTI stress

Chip to Chip Variation



- 8.6% to 13.3% of the ROSCs show signs of RTN

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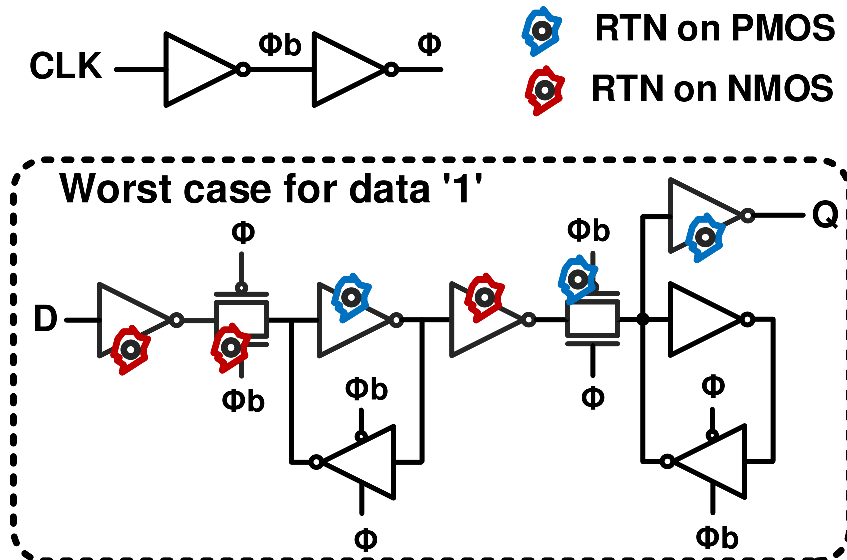
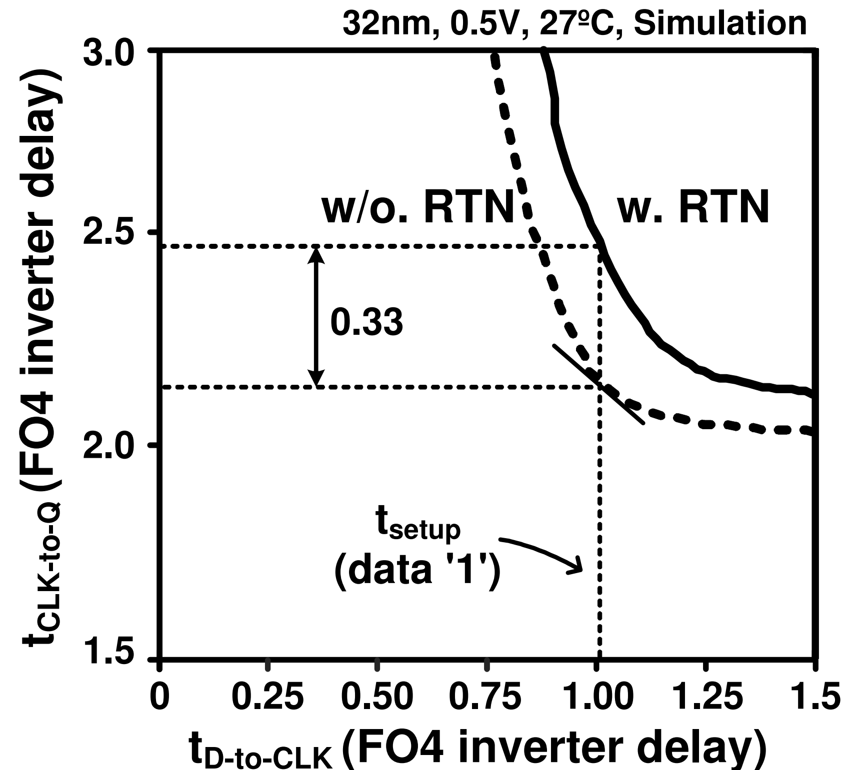
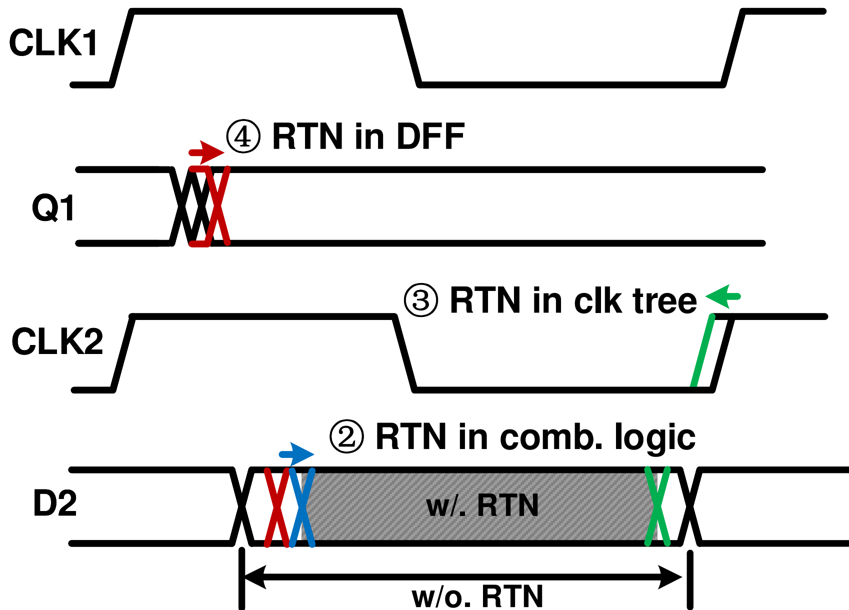
Flip-flop Timing Analysis

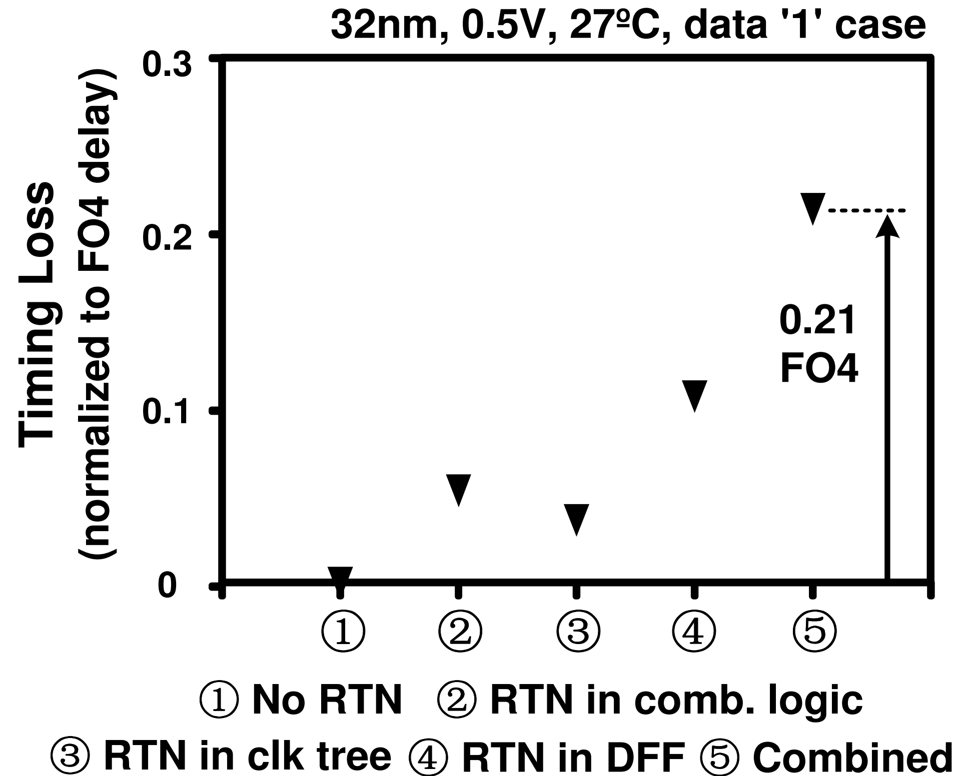




- **Flip-flop clk to Q delay increases by 0.33 FO4 inverter delay given the same setup time (assuming traps in locations specified above)**

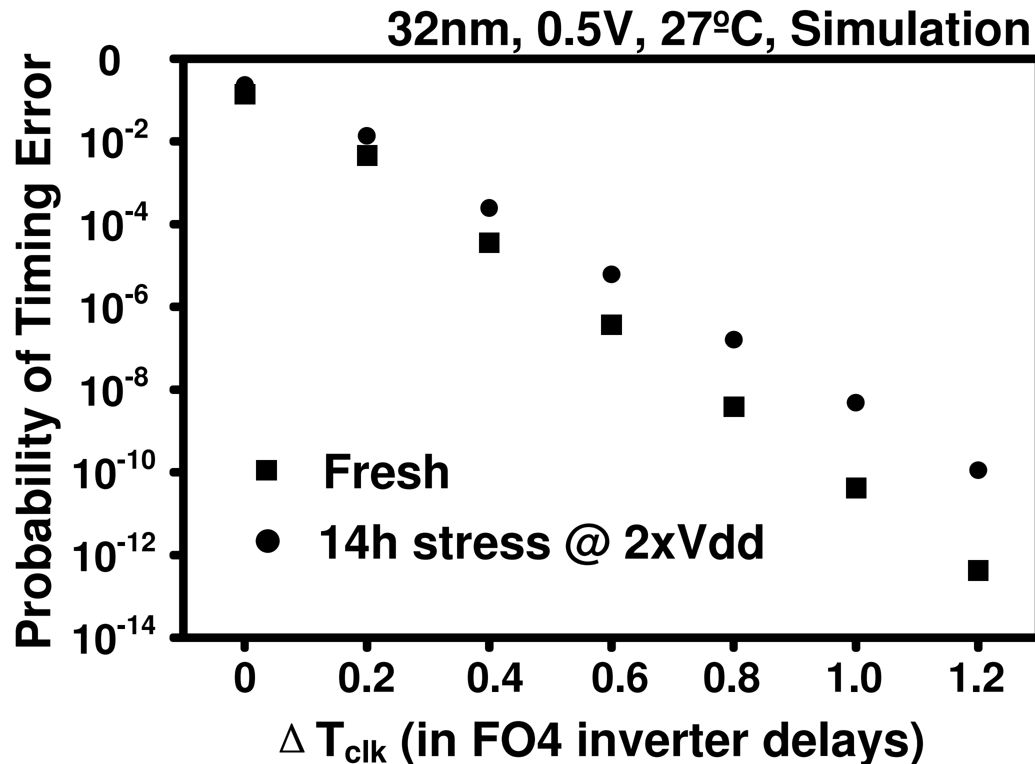
Overall Timing Loss Analysis





- Clock period must be increased by 0.21 FO4 inverter delays for correct operation (assuming one RTN trap in each block, i.e. logic, clock tree, and DFF)

Increasing Clock Period to Prevent RTN Induced Timing Errors



$$\Pr(\text{Timing error} \mid \Delta T_{\text{clk}} = x)$$

$$= 1 - \sum_{i,j,k} \Pr(N_{\text{clk}} = i) \cdot \Pr(N_{\text{data}} = j) \cdot \Pr(N_{\text{DFF}} = k)$$

$$\forall\, i, j, k,\ \ \Delta t_{\text{skew}}(N_{\text{clk}} = i) + \Delta t_{\text{data}}(N_{\text{data}} = j) + \Delta t_{\text{DFF}}(N_{\text{DFF}} = k) \le x$$

N_{clk}, N_{data} and N_{DFF} are the number of traps in clock tree, combinational logic and DFF, respectively.

- **Probability of a trap being present and its impact on delay used to estimate timing guard band required for correct operation**

Conclusions

- **New dual ROSC array can measure RTN induced frequency shift with resolution <0.01% at 0.45V**
- **Various aspects of RTN measured from a 32nm test chip**
- **Assessed RTN impact on logic path timing and estimated probability of timing error**

Acknowledgement

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