An 8bit, 2.6ps Two-Step TDC in 65nm CMOS Employing a Switched Ring-Oscillator Based Time Amplifier

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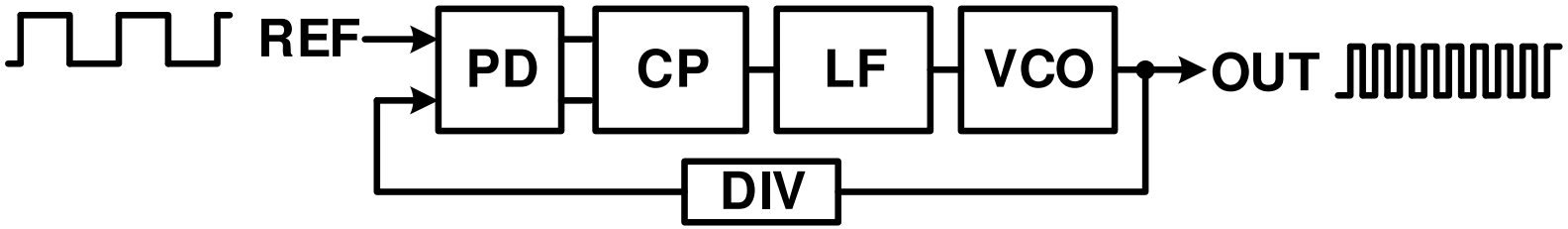
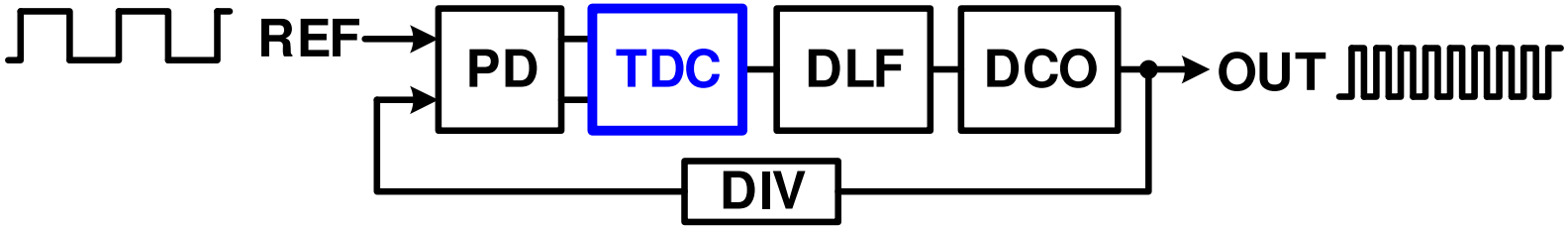
Agenda

- Conventional Time-to-Digital Converters
- Proposed Switched Ring Oscillator Based Time Amplifier Circuit
- TDC Test Chip Configuration
- Measurement Results
- Conclusion

Analog/Digital Phase Locked Loops



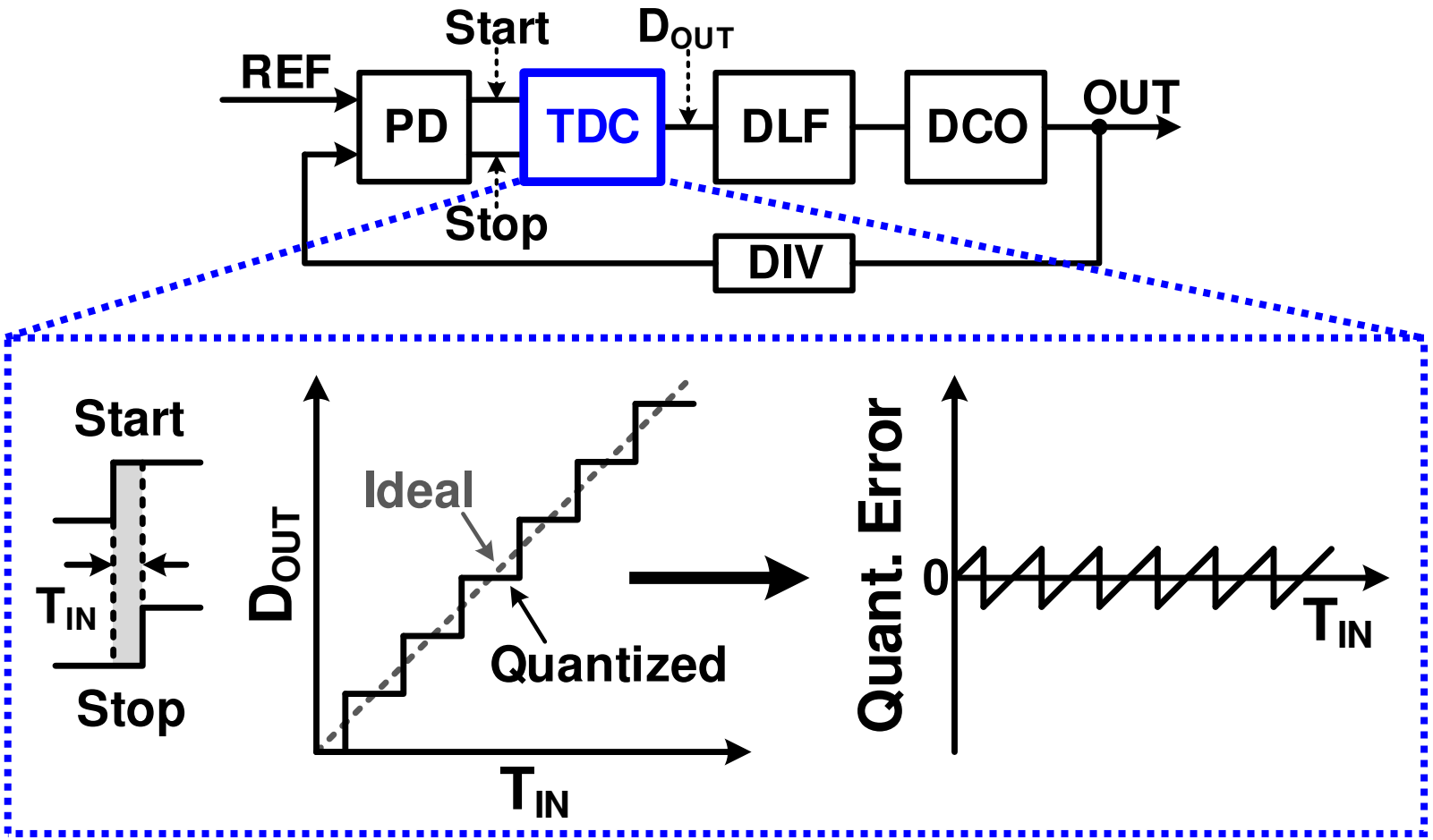
Analog PLL



Digital PLL

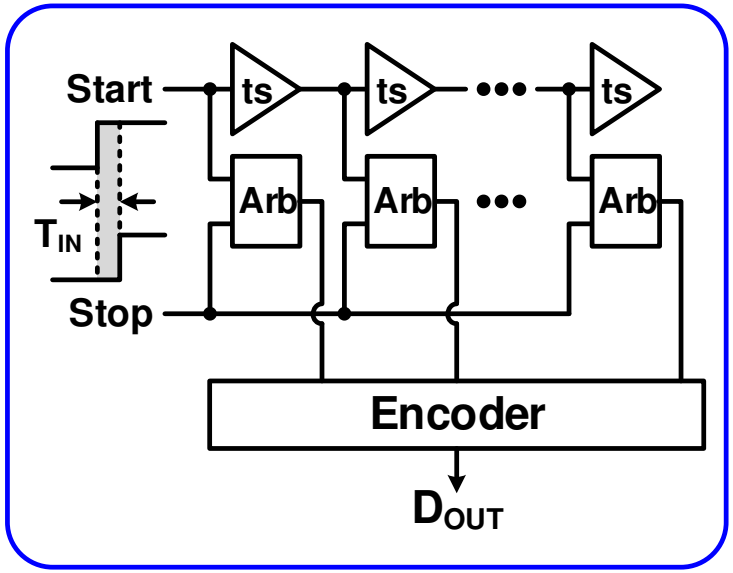
- Compact area, scalable, insensitive to supply noise, etc.
- Phase noise degradation due to quantization error

TDC Quantization Noise

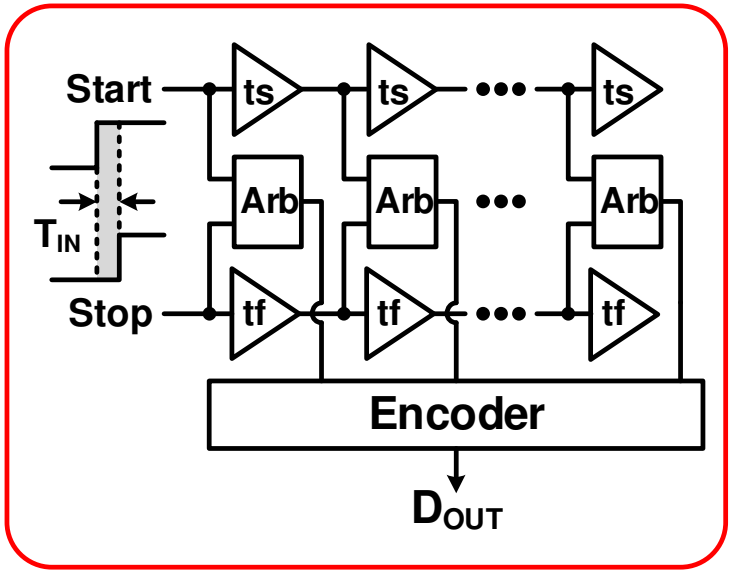


- Critical building blocks of DPLL: TDC and DCO
- TDC quantization error degrades PLL in-band phase noise

Conventional TDCs and Trade-offs



Delay Line (DL)



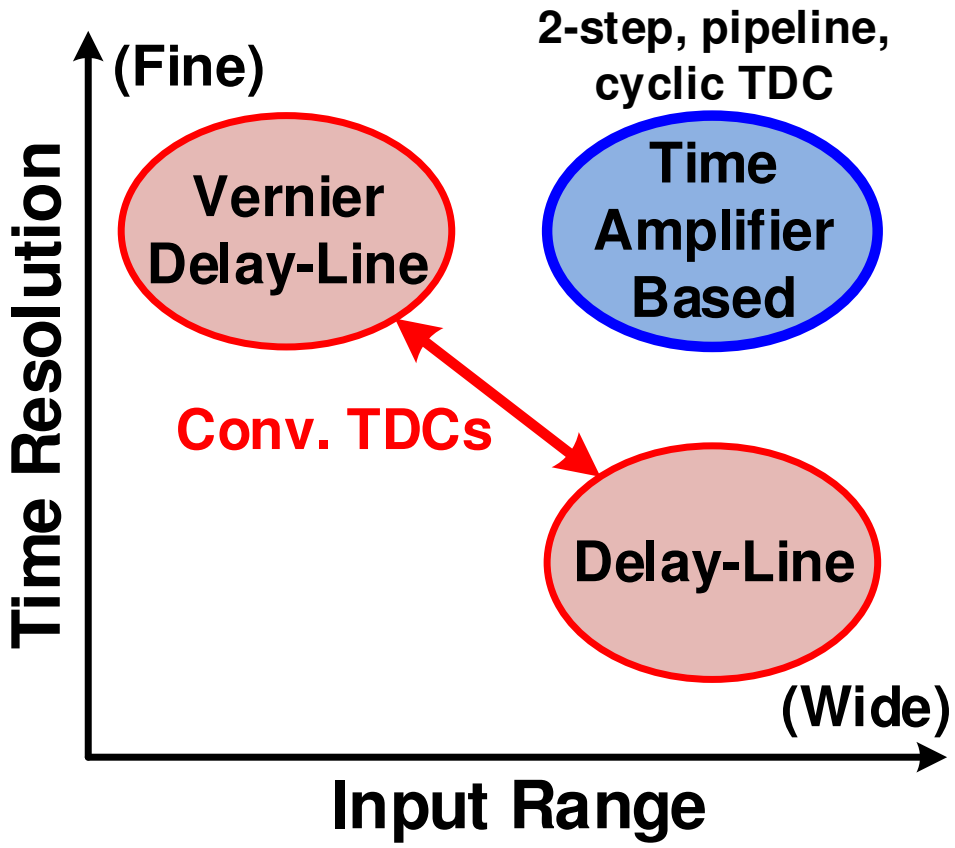
Vernier Delay Line (VDL)

	DL TDC		VDL TDC	
Resolution	ts	40ps	ts−tf	2ps
Input Range	$2^N \cdot ts$	10.24ns	$2^N \cdot (ts-tf)$	0.512ns
Conv. Time	$2^N \cdot ts$	10.24ns	$2^N \cdot ts$	10.24ns

*e.g. 8bit TDC with two delay cells (i.e. ts=40ps and tf=38ps)

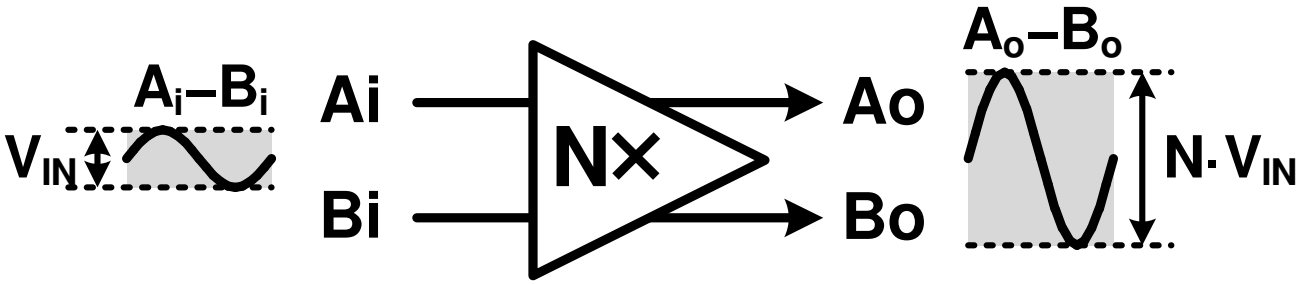
- Trade-off between time resolution and input range

TDC Resolution vs. Input Range

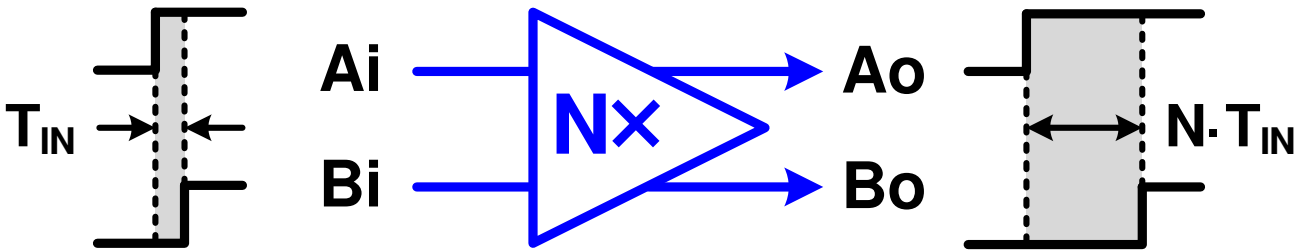


- To achieve both fine time resolution and wide input range
- Time amplifier (TA) based TDCs: two-step, pipeline, etc.

Voltage vs. Time Amplifier



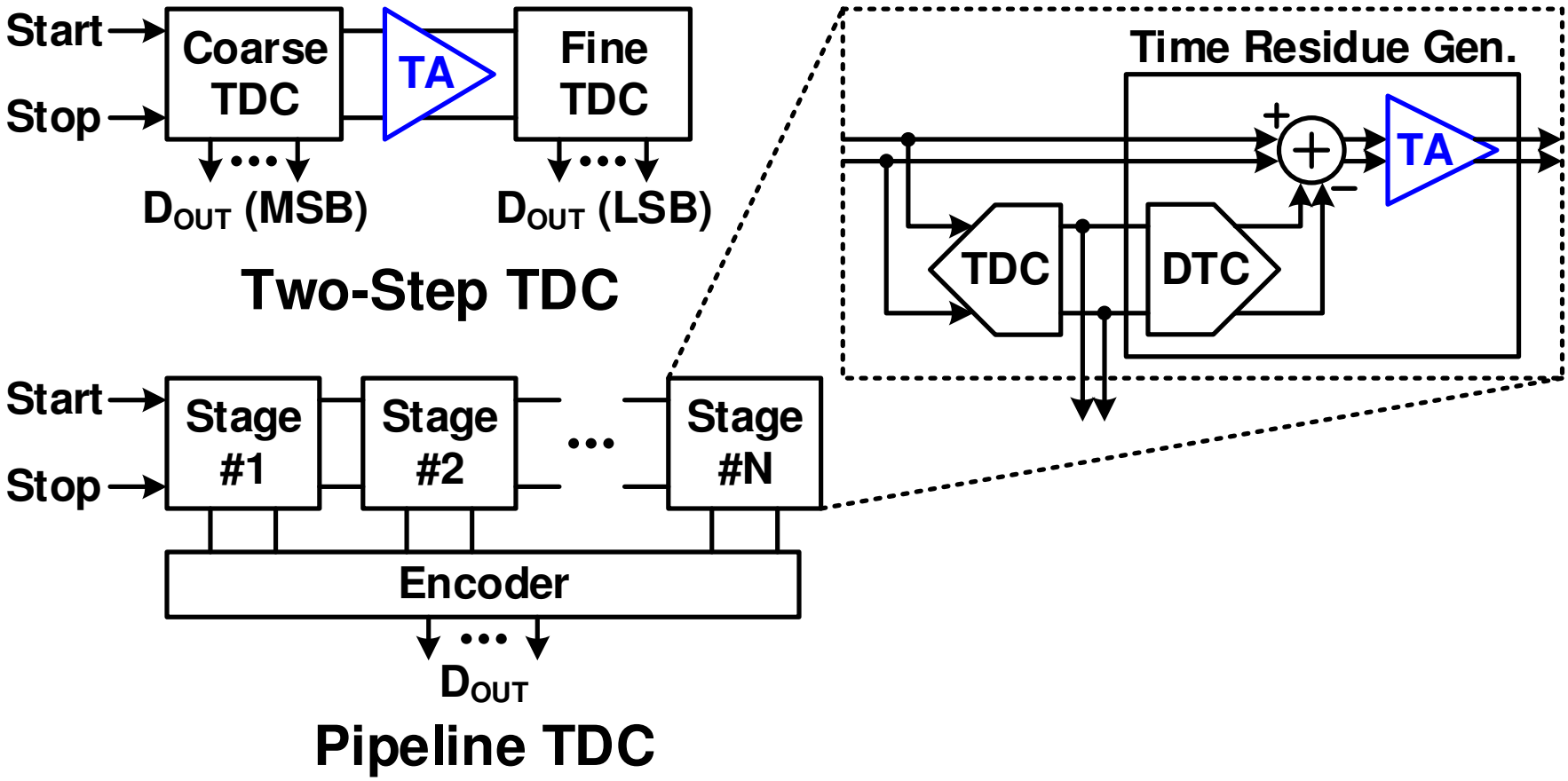
Voltage Amplifier



Time Amplifier (TA)

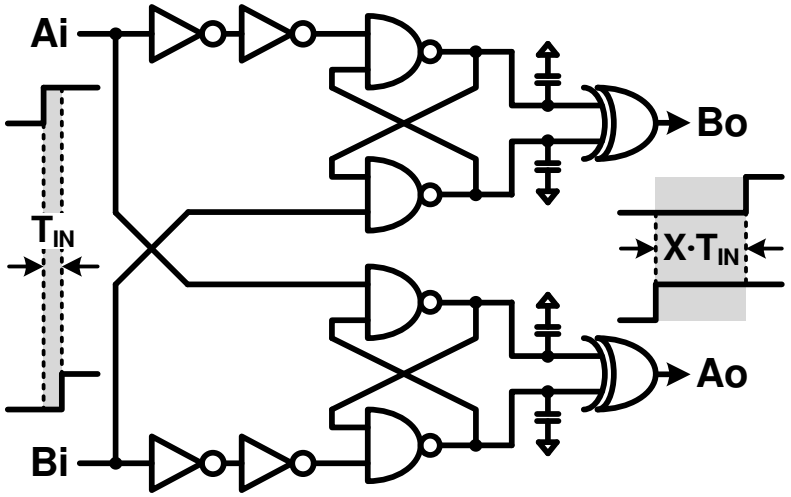
- Amplify time (input phase difference) instead of voltage

Time Amplifier Based TDC Types



- Two-step TDC: Coarse and Fine resolution TDC+TA
- Pipeline TDC: Cascaded stages of TDC+DTC+TA circuits

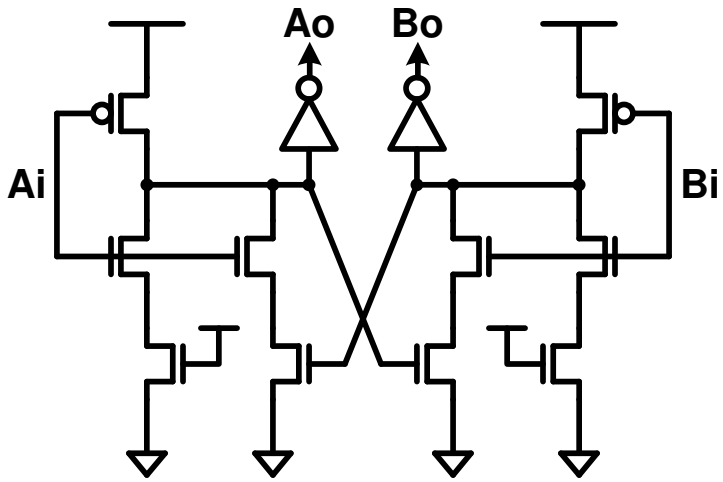
Existing Time Amplifier Circuits



SR latch metastability based

✓ Unpredictable TA gain

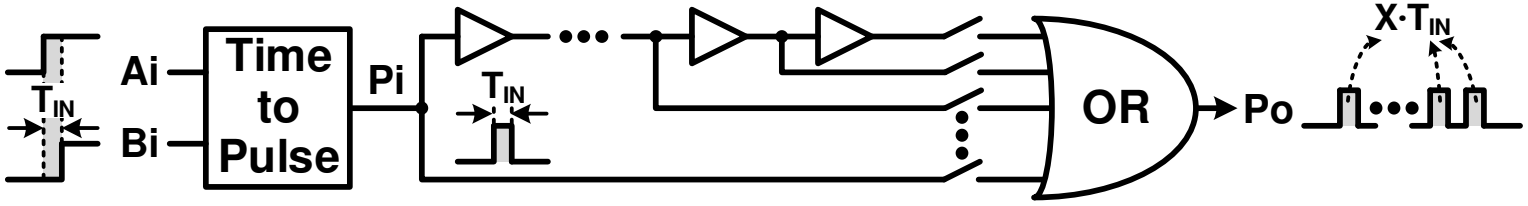
✓ Narrow input range



Discharging time control based

✓ Large TA gain error

✓ Requires background calibration

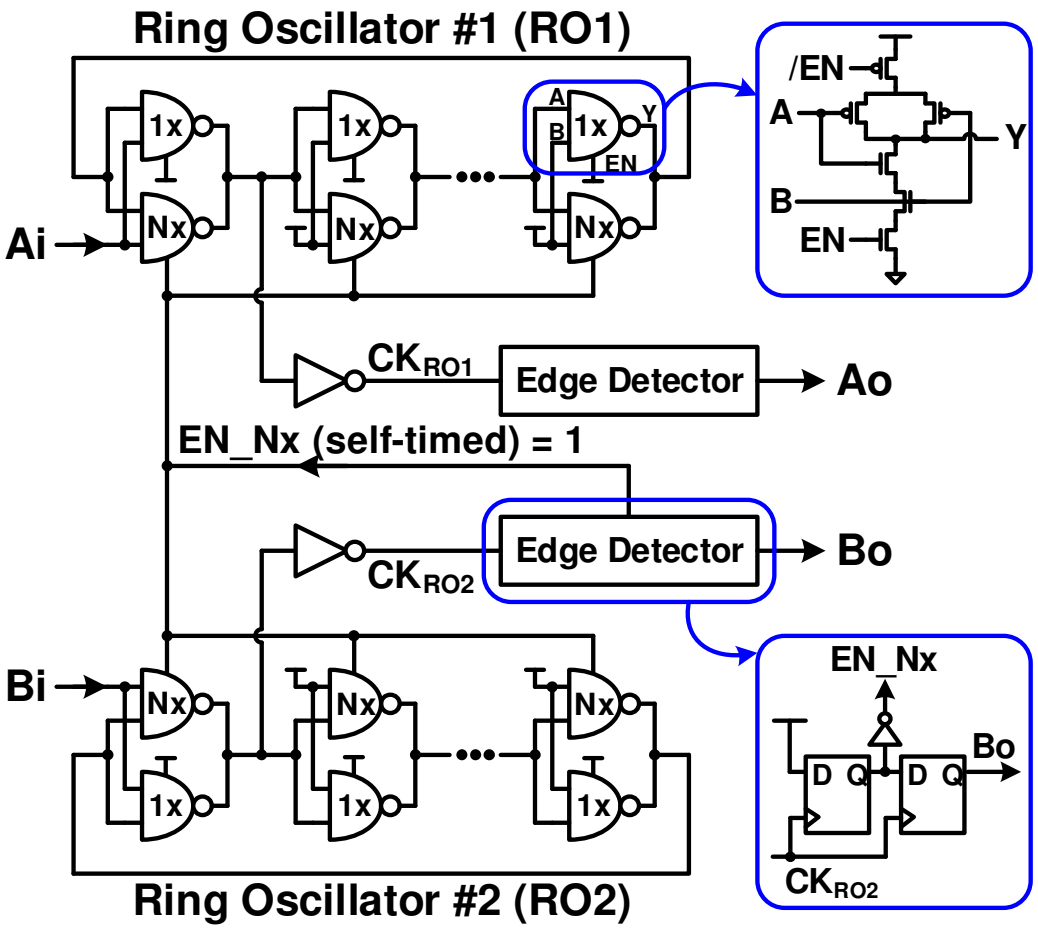


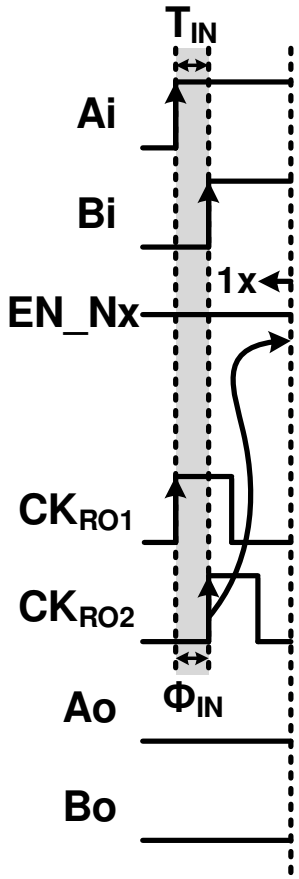
Pulse train based

✓ Susceptible to variation due to summation of multiple pulses

✓ Requires a "gated" delay line based fine TDC

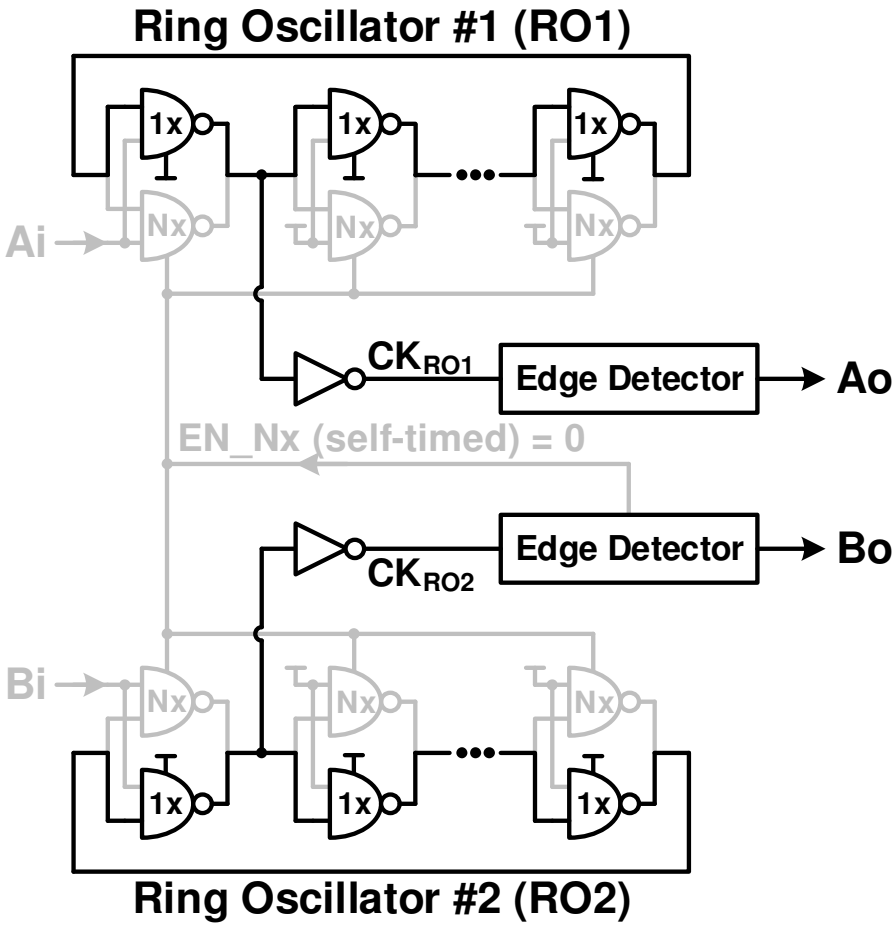
Proposed Switched Ring-Osc TA

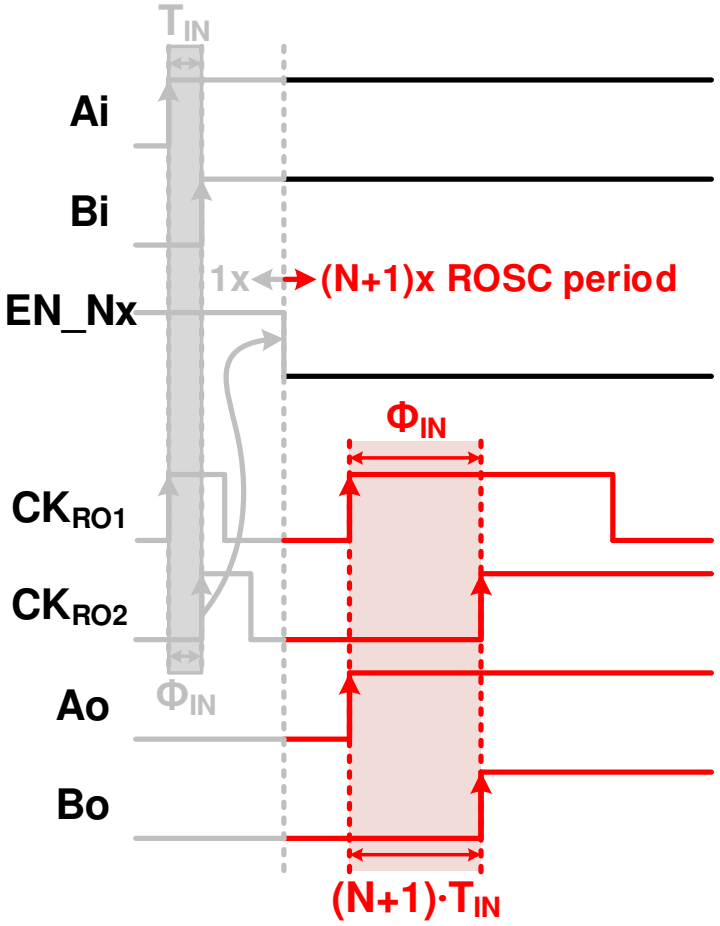




- **Both 1x and Nx gates are switched on w/ input signals**
- **Initial frequency is (N+1)x with '1:N' NAND gate sizing**

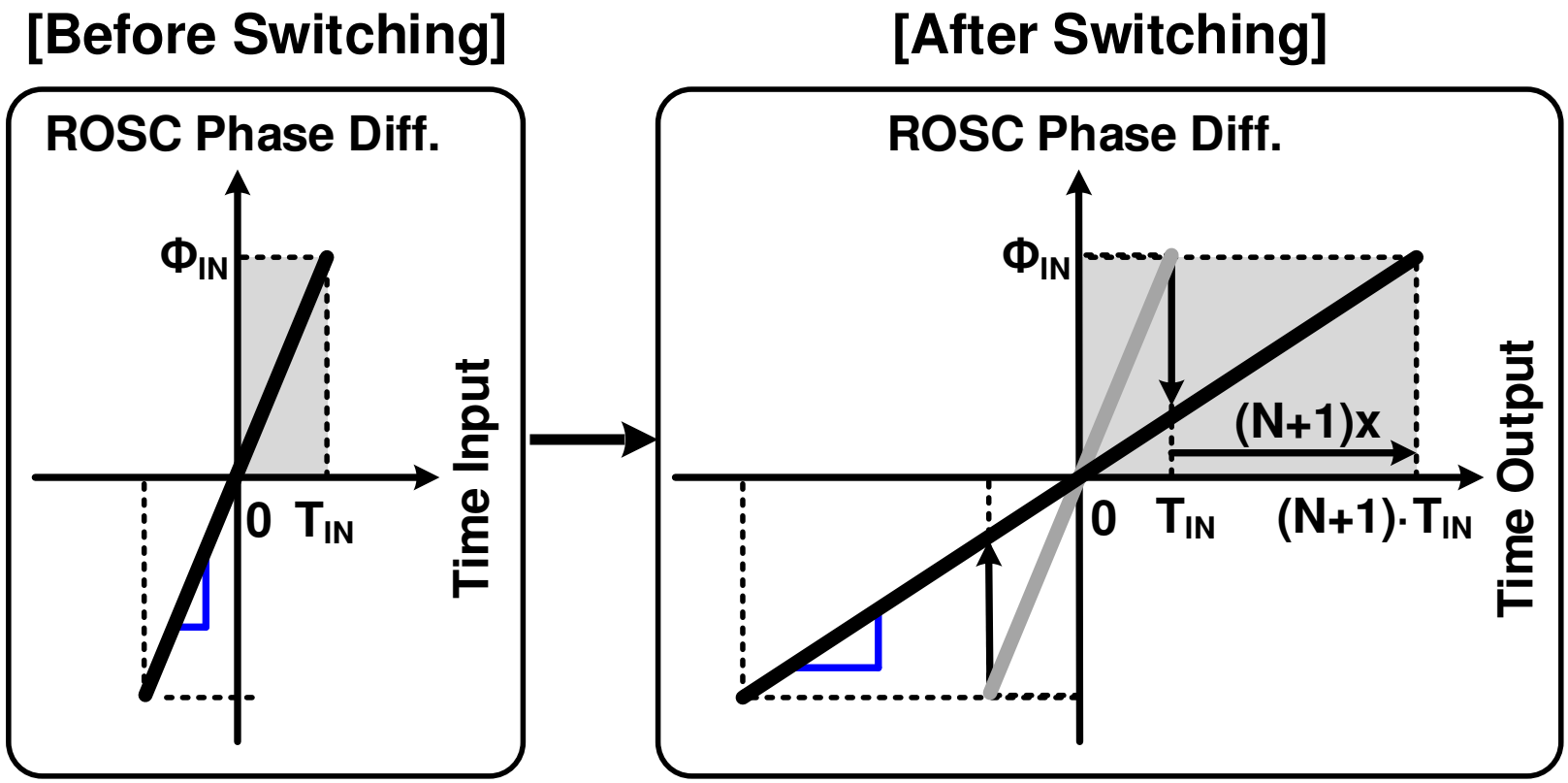
Proposed Switched Ring-Osc TA





- Nx gates are switched off by self-timed EN_Nx (1 => 0)
- ROSC freq. reduces to 1x => Time is amplified by (N+1)x

Mechanism of Proposed SRO-TA

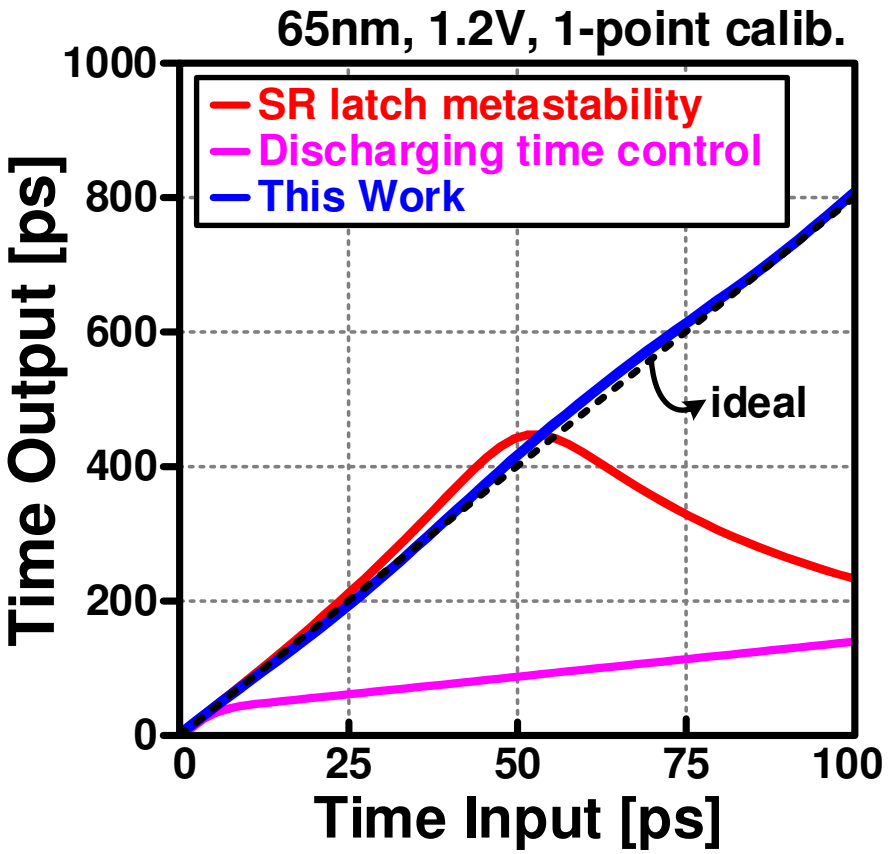


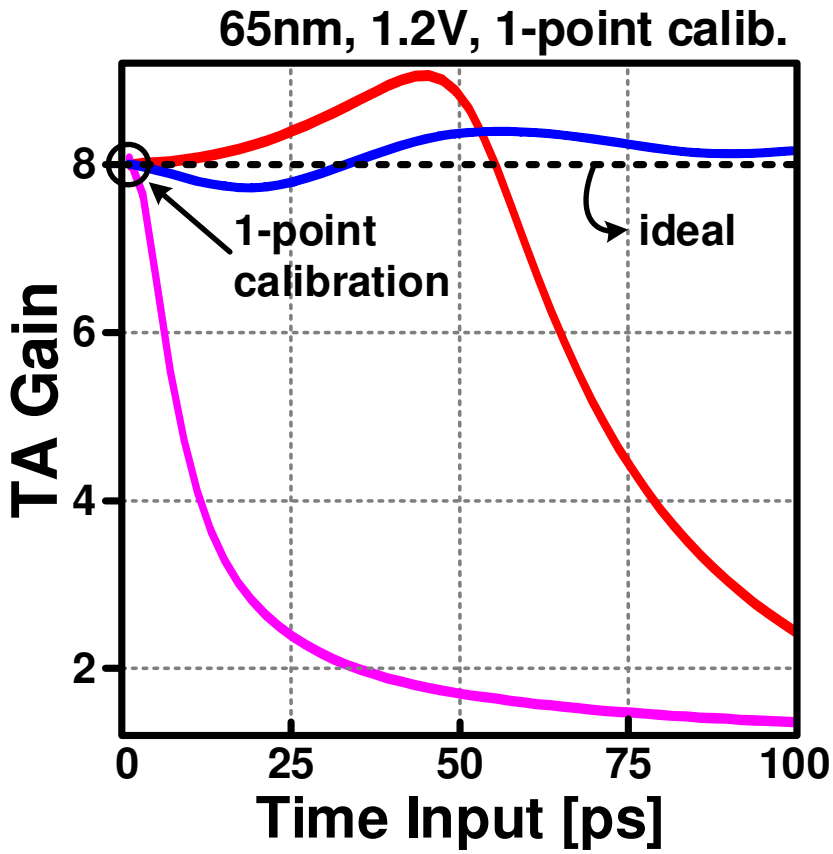
$\Phi_{IN}=\underbrace{2\pi \cdot f_{ROSC}}_{\text{(slope)}} \cdot T_{IN}$

$\Phi_{IN}=\underbrace{2\pi \cdot (f_{ROSC}/(N+1))}_{\text{(slope)}} \cdot (N+1)T_{IN}$

- The slope in the graph represents ring oscillator frequency

Time Amplifier Simulation Results





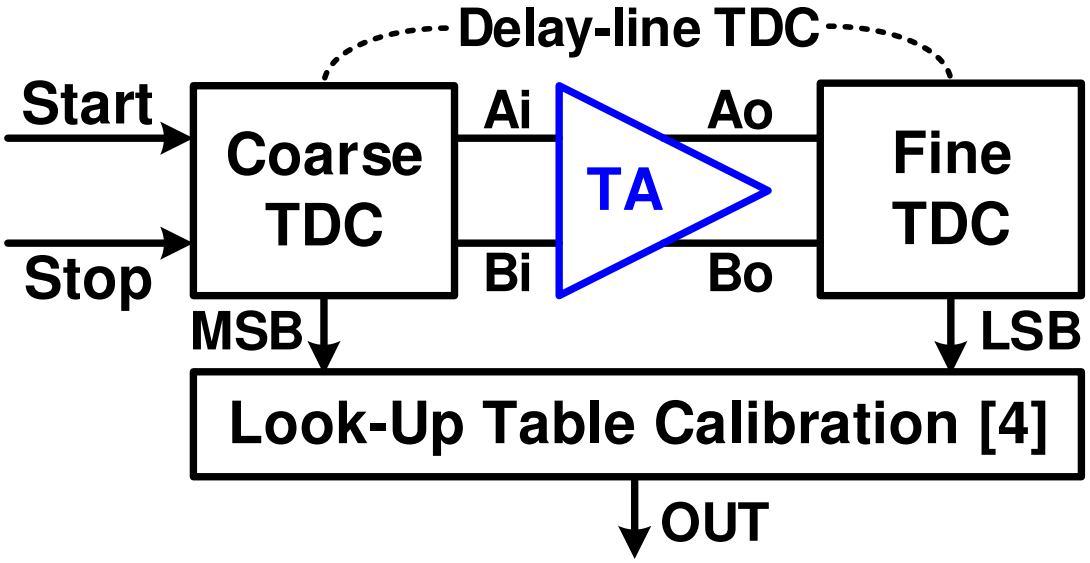
- Existing TA gain error: -71% to 15% and -83% to 3%
- Proposed TA gain error: -4% to 5% @ 100ps input range

Comparison with Existing TAs

	TA Principle	Analog/Digital (Gain Control)	Predictable TA Gain	Required Fine TDC
[1] VLSI'07*	Metastability	Analog	NO	Delay-line
[2] ISSCC'10*	Discharging Time Ctrl	Analog	YES (with calib.)	Delay-line
[3] VLSI'12*	Pulse Train	Digital	YES	Gated Delay-line
This Work	Switched ROSC	Digital	YES	Delay-line

*Original publications where the TA circuits were firstly introduced

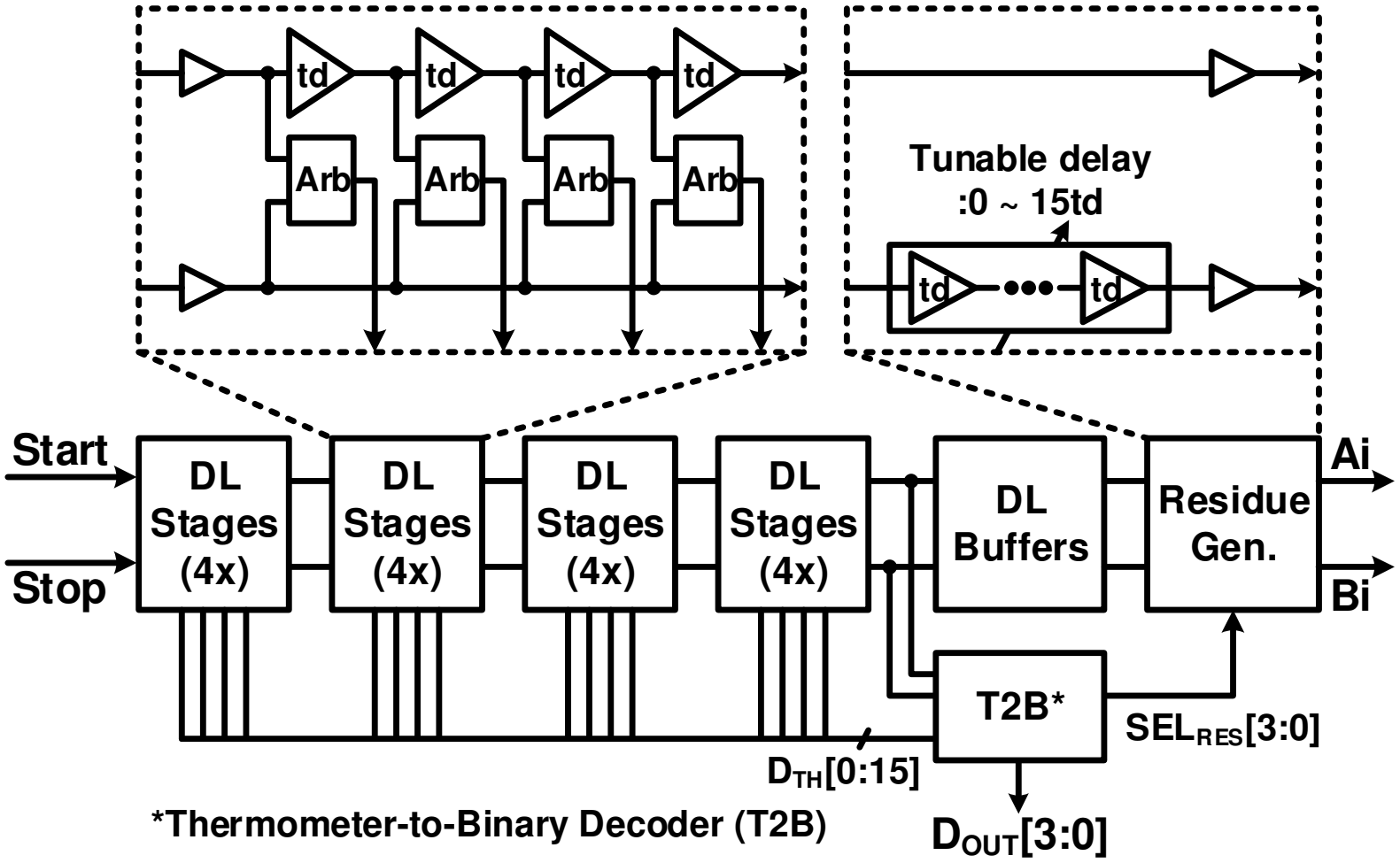
Implemented Two-Step TDC



	6b	7b	8b
Coarse	4b		
TA	4x	8x	16x
Fine	2b	3b	4b

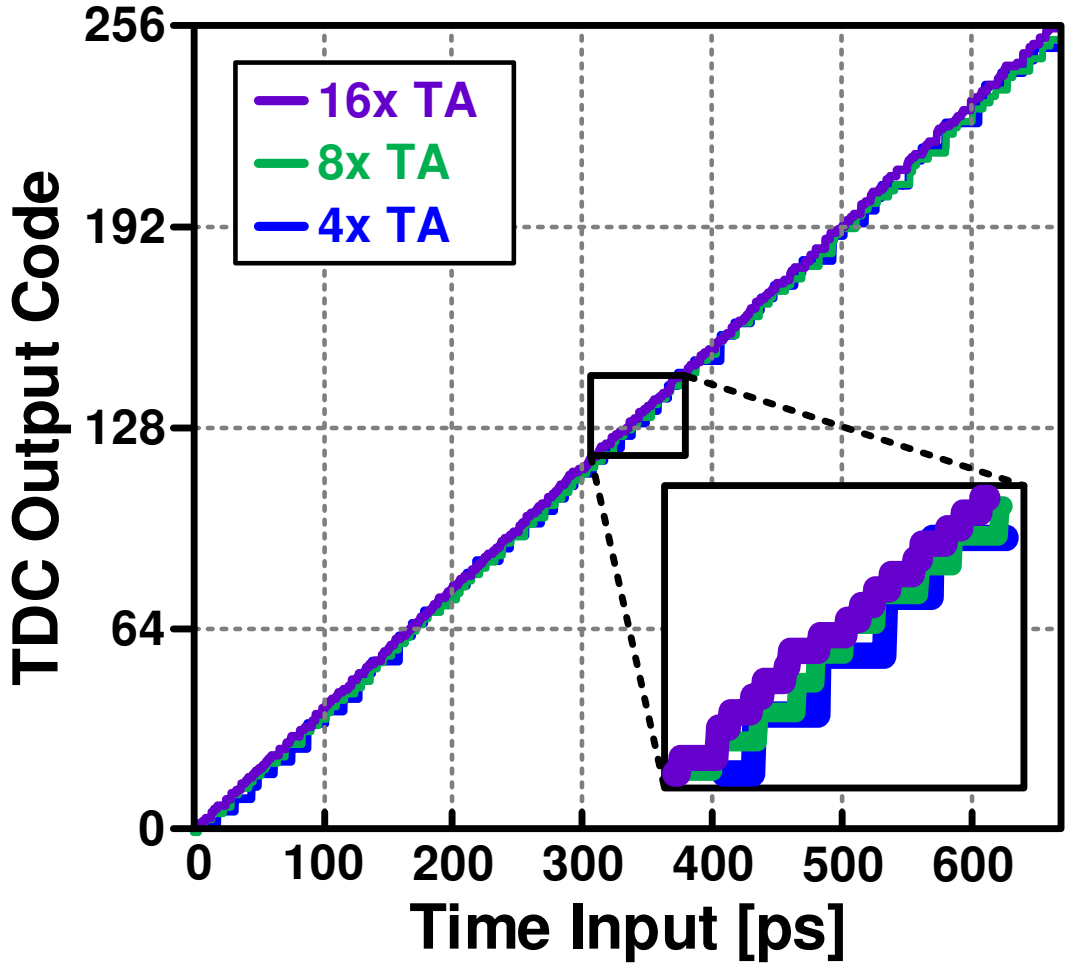
- Proposed two-step TDC consists of coarse/fine delay line TDCs and a proposed time amplifier in between them
- A LUT-based calibration is used to improve TDC linearity

4bit Delay Line TDC Circuit



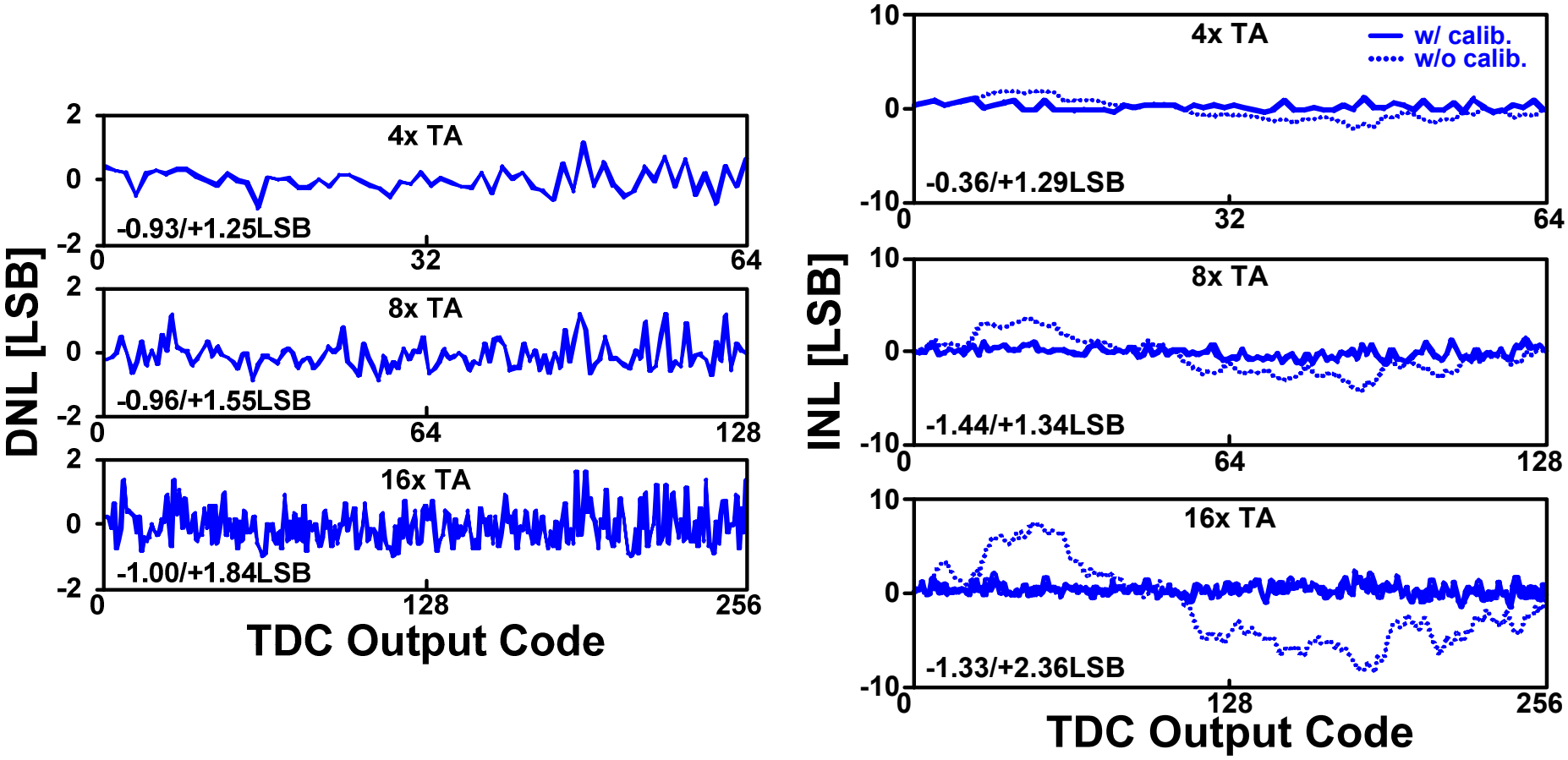
- **A 4b delay line TDC is used for both coarse and fine TDCs**

Measured Output vs. Ramp Input



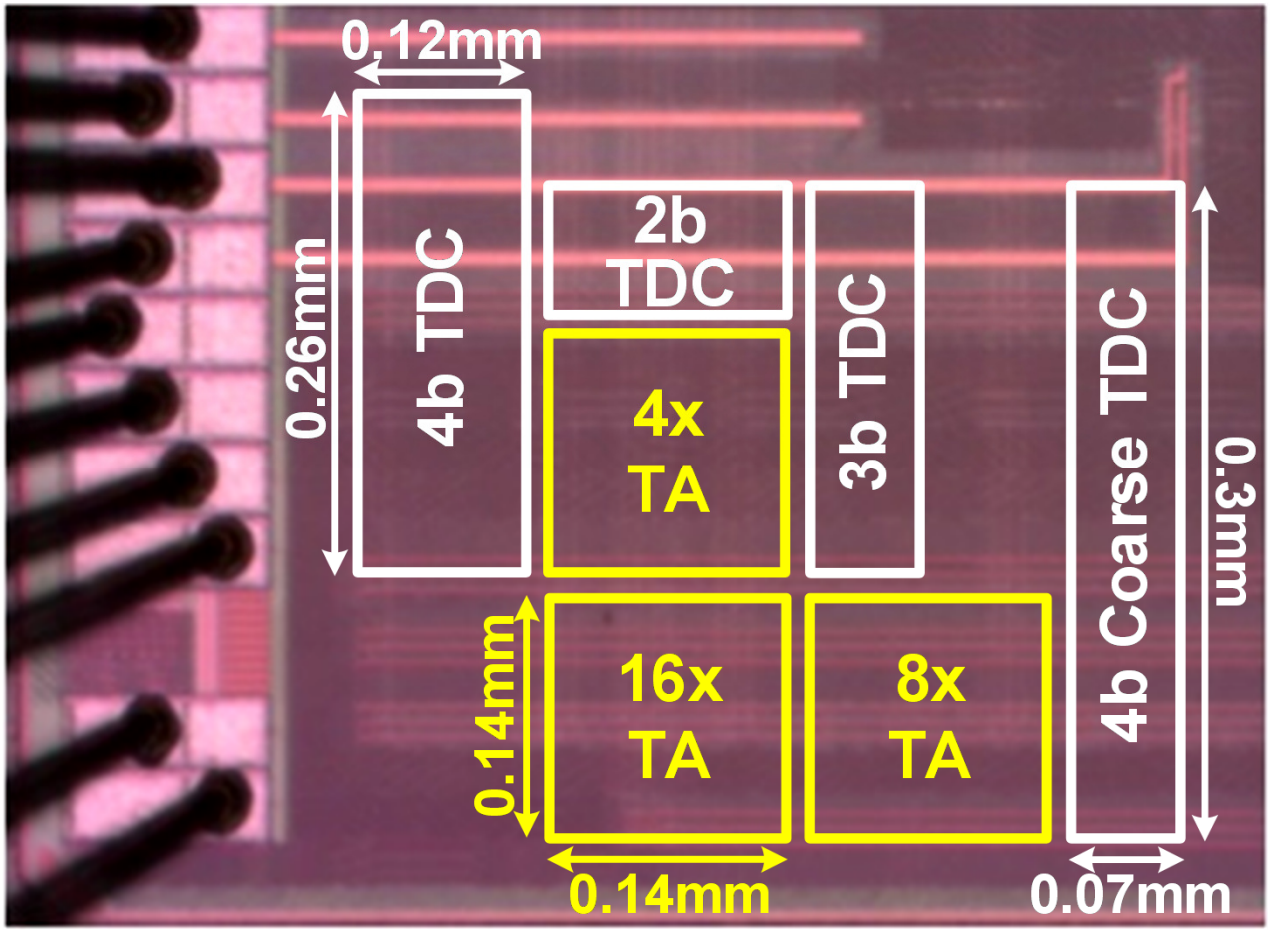
- Measured TDC outputs with respect to a ramp time input

Measured DNL and INL



- Implemented 6/7/8bit two-step TDC with 4/8/16x TA
- Achieved maximum DNL of 1.84LSB and INL of 2.36LSB

65nm Test-Chip Micrograph



Performance Comparison

	[6] CICC'09	[2] VLSI'11	[3] VLSI'12	This Work
Process	65nm	130nm	65nm	65nm
Scheme	Vernier	Pipeline	Two-Step	Two-Step
Resolution	4.80ps	0.63ps	3.75ps	2.60ps
Bits	7	11	7	8
Conv. Rate	50MS/s	65MS/s	200MS/s	80MS/s
Max. DNL	1LSB	0.5LSB	0.9LSB	1.84LSB
Max. INL	3.3LSB	9LSB	2.3LSB	2.36LSB
Power	1.7mW	10.5mW	3.6mW	2mW
Area	0.07mm^2	0.32mm^2	0.02mm^2	0.07mm^2

Conclusion

- **A switched ring oscillator based time amplifier is proposed and fabricated in 65nm CMOS**
- **An 8bit two-step TDC based on the proposed TA achieves 2.6ps time resolution with 16x TA**
- **Measured TDC DNL and INL results show 1.84 and 2.36 LSB while consuming 2mW at 80MS/s and occupying 0.07mm^2**