Two-step Beat Frequency Quantizer Based ADC with Adaptive Reference Control for Low Swing Bio-potential Signals

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***Abstract*— A two-step fully digital beat frequency quantizer based continuous time ADC is demonstrated in a 65nm test chip to achieve high resolution (6-7 ENOB) for direct conversion of low swing (<10mV) bio-potential signals. The resolution of ADC can be adaptively controlled depending on the input signal swing. A triple-sampling technique generates a synchronous ADC output from an asynchronous beat frequency quantizer. The proposed two-step ADC achieves a 44.5dB SNDR which is 5.6dB higher than the previously proposed single step architecture for a 10mVpp, 300Hz differential input signal.**

***Index Terms*—beat frequency, voltage-controlled oscillator, bio-potential, analog to digital converter, two-step.**

I. Introduction

Low power analog-to-digital converters (ADC) are one of the critical building blocks for bio-potential (e.g. ECG, EMG, EEG) acquisition systems. In many cases, the biggest bottleneck in making these systems low power and area efficient, as shown in Fig. 1, is the overhead of the analog front end (AFE) circuits such as low noise amplifier and variable gain amplifier. Most low power ADC designs [4, 5] do not account for the complexity and power overhead of the AFE circuits as they assume an input signal with a rail-to-rail swing. One recent attempt to address the AFE power was the beat frequency quantizer based ADC (BFADC) design to directly convert sub-1mV input signals [6] (shown in Fig.2). Performance of the BFADC was further improved in [7] by utilizing a multi-phase VCO and making it noise shaping. A major drawback of this technique, however, is that quantization error (Δ_q) increases with the increase in signal swing, due to inherent nonlinearity in the system. This shortcoming limits the performance for input amplitude more than only a few mV. Most bio-potential signals, as shown in Fig.2, have a maximum amplitude and common-mode voltage variation in the range 5-10mV [8] that could significantly degrade the BFADC performance. In order to address this issue, a new two-step beat frequency (BF) conversion technique is proposed in this paper, where the reference frequency is adaptively changed based on the input signal.

II. Proposed Two-step Beat Frequency Quantizer

Fig. 3 explains the basics of the BF detection scheme and its advantage over VCO based linear counting [9]. Linear quantizer counts number of VCO clock cycles in a sampling period (CK_s). Therefore, output code (D_{OUT})

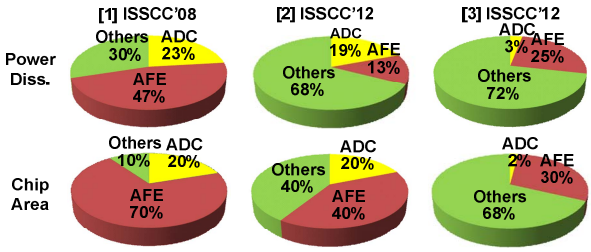

Fig. 1. Power and area breakdown of biopotential acquisition ASICs [1,2,3]. AFE (=LNA, VGA, preamp) accounts for a major portion of the chip power and area.

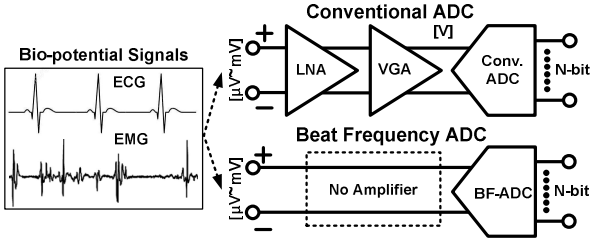

Fig. 2. Beat Frequency ADC can reduce the AFE overhead by directly converting low swing bio-potential signals.

changes linearly with input frequency (f_{SIG}) and Δ_q plot, which looks like a saw-tooth wave has a fixed maximum value. Low swing input must be adequately amplified before applying to VCO for good SNR. In BF quantizer [6,7], on the other hand, f_{SIG} is compared with another reference frequency f_{REF} and their difference i.e. beat frequency ($\Delta f = f_{REF} - f_{SIG}$) is utilized for quantization. Due to non-linear D_{OUT} vs f_{SIG} relationship, the slope is very high for small Δf. Therefore, a small change in f_{SIG} creates large variation in D_{OUT}. As a result Δ_q reduces significantly for small Δf achieving much better resolution for low swing signals. This allows us to eliminate AFE from the system, reducing the power and area overhead. To explain it quantitatively, if frequency difference between f_{REF} and f_{SIG} is 1%, D_{OUT} will be 100. Now 1% reduction in f_{SIG} will increase the difference to 2% and D_{OUT} will be 50. Therefore only 1% change in input changes the output count by 50. Whereas, 1% input change in linear quantizer changes the output code by only 1 if full scale is 100. However, Δ_q increases significantly for higher Δf, increasing quantization noise and limiting the resolution of ADC for relatively large input amplitude.

Proposed two-step BF detection scheme (shown in bottom part of Fig. 3) solves this issue by introducing

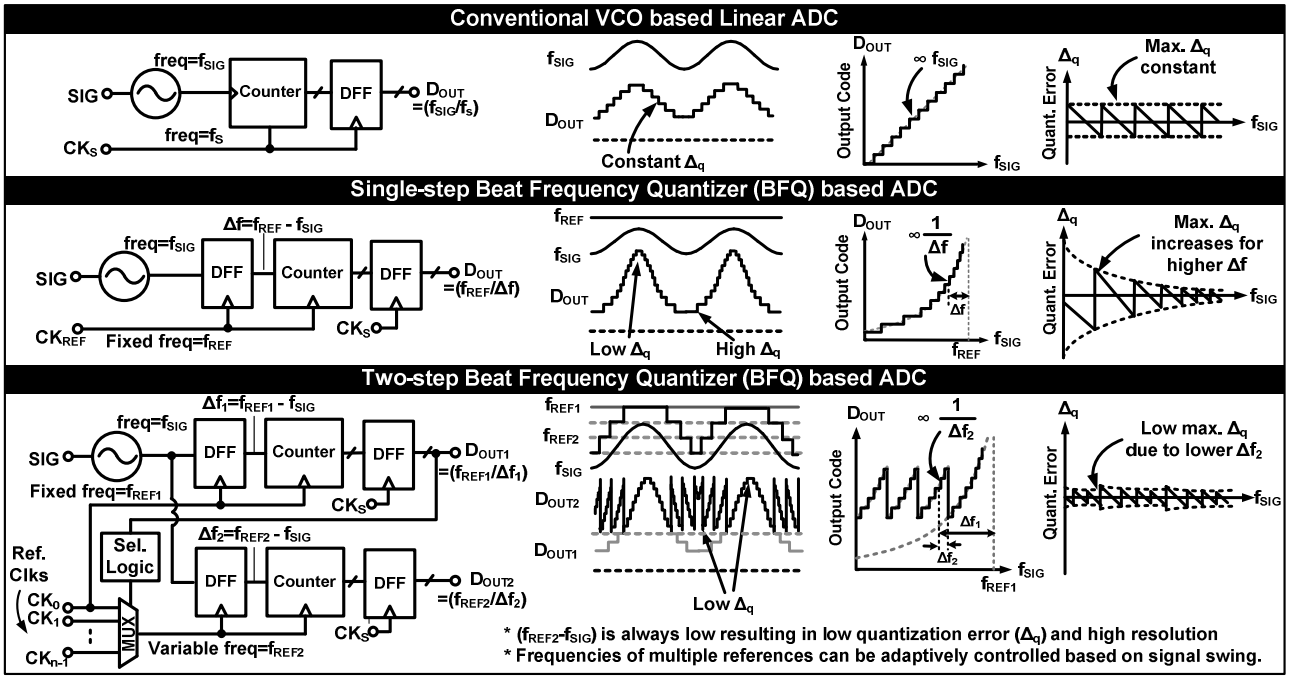

Fig. 3. Operation of the conventional VCO based linear ADC, the original BFADC and the proposed two-step BFADC.

multiple reference frequencies and selecting the appropriate one depending on the input signal level. First step is same as in the original BFADC and is used to detect the signal level using rough BF count (D_{OUT1}). Based on the value of D_{OUT1}, the appropriate reference clock (CK_{0-3}) is selected using selection logic and MUX. Subsequently, the final BF count (D_{OUT2}) is obtained in the second step. In this way, high output count is always maintained and better resolution is achieved for signals with a wider dynamic range. Although f_{REF2} varies with input, its value corresponding to each D_{OUT2} count is known from D_{OUT1} and signal can be reconstructed accurately. The number of reference levels and spacing among them can also be adaptively controlled depending on the type of bio-potential signal and its maximum swing.

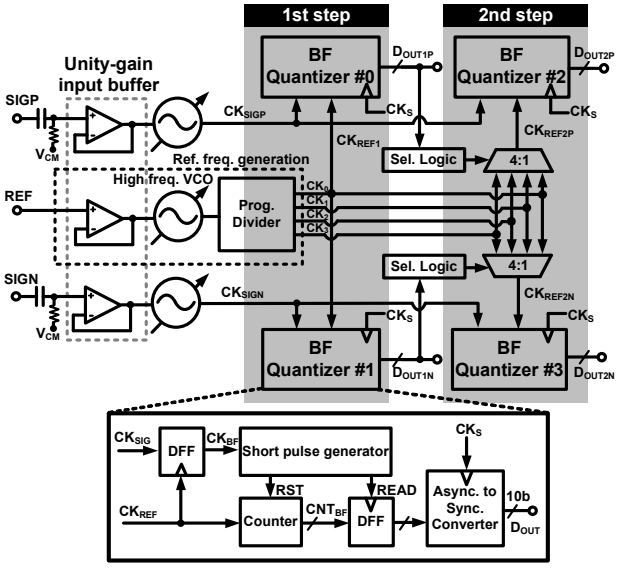

Fig. 4. Block diagram of the proposed two-step BFADC.

III. Circuit Implementation

Fig. 4 describes the circuit implementation of the proposed ADC. Differential AC coupled inputs (SIGP, SIGN) control the frequency of the two VCOs to generate input clocks (CK_{SIGP}, CK_{SIGN}). Gain of these VCOs i.e. K_{VCO} is lower than the one implemented in [6,7] to cover maximum 10mV range of bio-potential signals without degrading resolution. Input common-mode voltage (V_{CM}) is adjusted externally. Multiple reference clocks (i.e. CK_{0-3}) with fixed frequency difference can be generated in many ways. Firstly, using a frequency synthesizer and changing the multiplication factor depending on the decision made by the first step. Secondly, generating multiple voltage references and feeding it to a reference oscillator. Thirdly, dividing the output of a high frequency VCO with a programmable frequency divider where the division factor is decided by the first step. As the focus of this work is mainly on the ADC implementation, we chose option #3 to reduce circuit complexity at the cost of power consumption of the high frequency VCO. Note that a single reference generation block can be shared among multiple ADC channels. In our implementation, four reference frequencies are generated from the reference generation block. Depending on the signal swing, the frequency difference among different references is made adaptive by controlling the frequency division factor. Each

BF quantizer consists of a D flip-flop to detect BF ($\Delta f = f_{REF} - f_{SIG}$), a counter that resets at every BF cycle by a short-pulse generator and a triple-sampling asynchronous-to-synchronous converter to read counter output at a fixed sampling rate without meta-stability. Similar to [7], quantization noise in each cycle is accounted for in the subsequent BF cycle without resetting the VCO accomplishing first-order noise shaping. BF quantizers #0 and #1 form the differential first step while #2 and #3 form the second step quantizer. Same input clock is applied in both steps for continuous-time operation. The highest frequency reference clock (CK_0) is utilized by each BF quantizer in the first step as reference (CK_{REF1}) and based on its output code the appropriate reference clocks (CK_{REF2P}, CK_{REF2N}) are selected in the second step.

IV. Triple-Sampling Synchronization Technique

The BF counter is updated at every edge of the BF clock (CK_{BF}), which varies with signal voltage and PVT variations. Since the rate at which digital data is generated from the BF quantizer is not constant, an asynchronous-to-synchronous converter is required to sample this data at a constant rate for subsequent digital blocks. Otherwise, a wrong value may be sampled due to meta-stability and delay mismatch among different data paths. This issue was not addressed in prior work. Fig. 5 shows the triple-sampling method designed for this purpose. The incoming asynchronous data (D_{async}) is sampled three times by phase shifted versions of an external sampling clock (CK_s) to generate $OUT_{1\text{-}3}$. These outputs are then compared to detect data transition point. For example, if OUT_1 is different from OUT_2 and OUT_3, data transition occurs between rising edges of CK_1 and CK_2. Data transition timing conditions and selected correct sampled data are shown with a timing diagram example in Fig. 5. As long as sampling clock period is lower than minimum beat period, we will not miss any data due to synchronization.

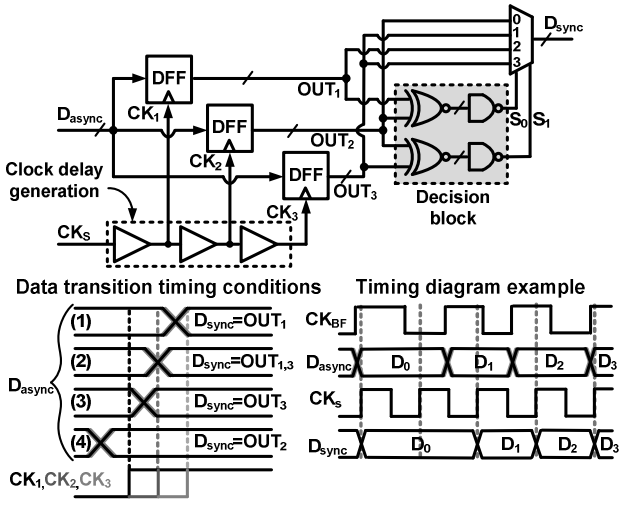

Fig. 5. Triple-sampling technique for data synchronization.

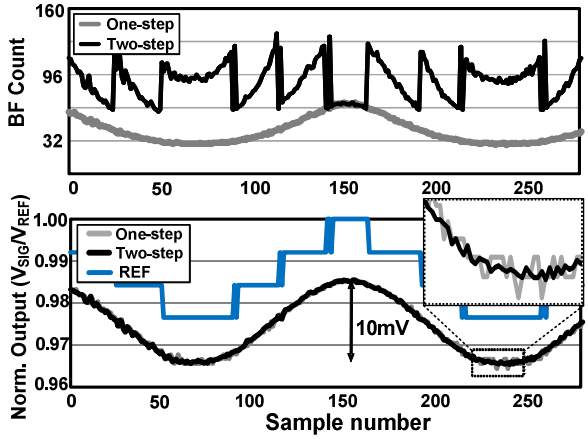

Fig. 6. Measured time-domain BF count and reconstructed signal from one of the differential ADC outputs.

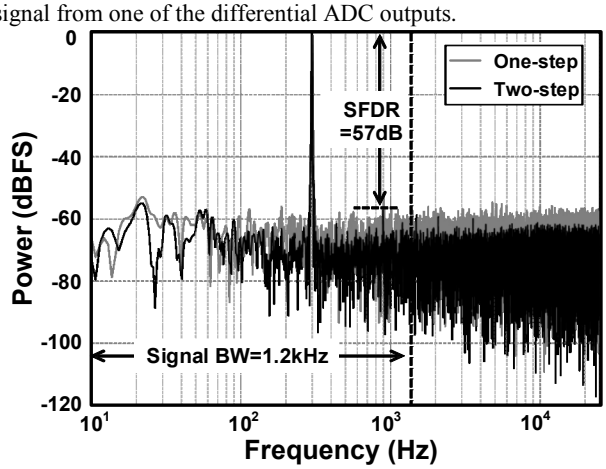

Fig. 7. Measured FFT for a 10mVpp, 300Hz differential sinusoidal input sampled at 50 kHz.

V. 65nm Test Chip Measurement Results

A test chip was fabricated in a 65nm LP CMOS process to demonstrate the proposed techniques. Fig. 6 shows the measured BF count and the reconstructed output at each steps of the BFADC for a 300Hz, 10mVpp differential sine input. Sampling frequency is 50kHz. Reconstructed signal clearly shows lower quantization noise for the two-step case due to higher BF count. Measured SNDR for a 1.2kHz signal bandwidth is 44.5dB and 38.9dB for the two-step and one-step cases, respectively (Fig. 7). Noise shaping is not clearly visible due to low frequency device flicker noise. Measured SFDR is 57dB. Fig. 8 shows the measured SNDR as a function of input amplitude while keeping the maximum count constant at 128. As expected, the difference between two-step and one-step SNDR increases with larger signal amplitude. SNDR is 0dB for input amplitude of -86dBFS (i.e. 62.5µVpp). Ideal linear ADC (full scale count 128) has much lower SNDR than measured BFADC. Table 1 compares the performance of this ADC with other state-of-the art designs when 10mVpp is directly applied at the input. Results from [6, 7]

TABLE I PERFORMANCE COMPARISON

Parameters	This Work		[4] ESSCIRC'11	[10] VLSI'11	[11] VLSI'12	[12] CICC'14
ADC Type	One- step Beat freq.	Two- step Beat Freq.	CT- ΣΔ	VCO Based	Two-step ΣΔ	PWM Based ΣΔ
Process/Supply	65nm/1.2V		0.18µm/1.4V	90nm/1.15V	0.13µm/1.2V	0.18µm/1.8V
Input freq./BW	300Hz/1.2kHz		21Hz/256Hz	30kHz/8MHz	500kHz/5MHz	221.5kHz/1MHz
Sampling Rate	50kHz		57kHz	640MHz	80MHz	144MHz
IN_{0dB}[dBFS]*	-86		-80	-65	-71	-54
$SNDR_{10mVpp}$**	38.9dB	44.5dB	40dB	20dB	22dB	20dB
$ENOB_{10mVpp}$**	6.17	7.1	6.35	3.03	3.36	3.03
Power	34µW	38µW	13.3µW	4.3mW	8.1mW	2.7mW
FoM_{10mVpp}[pJ/Conv]***	197	115	318	33	79	165.3
Chip area	0.096mm^2		0.51mm^2	0.1mm^2	0.37mm^2	0.0275mm^2

*Input amplitude at SNDR=0dB, **SNDR/ENOB for 10mVpp, ***FoM = $\frac{Power}{2^{ENOB_{10mVpp}*2*BW}}$

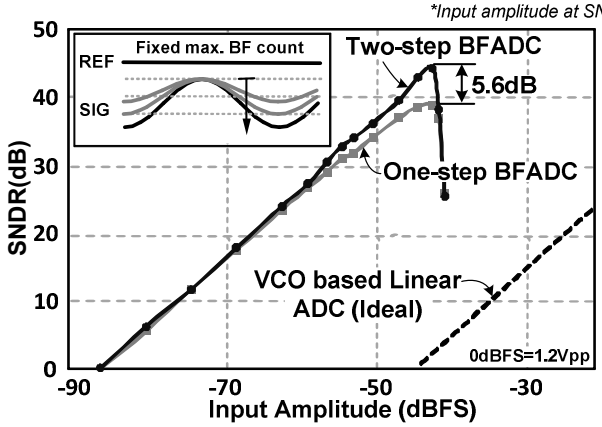

Fig. 8. Measured SNDR vs. input amplitude for fixed maximum BF count. Ideal linear ADC has much lower SNDR for input amplitude up to -40dBFS (12mVpp).

are not included here as their operation is limited to only a few mV signals (<6mV) due to higher K_{VCO}. However, one-step case is similar to [6]. The die photo is shown in Fig. 9 indicating an active area of 0.096mm^2. ADC core consumes 38µW (not including the reference generation block) under a nominal 1.2V supply of which 30µW is consumed by VCOs and only 8µW for the two-step BF quantizer switching. Calculated FoM is higher than [10, 11] due to the very low application bandwidth.

VI. CONCLUSION

In this paper, we have presented a fully-digital beat frequency quantizer based two-step ADC by controlling the reference signal adaptively depending on the signal swing. Additionally, a triple sampling based synchronization technique is implemented to sample the ADC output data at a fixed sampling rate while eliminating meta-stability issues. A 65nm test chip of the proposed two-step ADC demonstrates a SNDR of 44.5dB (i.e. 7.1 ENOB), which is 5.6dB higher than the previously proposed single step scheme, for a 10mVpp input differential signal sampled at 50 kHz.

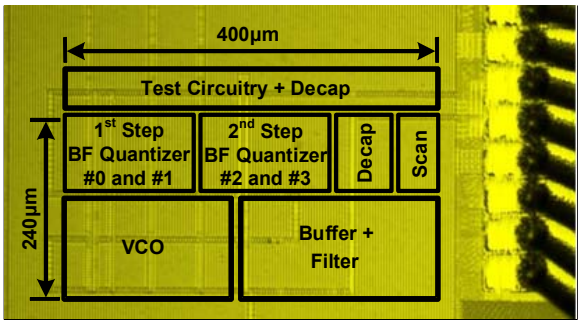

Fig. 9. 65nm die photo showing different blocks of the two step BFADC test chip. Total active area is 0.096mm^2.

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