Leakage Modeling for Transistors with Steep Sub-threshold Slope Considering Random Threshold Variations

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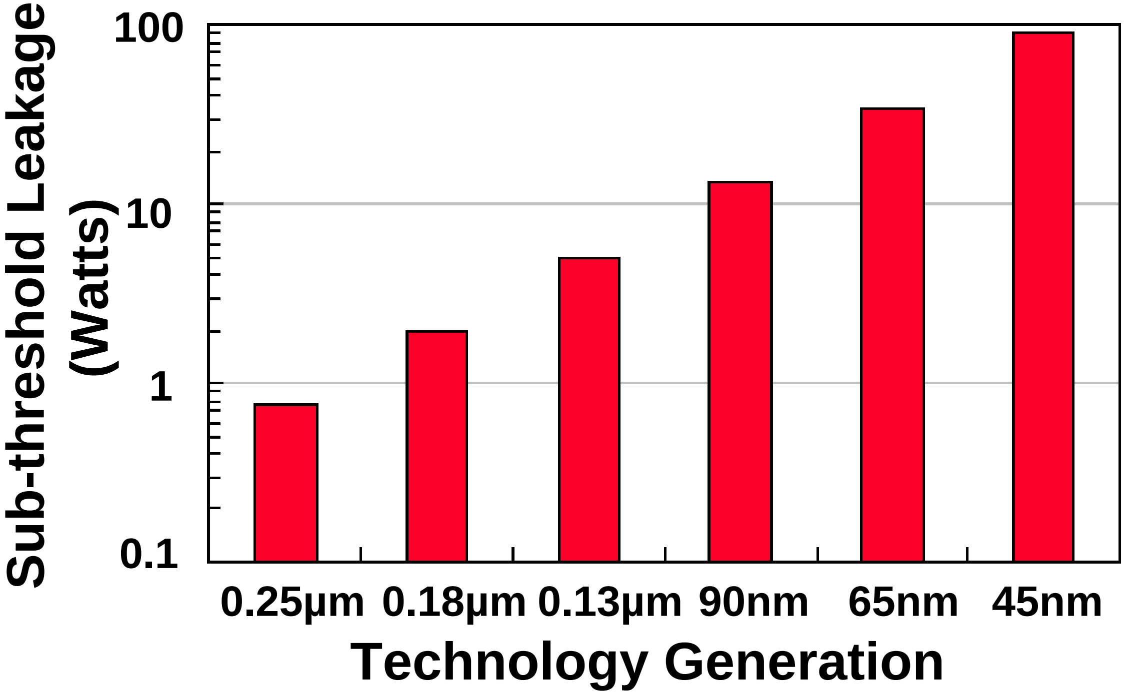
Outline of Presentation

- **Introduction to steep transistors and tunneling FETs**
- **Statistical leakage estimation of steep transistors**
- **Monte-Carlo simulation results**
- **Circuit example: SRAM delay modeling**
- **Conclusion**

MOSFET Leakage Power

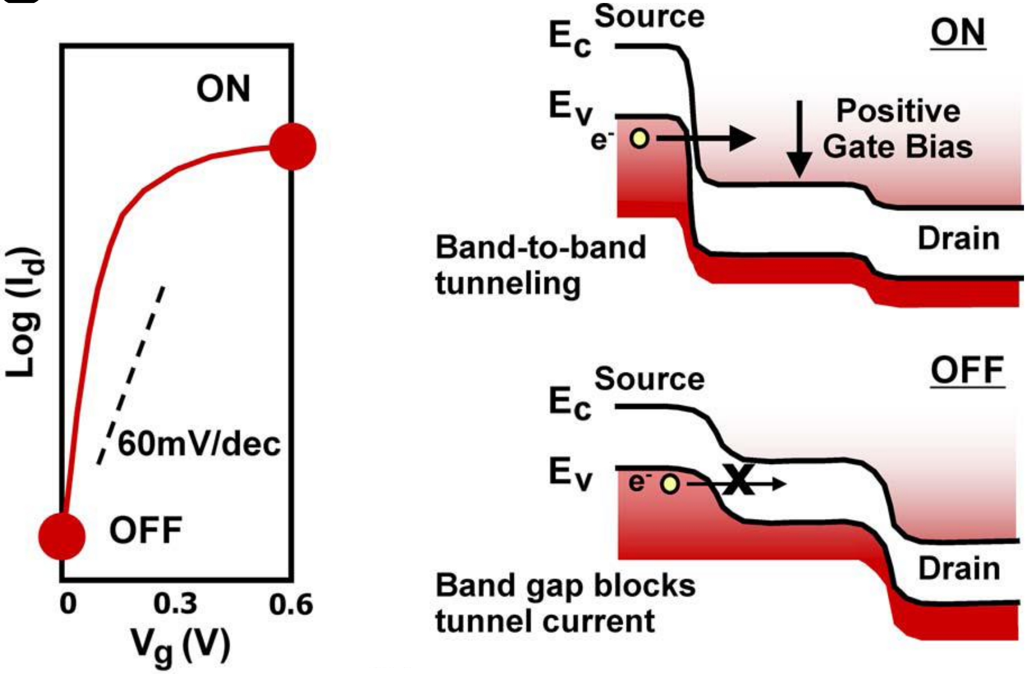
- **Challenge:** Sub-threshold current increases exponentially with every generation!



S. Borkar, Intel Corporation

- **Solution:** Reduce threshold voltage by using steep transistor (e.g. Tunneling FET, Ferro-electric FET)

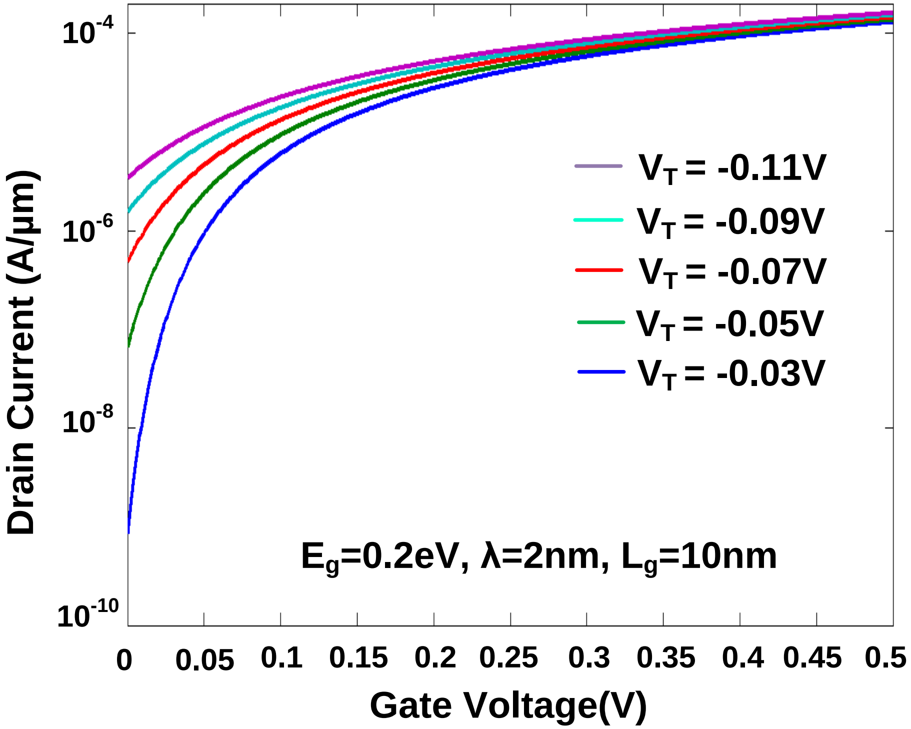
Tunneling Field Effect Transistor (TFET)



L. Chang, et. al., Proceedings of the IEEE 98.2 (2010)

- ON state: Positive gate voltage lowers the conduction band edge in the channel
- OFF state: Channel conduction band edge is pushed above the source valence band edge

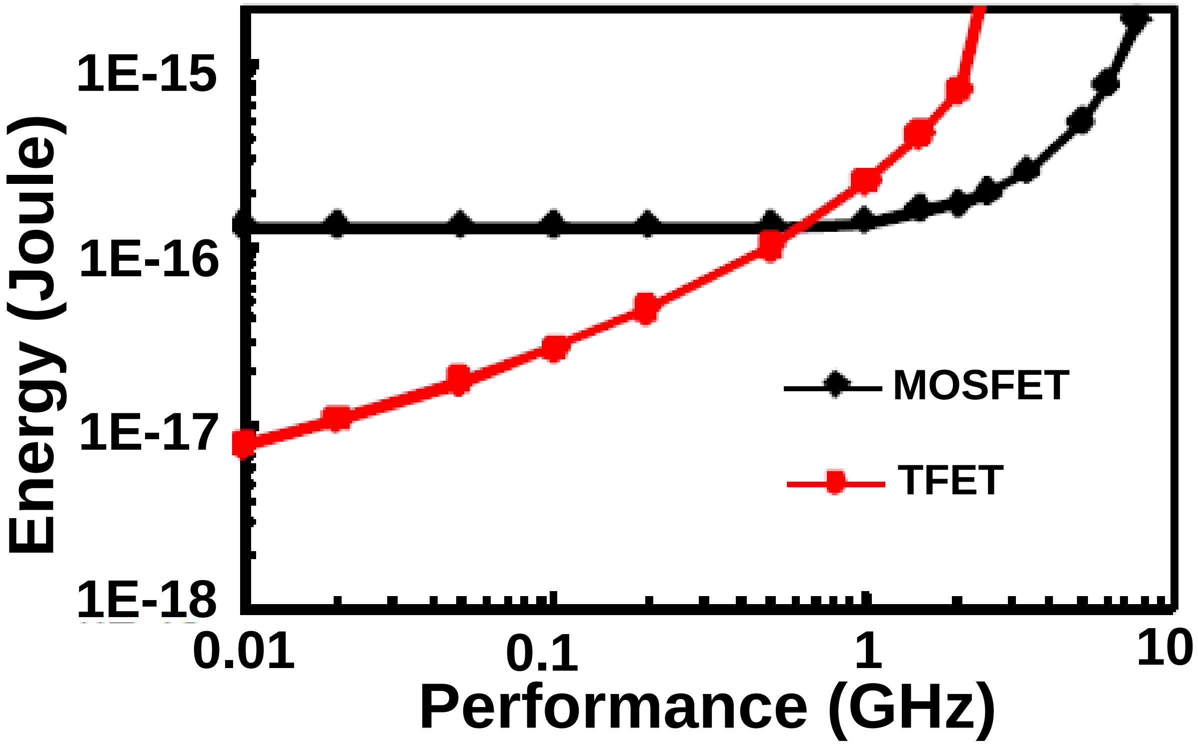
TFET I_d-V_g Characteristics



$$I_d = W \cdot A \cdot E_s \cdot e^{-B/E_s}$$

- $E_s = (V_g - V_T)/\lambda$ where λ is the effective tunneling distance
- Issues: Slope worsens at higher gate voltages, low ON current at high gate voltages

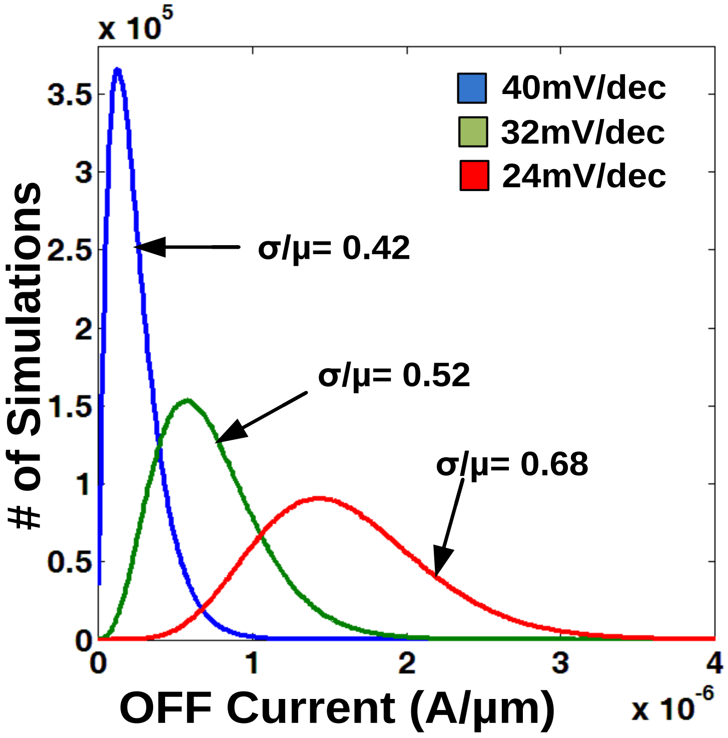
Energy-Performance Comparison: TFET vs. MOSFET

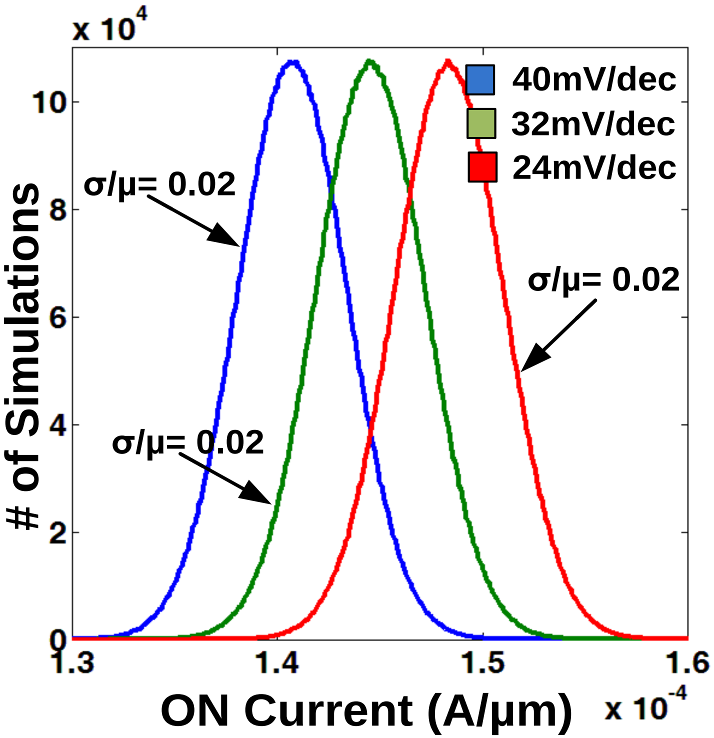


H. Kam, et. al., IEDM 2008

- Sub-threshold slope of TFET is function of V_{gs}
- Average sub-threshold slope of TFET is larger than MOSFET
- TFET is energy efficient for frequency below 1GHz

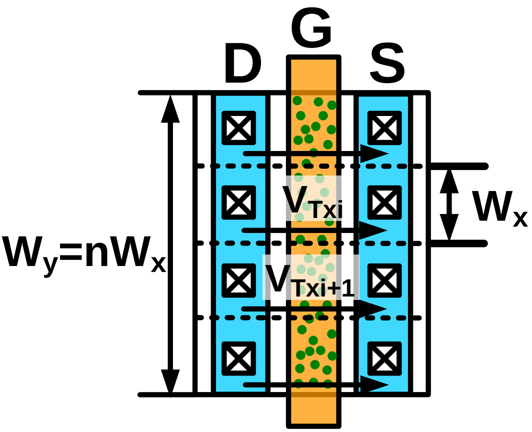
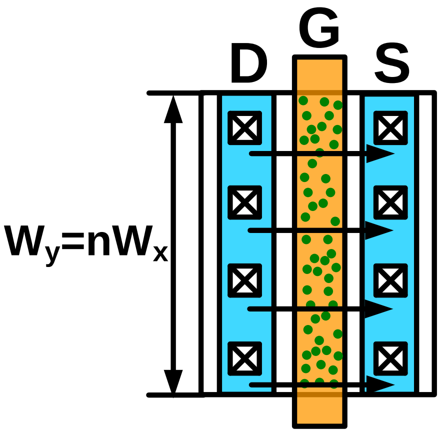
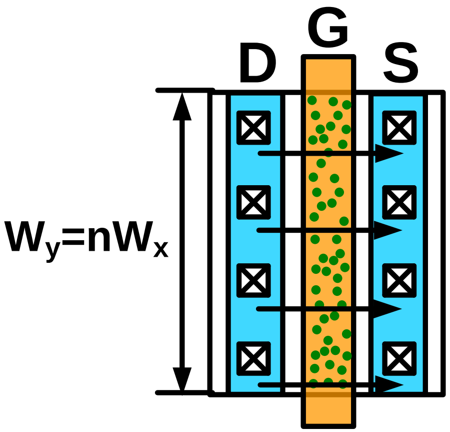
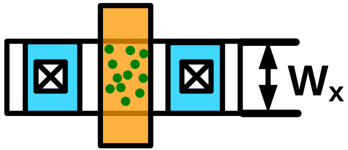
V_T Induced OFF and ON Current Distribution of Tunnel FET





- Monte Carlo simulation assumption: σ_{VT}/μ_{VT} =0.1
- ON current is independent of sub-threshold slope
- OFF current depends on sub-threshold slope

Statistical Leakage Estimation Techniques

<table>
<tr><th>Golden</th><th>Square-root</th><th>Proposed</th></tr>
<tr>
<td>
V_{Txi}: V_T of i-th sub-device</td>
<td>
V_{Ty}: effective V_T</td>
<td>
V_{Ty}: effective V_T</td>
</tr>
<tr>
<td colspan="2">Given inputs for reference device:
$W_x, \mu_{V_{Tx}}, \sigma_{V_{Tx}}$</td>
<td> </td>
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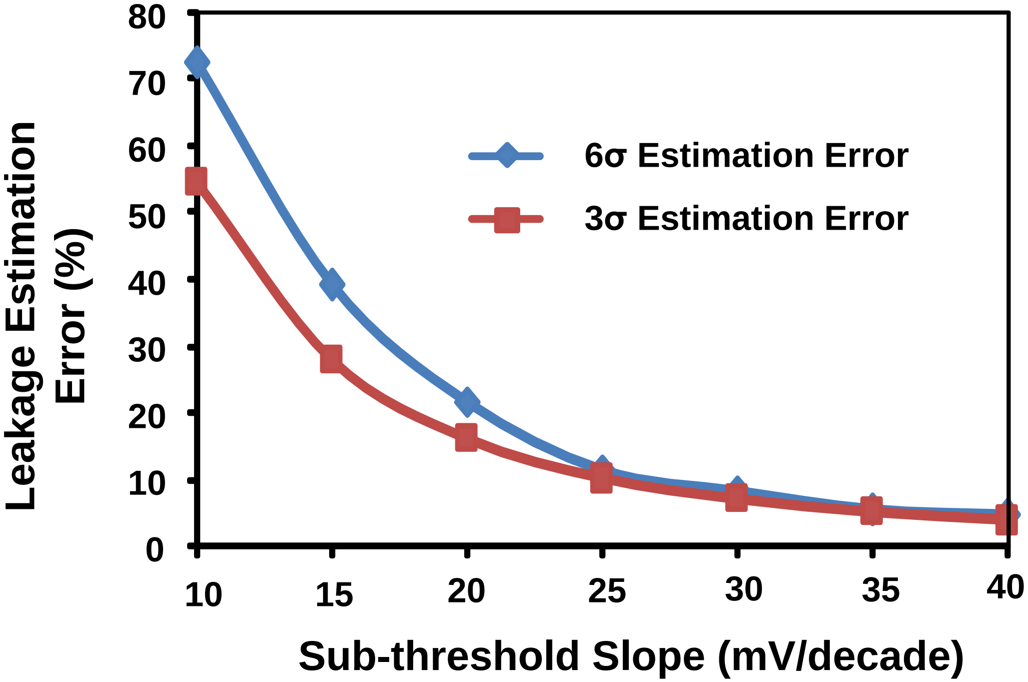
<tr>
<td>$$I_{leak} \propto \sum_{i=1}^{n} W_x e^{-K_2 V_{Txi}}$$ $$\begin{cases} \mu(V_{Txi}) = \mu_{V_{Tx}} \\ \sigma(V_{Txi}) = \sigma_{V_{Tx}} \end{cases}$$</td>
<td>$$I_{leak} \propto W_y e^{-K_2 V_{Ty}}$$ $$\begin{cases} \mu(V_{Ty}) = \mu_{V_{Tx}} \\ \sigma(V_{Ty}) = \sigma_{V_{Tx}} / \sqrt{\dfrac{W_y \cdot L_y}{W_x \cdot L_x}} \end{cases}$$</td>
<td>$$I_{leak} \propto W_y e^{-K_2 V_{Ty}}$$ $$\begin{cases} \mu(V_{Ty}) = f_\mu(W_y, \mu_{V_{Tx}}, \sigma_{V_{Tx}}) \\ \sigma(V_{Ty}) = f_\sigma(W_y, \mu_{V_{Tx}}, \sigma_{V_{Tx}}) \end{cases}$$</td>
</tr>
</table>

J. Gu, et. al., DAC 2007

Leakage Estimation Error Using Square Root Method



- Mean value of V_T of device to be modeled is same as the mean value of the reference device
- % error increases with steeper sub-threshold slope

Leakage Estimation: Wilkinson's Method

- Basic Premise: Sum of log-normal distributions of a number of random variables can be expressed as a single log-normal distribution
- Define variables:

1. Mean and standard deviation of reference Gaussian random variable X_i are (m_{X_i}, σ_{X_i})
2. Mean and standard deviation of Gaussian random variable to be estimated Y are (m_y, σ_y)
3. r_{ij} is the correlation coefficient between random variables X_i
4. Define log-normal distributions corresponding to Y and X_i

$$e^y \text{ and } \sum_{i=1}^{n} \frac{1}{n} e^{X_i}$$

Wilkinson’s Method Contd.

- Equate first and second moment of two log-normal distributions:

1. $\sum_{i=1}^{n} \frac{1}{n} e^{m_{X_i} + \frac{\sigma_{X_i}^2}{2}} = e^{m_y + \frac{\sigma_y^2}{2}}$ (1st moment)

2. $\frac{1}{n^2}\left(\sum_{i=1}^{n} e^{2m_{X_i} + 2\sigma_{X_i}^2} + 2\sum_{i=1}^{n-1}\sum_{j=i+1}^{n} e^{m_{X_i}+m_{X_j}} e^{\frac{\sigma_{X_i}^2 + \sigma_{X_j}^2 + 2r_{ij}\sigma_{X_i}\sigma_{X_j}}{2}}\right) = e^{2m_y + 2\sigma_y^2}$ (2nd moment)

- Solve for m_y and σ_y:

1. $m_y = m_X + \frac{1}{2}\Delta$ and 2. $\sigma_y^2 = \sigma_X^2 - \Delta$

where $\Delta = \sigma_X^2 - \ln\left(\frac{e^{\sigma_X^2} + (n-1)\cdot e^{r\cdot\sigma_X^2}}{n}\right)$

Proposed Leakage Estimation Technique

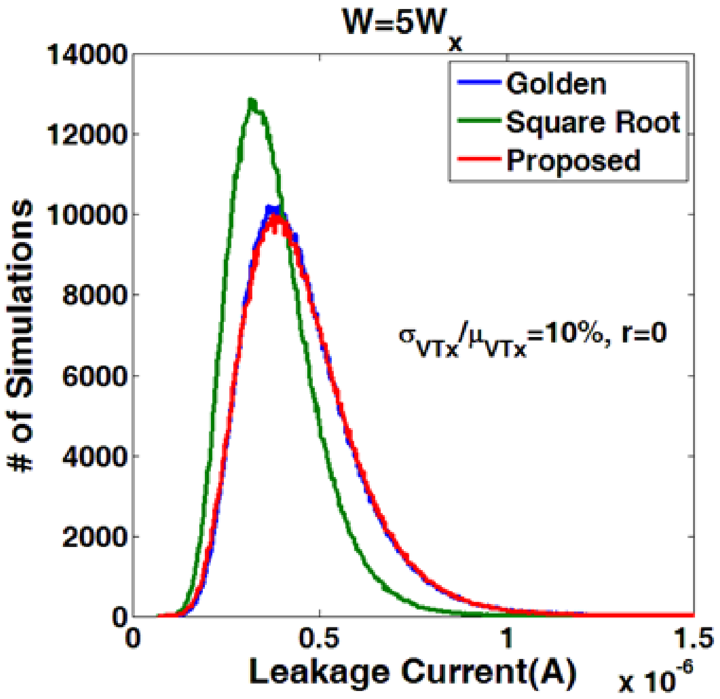
$$\mu_{V_{Ty}} = \mu_{V_{Tx}} - \frac{1}{2}\Delta/K_2$$

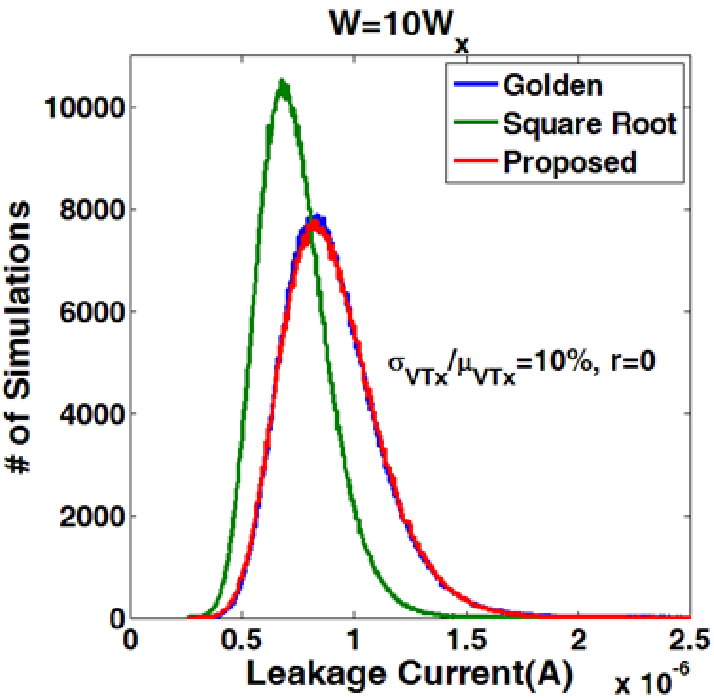
$$\sigma^2_{V_{Ty}} = \sigma^2_{V_{Tx}} - \Delta/{K_2}^2 \qquad (\Delta \geq 0)$$

Where $\Delta = {K_2}^2\sigma^2_{V_{Tx}} - \ln\left(\frac{e^{{K_2}^2\sigma^2_{V_{Tx}}} + (n-1)\cdot e^{r{K_2}^2\sigma^2_{V_{Tx}}}}{n}\right) \geq 0$

- **Based on Wilkinson’s approach of moment matching of log-normally distributed random variables**
- **Takes spatial correlation between reference devices into account**
- **Matches golden leakage distribution almost accurately**

Monte-Carlo Simulation Results (Different Device Widths)

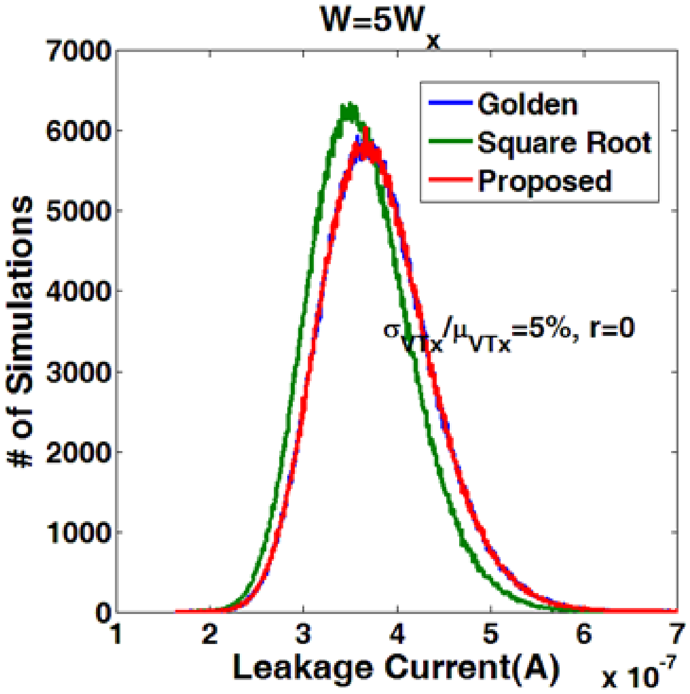


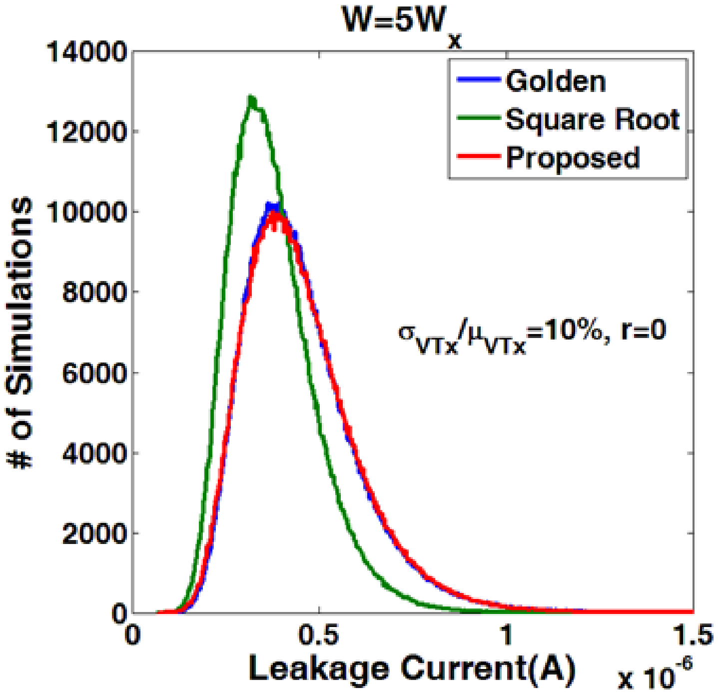


W=5W$_x$, σ_{VTx}/μ_{VTx}=10%, r=0		
	Square Root	Proposed
3σ error in leakage	22.21%	0.99%
6σ error in leakage	31.52%	10.91%

W=10W$_x$, σ_{VTx}/μ_{VTx}=10%, r=0		
	Square Root	Proposed
3σ error in leakage	23.58%	1.11%
6σ error in leakage	30.47%	5.98%

Monte-Carlo Simulation Results (Different V_T Variations)

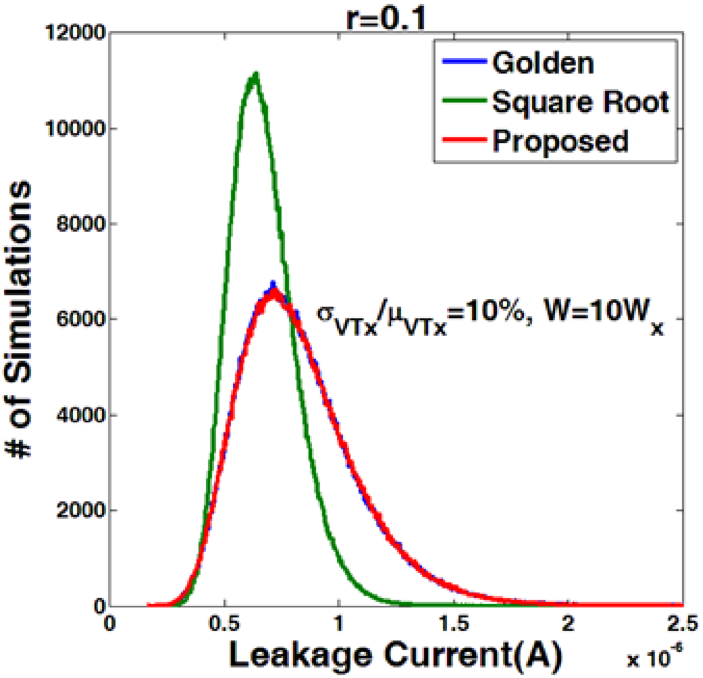


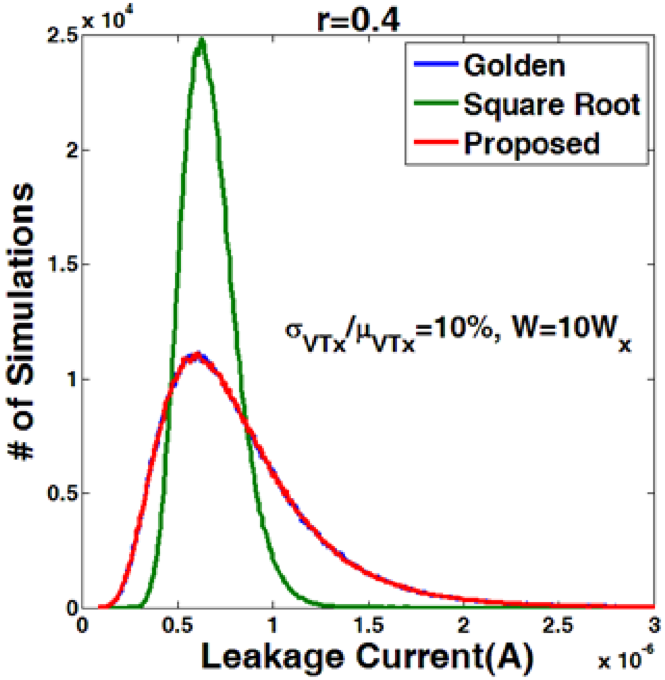


W=5W$_X$, σ_{VTx}/μ_{VTx}=5%, r=0		
	Square Root	**Proposed**
3σ error in leakage	5.36%	0.09%
6σ error in leakage	6.50%	1.66%

W=5W$_X$, σ_{VTx}/μ_{VTx}=10%, r=0		
	Square Root	**Proposed**
3σ error in leakage	22.21%	0.99%
6σ error in leakage	31.52%	10.91%

Monte-Carlo Simulation Results (Different Correlation Coefficients)

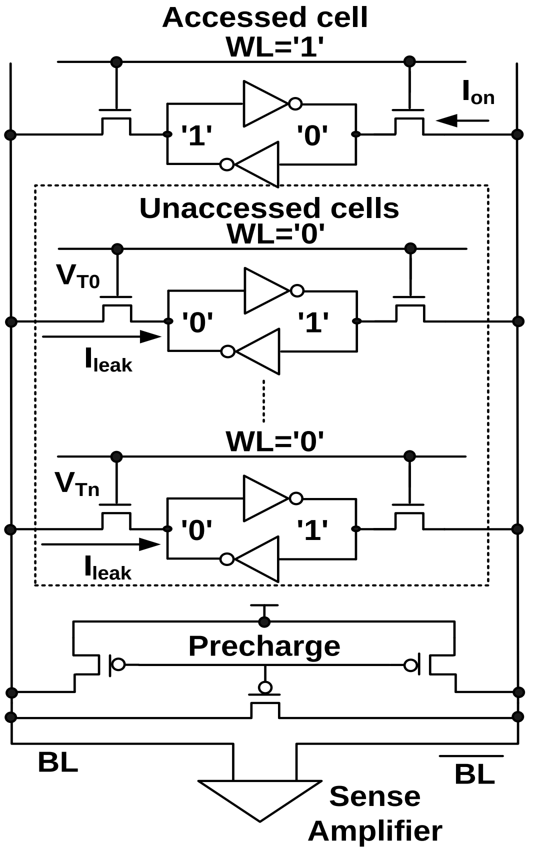


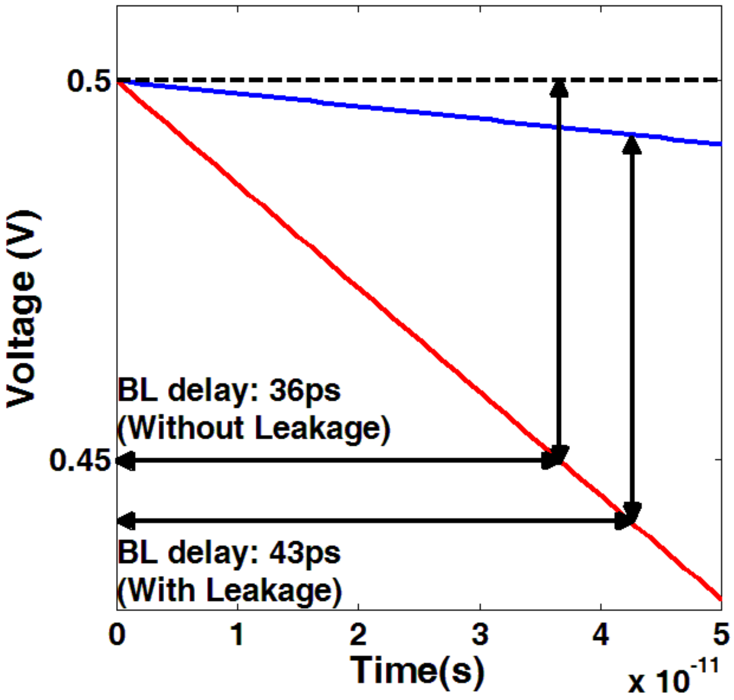


W=10W_X, σ_{VTx}/μ_{VTx}=10%, r=0.1		
	Square Root	**Proposed**
3σ error in leakage	33.61%	0.49%
6σ error in leakage	42.58%	2.37%

W=10W_X, σ_{VTx}/μ_{VTx}=10%, r=0.4		
	Square Root	**Proposed**
3σ error in leakage	50.58%	0.59%
6σ error in leakage	64.60%	0.30%

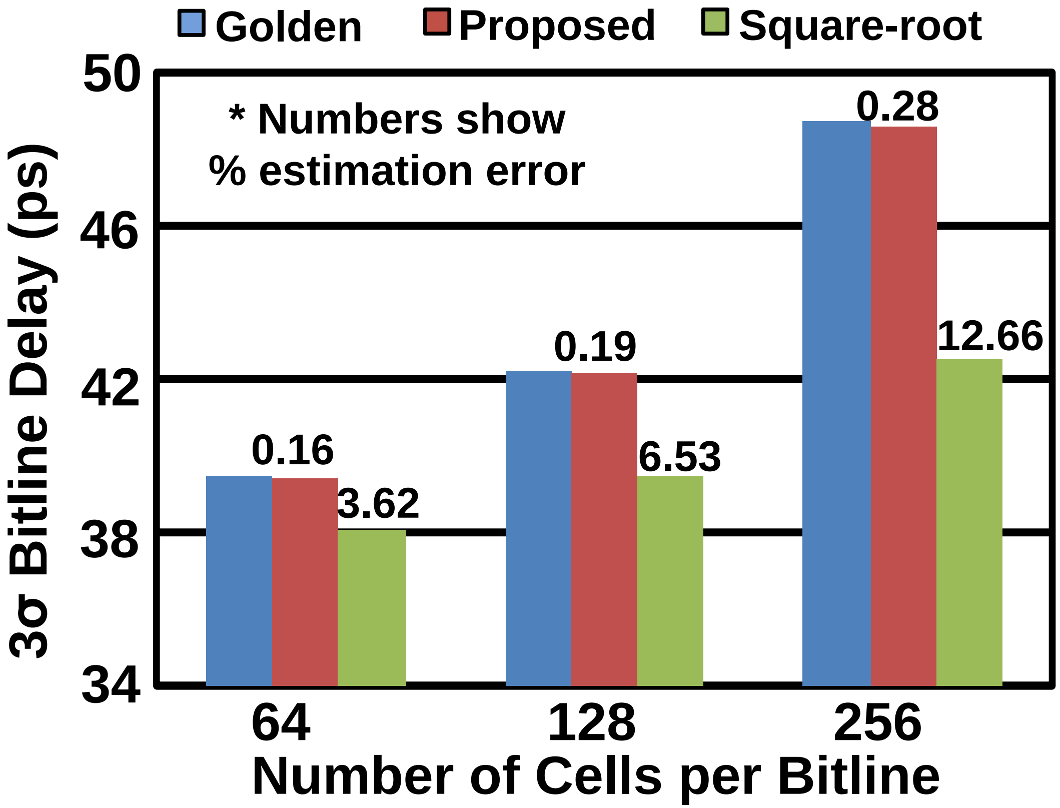
Circuit Example: SRAM Bitline Delay





- SRAM bitline read delay increases due to leakage current of unaccessed cells
- Worst case sensing delay: accessed cell stores a ‘1’ and all other cells store ‘0’

SRAM Bitline Delay Contd.



- For bitline delay modeling Monte Carlo simulations were performed assuming $\sigma_{VT}/\mu_{VT}=0.1$
- Proposed method shows less than 1% error in 3σ bitline delay estimation

Conclusions

- **Devices with steep sub-threshold slope are vulnerable to leakage variation due to random V_T shift**

- **Wilkinson’s approach estimate leakage variation in steep SS devices with high accuracy**

- **Monte Carlo simulations shows less than 11% error in estimating 6σ leakage current**

- **Worst-case error in 3σ SRAM bitline delay estimation using our model is less than 0.5%.**