

# A Comparative Study of Single-Poly Embedded Flash Memory Disturbance, Program/Erase Speed, Endurance, and Retention Characteristic

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**Abstract**—Single-poly embedded flash (eFlash) memory is a unique category of embedded nonvolatile memory (eNVM) that can be built in a generic logic technology. Several single-poly eFlash cells have been proposed for cost-effective moderate density eNVM applications. However, the optimal cell configuration of single-poly eFlash is still under debate. In this paper, we compared various single-poly eFlash memory structures in terms of disturbance, program/erase speed, endurance, and retention characteristic based on simulated and experimental data from two eFlash test chips fabricated in a generic 65-nm logic process using standard 2.5 V I/O transistors with 5-nm tunnel oxide. We conclude that a 5T eFlash cell structure combining a pMOS coupling device, an NCAP tunneling device, and an nMOS read/program device with two additional pass transistors to support self-boosting is the most attractive option for logic-compatible eNVMs.

**Index Terms**—Embedded flash (eFlash) memory, embedded nonvolatile memory (eNVM), single-poly eFlash.

## I. INTRODUCTION

EMBEDDED flash (eFlash) memory technology has been adopted in a wide range of system-on-chip and microcontroller applications [1]–[12]. Traditional dual-poly [2] and split-gate [3], [4] eFlash technologies are optimized for high-density nonvolatile code and data storage applications. The former employs a floating gate (FG) device while the latter utilizes charge trap material for achieving nonvolatile storage. These special memory cell devices, along with the high-voltage (e.g., > 14 V) transistors required for the program and erase operation, incur considerable process overhead when compared with a standard logic process. Single-poly eFlash [5]–[12] on the other hand can enable nonvolatile memories with no such process overhead, as it can be implemented using discrete I/O devices readily available in both mature and leading-edge logic technologies. Typically, leading edge system-on-chip platform technologies do not provide a multiple-time programmable embedded nonvolatile

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TABLE I  
LOGIC COMPATIBLE NVM OPTIONS

Logic Compatible Embedded NVM	2T Anti-Fuse [14]	NOVeA [5]	PND-Flash [6]	C-Flash [8]	NeoEE [9]	5T eFlash [10, 11]
Logic Process	32nm	0.13 $\mu$ m	N. A.	0.18 $\mu$ m	65nm	65nm
Access / Cell Tr.	1.8V I/O TR (HKMG)	3.3V I/O TR	3.3V I/O TR	3.3V I/O TR	2.5V I/O TR	2.5V I/O TR
Writing Method	Gate Oxide Breakdown	Electron FN Tunneling	Electron FN Tunneling	Electron FN Tunneling	Electron FN Tunneling	Electron FN Tunneling
Unsel. WL Disturb	No	No	No	Yes	Yes	No
Unit Cell Size	1.01 $\mu$ m <sup>2</sup>	700 $\mu$ m <sup>2</sup> (est.)	500 $\mu$ m <sup>2</sup>	72 $\mu$ m <sup>2</sup>	N. A.	8.62 $\mu$ m <sup>2</sup>
Capacity	1kb	2kb	5kb	256b	16kb	2kb

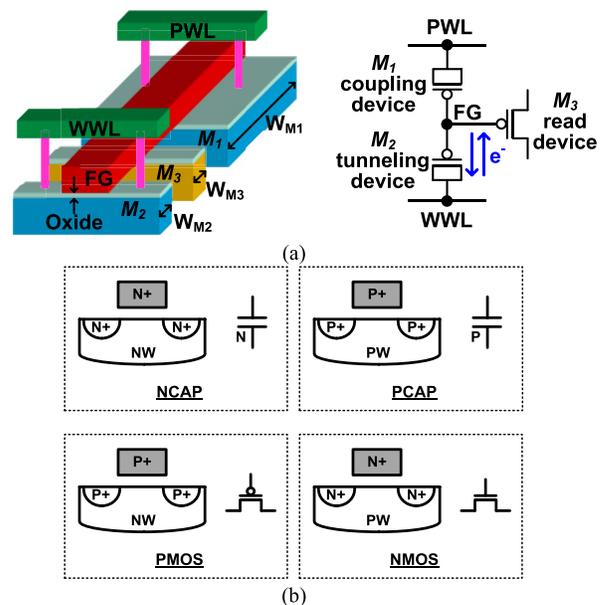


Fig. 1. (a) Bird's eye view and example schematic diagram of a single-poly eFlash memory cell core consisting of three standard I/O devices  $M_1$ – $M_3$ . (b) Cross section and circuit symbol of the four possible device configurations.

memory (eNVM) option. For example, advanced high- $k$  metal gate logic technologies [13], [14] have provided only a moderate density (i.e., few kilobit) one-time-programmable (OTP) memory option [14] using 1.8 or 3.3 V I/O devices. Single-poly eFlash, on the other hand, is expected to play a critical role in emerging postsilicon tuning applications, such as in adaptive techniques for mitigating circuit variability and reliability issues, memory repair schemes, and self-healing systems that require multiple-time-programmable eNVM. Table I compares various logic compatible eNVM options, including OTP and single-poly eFlash. The core structure of

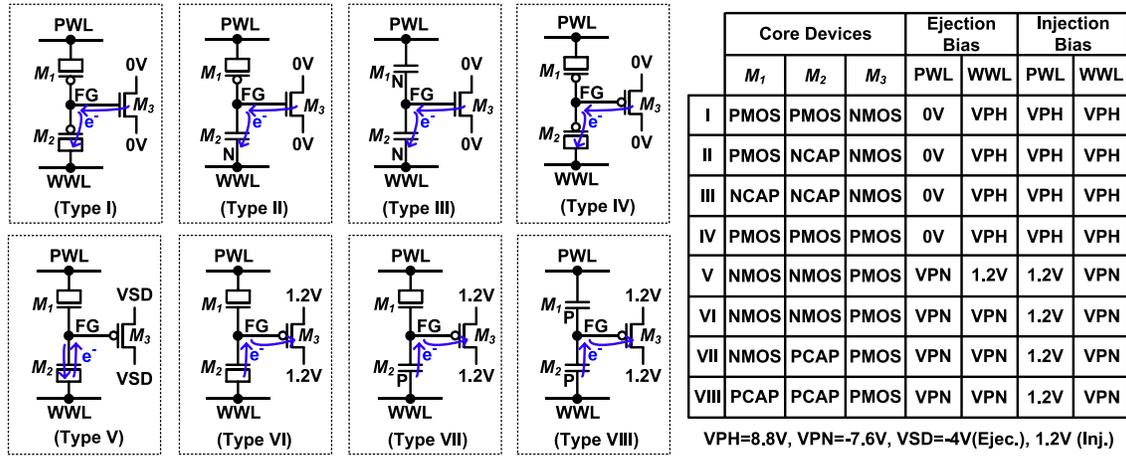


Fig. 2. Eight possible single-poly eFlash cell core configurations considered in this paper. In all types, the coupling device ( $M_1$ ) is large compared with the other two devices, and erase and program operations are performed via electron Fowler–Nordheim tunneling.

a single-poly eFlash cell typically comprises three standard I/O transistors, as shown in Fig. 1(a). Here,  $M_1$  is the coupling device,  $M_2$  is the tunneling device, and  $M_3$  is the read or read/program device depending on the bias condition. The FG node for nonvolatile charge storage is formed by connecting the transistors in a back-to-back fashion. Note that the coupling device  $M_1$  is large compared with the other two ( $M_2$  and  $M_3$ ) so as to maintain strong coupling between the control gate (i.e., body terminal of  $M_1$ ) and FG node. This ensures that the FG voltage closely follows the voltage applied to the coupling device, generating sufficient voltage across the dielectric of the tunneling device for efficient electron tunneling. For example, a boosted high voltage is applied to write wordline (WWL) while program wordline (PWL) is driven to 0 V during erase mode to remove electrons from the FG. On the other hand, a boost voltage is applied to PWL while WWL is driven to 0 V during program mode to inject electrons into the FG node. Depending on whether the cell is programmed or erased, the effective threshold voltage of the read device  $M_3$  changes. This can be simply read out by measuring the read current through  $M_3$  for given PWL and WWL bias conditions and comparing its value against a known reference. On the other hand, in a polygate CMOS technology, a device with an n-type gate typically has to be paired with an n-type junction. Similarly, a p-type gate is constrained to a p-type junction. However, the well can be either an n-type or a p-type, giving rise to four possible device configurations as shown in Fig. 1(b), namely, NCAP (n-type gate, n-type junction, n-type well), PCAP (p-type gate, p-type junction, p-type well), pMOS (p-type gate, p-type junction, n-type well), and nMOS (n-type gate, n-type junction, p-type well). So far, single-poly eFlash memories have adopted various device combinations by different groups [5]–[12]. For example, in [5], NCAP was used in the coupling ( $M_1$ ) and tunneling ( $M_2$ ) devices while pMOS was used in the read device ( $M_3$ ). In another design [6], pMOS, NCAP, and nMOS were used in the coupling ( $M_1$ ), erase ( $M_2$ ), and program/read ( $M_3$ ) devices, respectively, for the higher coupling ratios during program and erase operations. A work-function engineered n+ poly pMOS was used as the tunneling

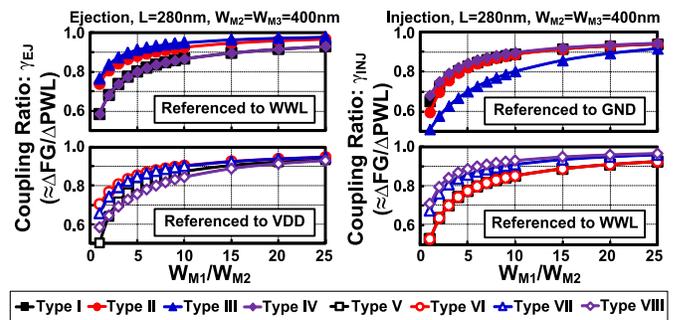


Fig. 3. Coupling ratios  $\gamma_{EJ}$  and  $\gamma_{INJ}$  for different width ratios ( $= W_{M1}/W_{M2}$ ).

device ( $M_2$ ) in [7] for higher electron ejection efficiency and better reliability. However, there has been practically no work that provides an in-depth comparison between the cells in terms of disturbance, program/erase speed, endurance, and retention. We address this issue by analyzing the simulated and experimental data to gain better insight into the optimal single-poly eFlash cell configuration.

The remainder of this paper is organized as follows. Section II investigates the control gate coupling strength based on the simulation results of different single-poly eFlash types and sizing. Section III compares disturbance, program/erase speed, endurance, and retention characteristic of the different single-poly eFlash cells based on measurement results from two test chips fabricated in a 65-nm low-power CMOS process. Finally, conclusions are drawn in Section IV.

## II. CONTROL GATE COUPLING STRENGTH

The eight possible cell core configurations considered for this paper, along with their bias conditions for electron ejection and injection operations, are shown in Fig. 2. The nominal supply voltage (VDD) is 1.2 V in the process used in this paper, and each single-poly eFlash cell is implemented using 2.5 V standard I/O devices with a 5-nm oxide thickness. The findings of this comparative study would be equally applicable to eFlash cells built using different I/O devices such as 3.3 V

TABLE II  
COMPARISON OF COUPLING RATIOS

Configuration	$V_{FG\_EJ}(V)^*$	$V_{FG\_INJ}(V)^*$	$\gamma_{EJ}$	$\gamma_{INJ}$
Type I	1.3	7.7	0.85	0.87
Type II	0.8	7.6	0.91	0.87
Type III	0.5	6.8	0.94	0.77
Type IV	1.3	7.8	0.85	0.88
Type V	-6.3	-0.3	0.85	0.83
Type VI	-6.6	-0.3	0.89	0.83
Type VII	-6.6	0.3	0.89	0.89
Type VIII	-6.0	0.5	0.82	0.92

\*Assumes no initial FG charge and width ratio of 8

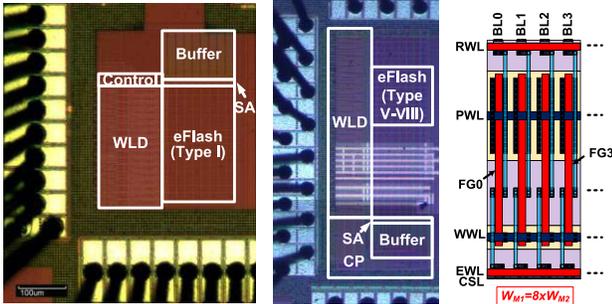


Fig. 4. Die microphotographs of the two single-poly eFlash test chips for this paper fabricated in a 65-nm standard logic process. Layout of a 5T eFlash array with a width ratio of 8 is shown on the right [10]–[12].

transistors [13]. The program voltages (i.e., 8.8 and  $-7.6$  V) are determined by the maximum voltage that can be supplied by the high-voltage circuitry [10], [12]. Fig. 3 shows the simulated control gate coupling ratios of the eight cell core configurations for different width ratios ( $= W_{M1}/W_{M2}$ ) subject to the bias conditions specified in Fig. 2. The coupling ratio for electron ejection (denoted as  $\gamma_{EJ}$ ) and injection (denoted as  $\gamma_{INJ}$ ) are defined as  $\Delta FG/\Delta PWL$ , assuming no initial charge on the FG and a negligible interpoly coupling effect in the eFlash array [15]. These ratios were calculated from the simulated FG node voltage (i.e.,  $V_{FG\_EJ}$  and  $V_{FG\_INJ}$ ) and bias voltages applied to the cells. For fast electron ejection and injection, higher  $\gamma_{EJ}$  and  $\gamma_{INJ}$  are preferred. The ejection and injection coupling ratios can be slightly different due to several reasons. For instance, the strong inversion capacitance of pMOS  $M_2$  device in Type I could reduce the coupling from PWL during electron ejection, whereas the same physical capacitance can increase the coupling from PWL during electron injection. The simulation results show that Type II and VII configurations using a nondepletion mode coupling device  $M_1$  and depletion mode tunneling device  $M_2$  provide high coupling ratios for both electron ejection and injection operations. A higher coupling ratio can be obtained by upsizing  $W_{M1}$ , too. However, this will directly impact the bit cell area. A summary of the simulation results for different configurations with a width ratio of 8 is given in Table II.

### III. DISTURBANCE, PROGRAM/ERASE SPEED, ENDURANCE, AND RETENTION CHARACTERISTIC

Two test chips were fabricated in a 65-nm standard logic process for this paper [10]–[12]. The die microphotographs

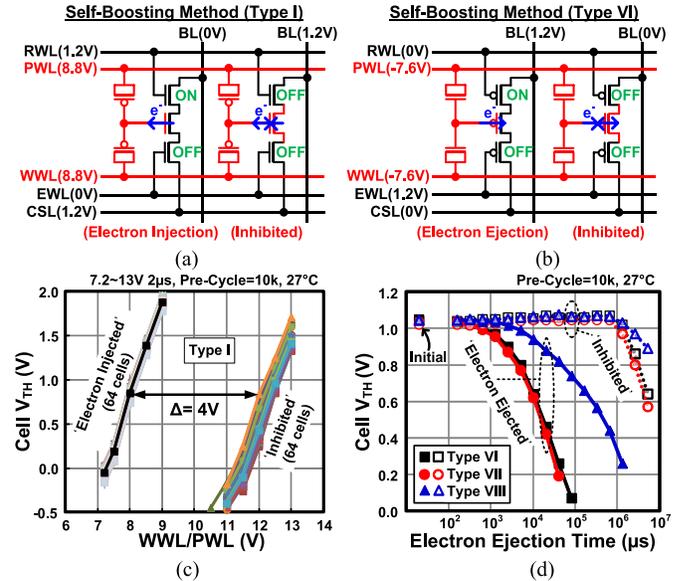


Fig. 5. (a) and (b) Self-boosting bias conditions of 5T eFlash. (c) and (d) Measured disturbance characteristic.

and array layout are shown in Fig. 4. The unit cell area for Types I–III and V–VIII configurations is identical at  $8.62 \mu\text{m}^2$ , whereas that for Type IV configuration is larger because of the high-voltage column circuits required for proper operation. Due to the short design time and limited die area, Type II–IV configurations were not implemented in this paper. Program/erase speed and endurance/retention characteristic of 5T eFlash having Type I configuration were already discussed with the detailed description of the peripheral circuits, such as the WL driver, charge pump (CP), and sense amplifier in [10]. In this paper, we focus comparing the fundamental characteristics of various eFlash cells starting with the disturbance behavior. As we do not have the measured data for the Type II–IV configurations, the results from the Type V–VIII configurations were used to theoretically predict the characteristics of the Type II–IV configurations.

#### A. Disturbance Characteristic of Single-Poly eFlash Cells

5T eFlash cells having Type I–III and VI–VIII configurations can be selectively program-inhibited without a boosted BL voltage via the self-boosting method described in [16] as shown in Fig. 5. Type IV and V configurations on the other hand, do not support self-boosting inhibition since the Type IV operates in an accumulation mode during program operation while the Type V programs or erases the entire WL regardless of the VSD level (Fig. 2). For Type I–III and VI–VIII, two additional devices are connected to the program device ( $M_3$ ), forming a 5T eFlash cell structure and thereby allowing both junctions of the program device to float for the inhibited cells while the other cells sharing the same WL are being programmed. For the inhibited cells, the channel voltages of program device need to be boosted sufficiently while the leakage currents from/to the boosted channel should be suppressed to minimize disturbance of these cells [17]. A longer channel pass transistor connecting the program

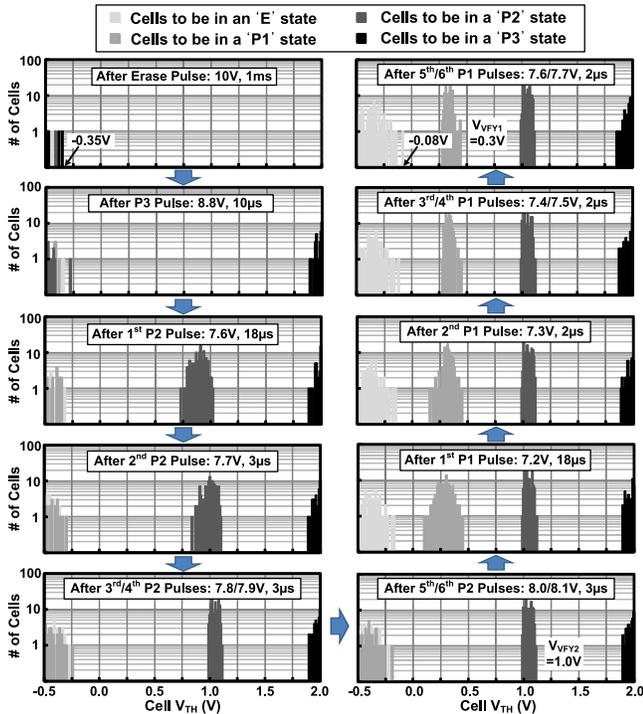


Fig. 6. Multilevel programming result of Type I 5T eFlash cell.

device to BL and shorter program pulse width are preferred to maintain the boosted channel voltages high enough during the inhibition mode. The measured data in Fig. 5(c) shows a voltage margin of 4 V between the electron injected and inhibited cells for 10 k precycled cells. A negligible cell  $V_{TH}$  disturbance up to a  $\sim 1$ s program pulse was verified in Fig. 5(d). The disturbance effect of the erased state cells during multilevel cell programming is shown in Fig. 6 for the Type I 5T eFlash cells. Here, the entire flash array was first precycled 10-k times, then erased, and then programmed in the following order: 1) P3; 2) P2; and 3) P1. Measured data shows that the erased cell  $V_{TH}$  tail is shifted by  $\sim 0.27$  V after the whole programming sequence has been applied.

The setup and measurement data from a wordline voltage-induced degradation test are shown in Fig. 7. Here, a bias voltage VSTR was applied to both PWL and WWL to measure the degradation time it takes for the erased cell  $V_{TH}$  tail to reach the sensing failure point under a dc bias condition. The bias voltage levels used in this experiment were 3.2, 4, 5, and 6 V. The measured results in Fig. 7(c) shows that the cell  $V_{TH}$  shift becomes significantly worse for VSTR > 5 V causing the degradation time to eventually drop <10 ms for a precycle count of 10 k. The voltage stress condition used in this experiment corresponds to that of unselected WL cells without self-boosting capability which means that those cells are exposed to a boosted BL voltage during write operation [8], [9]. On the other hand, 5T cells that support self-boosting are not affected by any voltage stress when the WL is unselected [10]. These results confirm the effectiveness and necessity of the self-boosting technique in an eFlash memory. Although Types I–III and Types VI–VIII all support self-boosting opera-

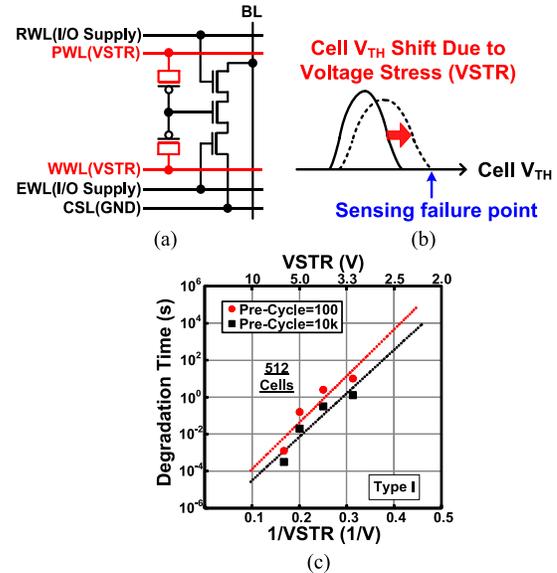


Fig. 7. (a) Bias condition for measuring wordline voltage-induced degradation. (b) Cell  $V_{TH}$  shift under voltage stress. (c) Measured degradation time with the sensing failure point of 0 V at 25 °C.

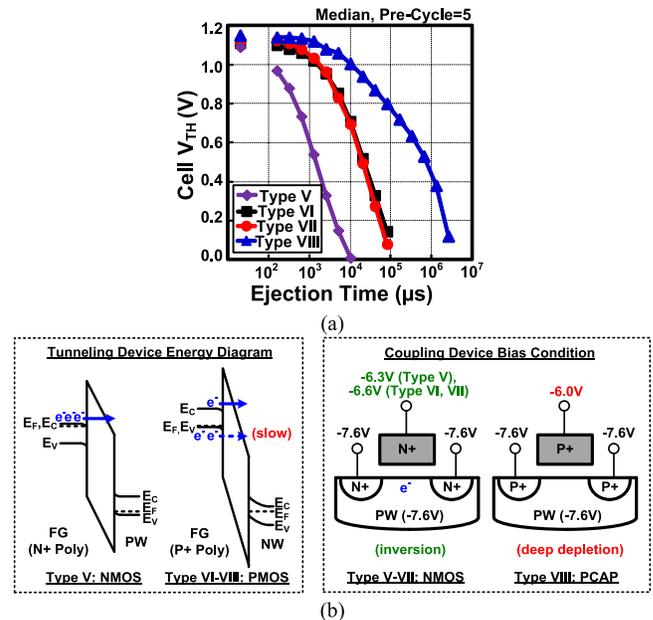


Fig. 8. (a) Measured electron ejection speed of various eFlash memory cells. (b) Energy band diagram of the tunneling device and bias condition of the coupling device that explain the fast ejection of Type V and slow ejection of Type VIII.

tion, Types I–III are preferred as they do not require a negative boosted supply, which can cause junction breakdown concerns in the high-voltage driver and CP circuits [12].

### B. Program and Erase Speed of Single-Poly eFlash Cells

The measured electron ejection speeds of the Type V–VIII cells are shown in Fig. 8 along with energy band diagrams of the tunneling device and cross sections of the coupling device. The bias conditions described in Fig. 2 were used for testing the electron ejection speed. Results show that the

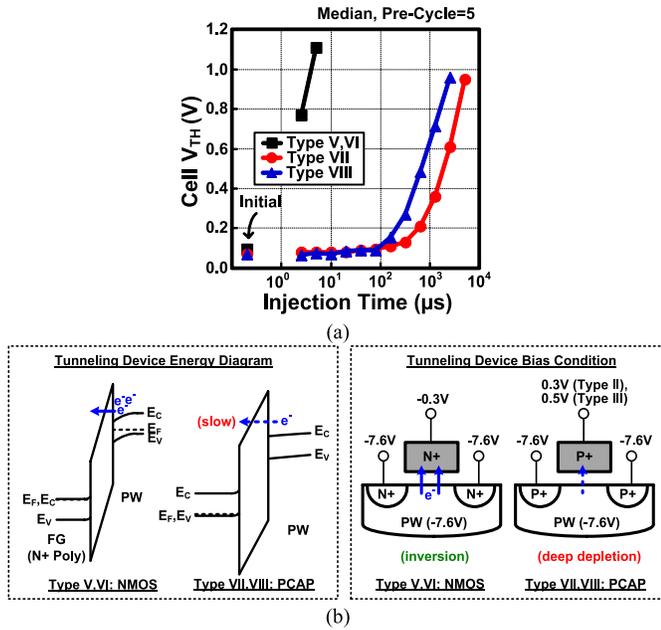


Fig. 9. (a) Measured electron injection speed of various types of eFlash memory cells. (b) Energy band diagram and bias condition of the tunneling device that explain the fast electron injection of Type V and VI configurations.

Type V cell has the fastest electron ejection speed which can be attributed to the nMOS tunneling device having more conduction band electrons compared with the pMOS tunneling devices used in Types VI–VIII. This is visualized in the left of Fig. 8(b). Note that the conduction band electron tunneling in Type V is roughly an order-of-magnitude faster than the valence band electron tunneling in Types VI–VIII, though the oxide field applied to the tunneling device is higher in the latter [18]. On the other hand, the Type VIII cell shows the slowest electron ejection speed. This is because the PCAP coupling device in this cell operates in a deep depletion mode during electron ejection, reducing the cell coupling ratio. In contrast, the nMOS coupling device in Types V–VII operates in an inversion mode, offering a stronger coupling effect as shown on the right in Fig. 8(b). Similarly, Type II and III cells utilizing n-type gate tunneling device are expected to have a faster ejection speed due to the higher number of conduction band electrons compared with Types I and IV. In fact, the faster electron ejection speed of the Type II cell compared with Type I was previously theoretically predicted by other groups [6]. Similarly, the higher electron ejection current of an n+ poly FG compared with a p+ poly FG was reported in [7], which agrees with our measurement results in Fig. 8.

The measured electron injection speeds of the Type V–VIII cell are shown in Fig. 9 along with the energy band diagrams and device cross sections of the tunneling device. Again, we apply the bias conditions mentioned in Fig. 2 for this experiment. According to our test data and analysis, the Type V and VI cells show the fastest electron injection speed because the nMOS tunneling device operates in a strong inversion mode. This is in contrast to Types VII and VIII, where a PCAP in deep depletion mode is used as the tunneling

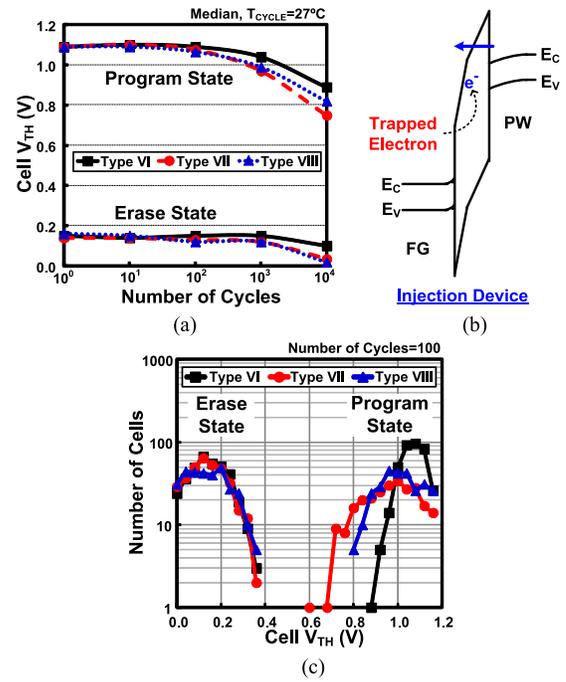


Fig. 10. (a) Measured endurance characteristics of Types VI–VIII. (b) Energy band diagram of the tunneling device with a trapped electron in oxide after cycling. (c) Measured cell  $V_{TH}$  distributions of Types VI, VII, and VIII after 100 P/E cycles.

device, which has fewer electrons in the conduction band available for tunneling as shown in Fig. 9(b). On the other hand, Type VIII is faster than Type VII because the coupling device of the former type quickly falls into the accumulation mode, producing a higher coupling effect from the body of the coupling device to the FG. This in turn generates a higher oxide field in the electron injection device. It is important to note, however, that the marginal improvement in electron injection speed due to the depletion mode coupling device is outweighed by the significant improvement of the electron ejection speed by the nondepletion mode coupling device as shown in Fig. 8(a). Among Type I–IV cells, Type III cell is expected to have a slow injection speed due to the depletion of coupling device. This is in contrast to Type I, II, and IV cells, where a strong inversion capacitance is formed during electron injection.

### C. Endurance and Retention Characteristics

Fig. 10(a) shows the measured endurance characteristic of Types VI–VIII. The negative cell  $V_{TH}$  shift after a large number of program and erase cycles can be explained by the trapped electron in the oxide of the electron injection device ( $M_2$ ) under stress [19] affecting the shape of the tunnel barrier as shown in Fig. 10(b), which in turn slows down the electron injection speed. The Type VI cell shows the least amount of cell  $V_{TH}$  degradation. The measured cell  $V_{TH}$  distributions after 100 P/E cycles in Fig. 10(c) indicate that the  $V_{TH}$  variation in program state (i.e., electron injected into FG) worsens for Type VII and VIII cells, further reducing the sensing margin. The larger variation can be attributed to

TABLE III  
COMPARISON BETWEEN DIFFERENT SINGLE-POLY eFLASH CELL CORE CONFIGURATIONS

Items	Coupling Ratios	Disturbance	Ejection Performance	Injection Performance	Intrinsic Retention	
Result	Fig. 3	Figs. 5-7	Fig. 8	Figs. 9-10	Fig. 11	
Preferred Configuration (Criteria)	$M_1$ : non-depletion $M_2$ : depletion ( $\gamma_{EJ}, \gamma_{INJ} > 0.87$ ?)	Support self-boosting effectively?	Ejection device: n-type poly ( $T_{EJ} < 10\text{ms}$ ?)	$M_1$ and inj. dev.: non-depletion ( $T_{INJ} < 10\mu\text{s}$ ?)	$M_1$ : p-type gate	
Cell Configurations	Type I ( $M_1$ : PMOS, $M_2$ : PMOS, $M_3$ : NMOS)	No	Yes	No	Yes	Yes
	Type II ( $M_1$ : PMOS, $M_2$ : NCAP, $M_3$ : NMOS)	Yes	Yes	Yes (Estimated)	Yes (Estimated)	Yes (Estimated)
	Type III ( $M_1$ : NCAP, $M_2$ : NCAP, $M_3$ : NMOS)	No	Yes	Yes (Estimated)	No (Estimated)	No (Estimated)
	Type IV ( $M_1$ : PMOS, $M_2$ : PMOS, $M_3$ : PMOS)	No	No	No (Estimated)	Yes (Estimated)	Yes (Estimated)
	Type V ( $M_1$ : NMOS, $M_2$ : NMOS, $M_3$ : PMOS)	No	No	Yes	Yes	No
	Type VI ( $M_1$ : NMOS, $M_2$ : NMOS, $M_3$ : PMOS)	No	Yes	No	Yes	No
	Type VII ( $M_1$ : NMOS, $M_2$ : PCAP, $M_3$ : PMOS)	Yes	Yes	No	No	No
	Type VIII ( $M_1$ : PCAP, $M_2$ : PCAP, $M_3$ : PMOS)	No	Yes	No	No	Yes

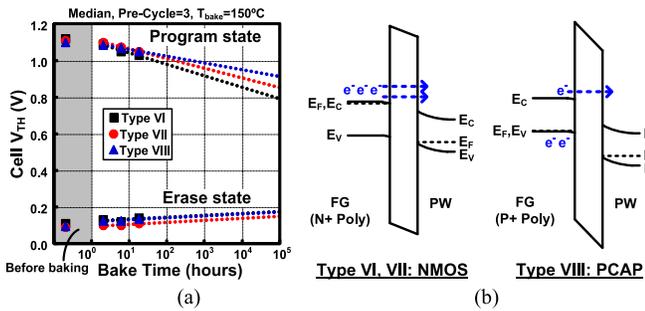


Fig. 11. (a) Measured retention results of Type VI–VIII cells. (b) Energy band diagram of nMOS (for Types VI and VII) and PCAP (for Type VIII) coupling devices that explain the slower charge loss of the latter type with a p-type gate coupling device.

the difference of the minority carrier generation rate between cells, as a PCAP electron injection device operates in a deep depletion mode where the depletion width varies depending on the doping concentration of each cell. At the same time, holes in the channel of the read device ( $M_3$ ) can be activated and trapped into the gate oxide of the same read device during electron ejection for Types VI–VIII, causing the  $V_{TH}$  to shift in the negative direction as shown in Fig. 10(a). However, this so-called anode hole injection theory [20] cannot explain the larger variation occurring in program state of Type VII and VIII cells.

Fig. 11 shows the measured retention results of Type VI–VIII cells. A small precycle count of three was used to match the initial cell  $V_{TH}$  between the different cell types without causing damage to the gate oxide. Results show a smaller cell  $V_{TH}$  shift for Type VIII compared with Types VI and VII, which can be explained by the superior intrinsic retention characteristic of cells containing a coupling device having a p-type gate. The Fermi level in the p-type gate is close to the valence band edge, which in turn reduces the number of conduction band electrons participating in the charge loss process [18]. According to this insight, we can conclude that the Type I, II, IV, and VIII cells containing a p-type gate coupling device will have a significantly lower gate leakage than the other types and hence are preferred for longer retention times.

## IV. CONCLUSION

Single-poly eFlash can be built using standard I/O devices readily available in a generic logic process, making it an attractive eNVM option for moderate density applications where a dedicated eFlash process is not available. In this paper, we present a comparative study of various single-poly eFlash cells. The results summarized in Table III show that the Type II 5T eFlash cell composed of a pMOS coupling device ( $M_1$ ), an NCAP tunneling (or electron ejection) device ( $M_2$ ), and an nMOS read/program device ( $M_3$ ) with two additional pass transistors to support self-boosting is the preferred choice among the eight possible configurations, when coupling ratios, disturbance, performance, and retention characteristics are all considered.

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