This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TDMR.2014.2308140, IEEE Transactions on Device and Materials Reliability

Aging Statistics based on Trapping/Detrapping: Compact Modeling and Silicon Validation

Ketul B. Sutaria, *Student Member, IEEE*, Jyothi B. Velamala, *Student Member, IEEE,* Chris Kim, *Senior Member, IEEE,* Takashi Sato, *Member, IEEE,* Yu Cao, *Senior Member, IEEE*

***Abstract*— Design for reliability is an increasingly important design step at advanced technology nodes. Aggressive scaling has brought forth reliability issues, such as Negative Bias Temperature Instability (NBTI). The aging process due to NBTI exhibits a significant amount of variability for a single device as well as for multiple devices. As a result, long-term reliability prediction from short-term stress measurement becomes dramatically challenging. With increasing reliability concerns, accurate statistical aging prediction is essential in order to develop robust guard banding and protection strategies during the design stage. To develop an accurate long-term prediction method under variations, this work first collects statistical device data from a 65nm test chip with a resolution of 0.2mV in threshold voltage (V_{th}) measurement. Comparing aging prediction from short-term stress data (<20k second) with direct long-term measurement (up to 200k second), we conclude that (1) the aging in a PMOS device follows logarithmic time dependence, rather than conventional power law; (2) traditional t^n model overestimates the aging rate and the variance for long-term behavior; (3) Trapping/De-trapping (TD) based *log(t)* model correctly captures the aging variability due to the randomness in number of initial available traps, and accurately predicts the mean and the variance of V_{th} shift. These results guide the development of a new aging model for robust long-term lifetime prediction. Furthermore, effectiveness of the new *log(t)* model is evaluated by the statistical aging data from 65nm ring oscillators. Compared to previous models, the new *log(t)* model based on TD theory well captures the mean and the variance of at the circuit level.**

***Index Terms*—Bias Temperature Instability, Reliability Modeling, Statistical Variations, Trapping/De-trapping.**

I. Introduction

Technology scaling has enabled integration of more transistors on a single chip, helping higher speed and lower power designs. Although beneficial, disproportional scaling of transistors and electric field has led to multiple reliability issues [1]-[4]. Bias Temperature Instability (BTI), Channel Hot Carrier (CHC) and dielectric breakdown are predominant aging mechanisms affecting circuit performance over the lifetime. Both NBTI and CHC result in the increase in absolute threshold voltage (V_{th}) of a device and reduce the drain current, thereby degrading the circuit speed and data stability at longer stress time [5]. With gate dielectric thickness close to 1nm, the shift in threshold voltage (ΔV_{th}) of a PMOS transistor due to NBTI is dominant because of increased vertical field. In digital circuits where transistors are more in the standby mode rather than in saturation, NBTI is indeed the limiting factor for circuit lifetime as compared to CHC. Accurate prediction of the aging rate during early design stage is crucial for guard banding. However, aging process under NBTI has shown a significant amount of variations. Stochastic V_{th} shift under NBTI complicates guard banding strategies in the long term. Hence, it is critical to understand, simulate and mitigate the NBTI effect in early design stages to ensure reliable circuit operation for desired lifetime.

NBTI mechanism is often explained by the classical Reaction Diffusion (R-D) model [2]-[5]. According to R-D theory, NBTI is caused by interfacial charge generation and diffusion due to Si-H bond breaking. Based on this theory, threshold shift follows power law relation with stress time, where the time exponent (n) is approximately at 0.16 and it should be independent on process and operation parameters. However,

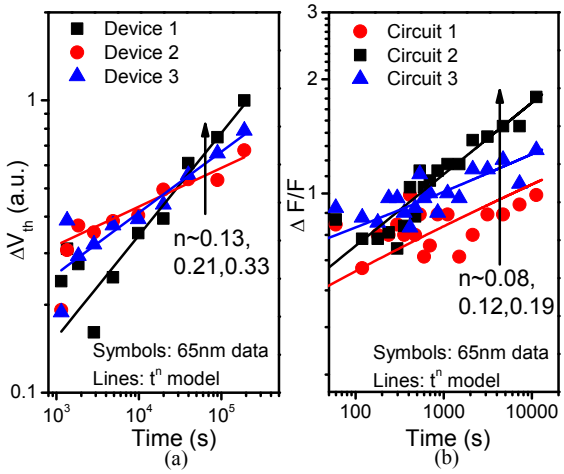

Fig. 1. (a) Time exponent of the t^n model extracted from 65nm silicon data (V_{gs} = -1.8V) (b) Time exponent extracted from 65nm bulk CMOS ring oscillators (RO) (V_{DD} = 1.8V).

Manuscript received January 10, 2013; accepted February 2, 2014.

K. B. Sutaria, J. B. Velamala and Y. Cao are with the Electrical Engineering Department, Arizona State University, Tempe, AZ 85004 USA (e-mail: kbsutari@asu.edu; jvelamal@asu.edu; ycao@asu.edu).

T. Sato is with the Kyoto University, School of Informatics, Kyoto, 606-8501 Japan (e-mail: takashi@i.kyoto-u.ac.jp).

C. Kim is with the Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN 55455 USA (e-mail: chriskim@umn.edu).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TDMR.2014.2308140, IEEE Transactions on Device and Materials Reliability

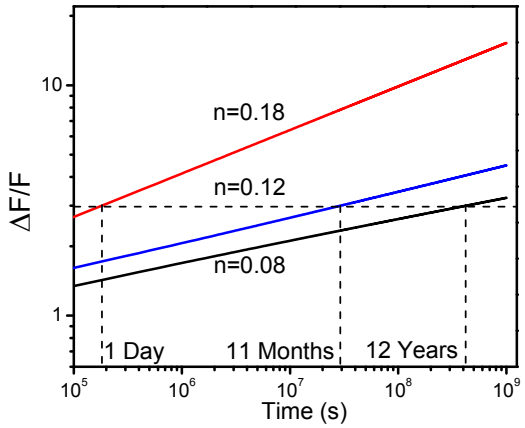

Fig. 2. Significant variations of lifetime prediction due to variation in time exponent (n) for a 65nm ring oscillator (RO) assuming ~12% frequency shift at the end of the lifetime.

Fig. 1(a) illustrates that even from the same process and under the same stress conditions, the values of n from three different PMOS devices do not match with each other. Similarly, ring oscillators of the same area and stressed at the same voltage exhibits different shift in frequency as described in Fig. 1(b). ΔV_{th} prediction from R-D based t^n model is very sensitive to the value of time exponent due to the mathematical relation. Hence, even a small change in n leads to dramatic difference in long term prediction of circuit lifetime [6]-[10]. As demonstrated in Fig. 2, lifetime prediction for a ring oscillator circuit using t^n model may vary from a day to a few years. Such wide variation in lifetime prediction may result in infeasible guard banding strategies for a resilient design.

Meanwhile, with improvement in measurement technologies, evidence of charge Trapping/Detrapping (T-D) for PMOS degradation has been accumulating [6]-[10]. According to this theory, V_{th} of a device under BTI stress increases if a trap captures the channel carrier; the trap may emit the carrier if the stress is released. To highlight T-D process, a single 65nm device is dynamically stressed under a sequence of 1.8V and 0V, with 36 stress and recovery cycles [9]. The device is allowed sufficient recovery time before it is stressed again. Fig. 3(a) for V_{th} degradation of the same device clearly shows the stochastic nature caused by random charge trapping/de-trapping. V_{th} at the end of stress time [Fig. 3(b)] follows a normal distribution, showing no history dependence of previous recovery. The degradation during the stress phase instantaneously recovers when the voltage is tuned to 0V, showing the process of de-trapping in BTI. The recovery cycles in Fig. 3(c) clearly exhibits several discrete levels and time constants, with almost no permanent component of previous stressing, further confirming the dominance of fast T-D in BTI for this 65nm technology. T-D based BTI model follows logarithmic relation with time.

Both T-D and R-D mechanisms successfully explain the threshold voltage shift due to NBTI depending on fabrication technology. There are many publications indicating V_{th} shift is a combination of fast T-D and slow R-D mechanism [11]-[14]. In order to address the challenges of statistical aging and to

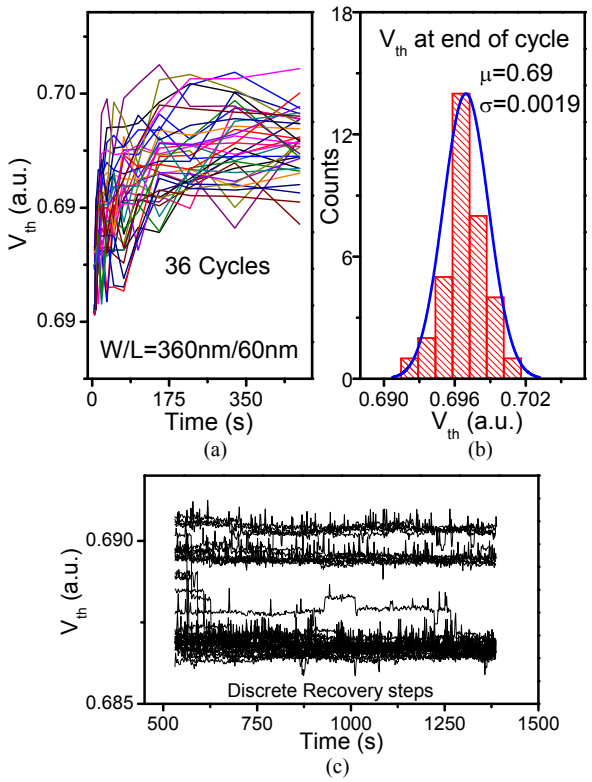

Fig. 3. (a) Multiple stress (V_{gs} = -1.8V) cycles on the same device after sufficient recovery time; (b) Randomness at the end of the stress phase follows a normal distribution; (c) Discrete recovery steps in the amplitude and time constants without any history effect, implying the role of discrete charge trapping/de-trapping that is stochastic in nature.

improve the accuracy of reliable lifetime prediction, this work investigates the variability in aging using 65nm silicon data. We propose a robust prediction method by understanding the underlying physics based on Trapping/De-trapping (T-D) mechanism [15]. The new set of compact aging models enhances the robustness by accurately predicting both the mean and variance for long-term aging. Moreover, this work analyzes 65nm RO data to identify and explain the stochastic role of charge trapping/detrapping at the circuit level. The main contributions of this work include:

1. T-D based *log(t)* model for aging prediction, suggesting logarithmic dependence on time, rather than the conventional power law expectation.

2. Statistical model evaluation shows that t^n model overestimates the aging and its variance leading to overestimate lifetime prediction at both device and circuit levels.

3. New *log(t)* model derived from trapping/de-trapping theory correctly predicts the aging variability due to the stochastic nature of the number of available traps.

4. Comprehensive validation of proposed aging models with statistical device and circuit aging data at 65nm.

The organization of the paper is as follows: Section II describes the test structure and measurement technique. Section III presents T-D based aging model, predicting logarithmic dependence on time and avoiding overly pessimistic lifetime prediction. Sections IV and V evaluate the new model with

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TDMR.2014.2308140, IEEE Transactions on Device and Materials Reliability

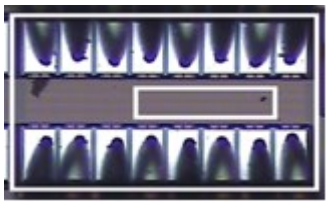

Fig. 4. Microphotograph of a 65nm test chip (489x332μm^2), with 128 PMOS transistors of 4 different aspect ratios.

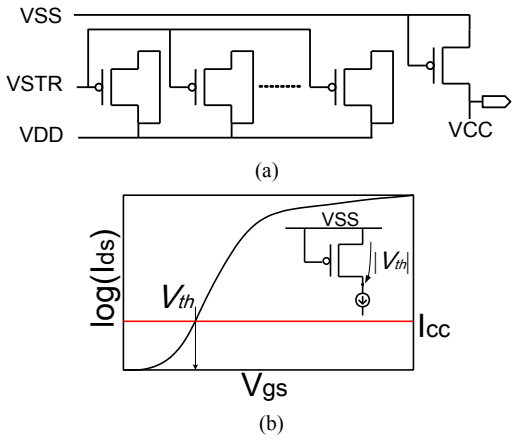

Fig. 5. Measurement setup: (a) All devices are under stress except the device under measurement. (b) V_{th} measurement using constant current method.

statistical device and circuit aging data at 65nm. Section VI concludes this paper.

II. Test Structure and Measurement Principle

To analyze aging variability and develop a reliable lifetime prediction method, we collect statistical device data from a 65nm test chip as shown in Fig. 4 [9]. The test chip is implemented with 11 metal layer CMOS process, consists of two identical arrays with 128 PMOS transistors in each array and switch controller. The gate material is oxy-nitride (SION) and the EOT = 2.3nm. The white box in Fig. 4 shows the circuit occupying an area of 489x332μm^2. NBTI exhibits significant recovery on releasing the stress voltage. Even a small stop of the stress time leads to large recovery, resulting in inaccurate aging data. Thus minimizing measurement delay is important for NBTI tests. This is especially challenging for multiple transistors stressed simultaneously, since obtaining degradation data by removing stress from all devices leads to a large measurement error. One solution is to place multiple DUTs on a chip so that stress periods and threshold voltage measurements can be conducted in parallel. This approach is very expensive, requiring a larger area and higher number of ports. Contrary to parallel measurement method, a parallelized stress period in a pipeline manner is implemented and V_{th} measurements for the DUTs are conducted in this work [9].

Fig. 5 presents the test structure and measurement principle implemented to extract statistical aging data. All the devices are stressed at 1.8V and a temperature of 125^{o}C for 200ks before collecting statistical aging data. Similarly, recovery in threshold voltage of a DUT in transistor array is measured by changing gate voltage to V_{DD} using a pass gate switch. These measurements are required in order to analyze device to device statistical aging behavior under constant stress and recovery operations. Except for the device in measurement, all other devices are stressed and V_{th} is measured using constant current method with a resolution of 0.2mV. Measurement time for each DUT is less than 0.4ms, minimizing the recovery and giving accurate aging data. Using these results, we validate the stochastic nature of NBTI, and derive T-D based *log(t)* model in Section III.

III. Trapping/Detrapping based NBTI Models

Traditionally, threshold voltage increase in a PMOS device is explained by Reaction Diffusion (R-D) theory. According to this theory, NBTI is caused by interfacial charge generation and diffusion due to Si-H bond breaking. Hydrogen is released and diffuses into gate dielectric, generating a positive charge which causes the shift in threshold voltage. This explanation predicts classical power law model where V_{th} shift has the following relation [2], [5], [16], [17]:

$$\Delta V_{th} = k \cdot t^n + M \quad (1)$$

where the time exponent, n, is a function of hydrogen species, *k* follows exponential dependence on voltage and temperature, and M accounts for device variations. The value of n is typically ~0.16. This model well predicts the exponential dependence of voltage and temperature.

With the advancement of fast measurement capabilities, several works show the role of charge trapping/de-trapping mechanism in NBTI degradation [18]-[19]. With the scaling of technology nodes, trapping and detrapping events leave distinct measureable signatures. Fig. 3(c) shows the measured V_{th} of a device under pure recovery with discrete V_{th} shifts due to trapping/de-trapping events, confirming the necessity for T-D based NBTI models for reliable aging prediction [20]-[22].

According to trapping/de-trapping theory, the traps located in the gate dielectric or at the silicon interface capture and re-emit some channel carriers that are responsible for the current between source and drain of a device [23]-[24]. When a negative bias is applied to a PMOS device, the trap energy is modulated. When the traps gain sufficient energy, it may capture carriers from the channel and thus, reduces the number of channel carriers. Due to this, the drain current decreases which is represented as the V_{th} increase. Similarly when the bias is relaxed, trapped charges are emitted resulting in V_{th} recovery of a device. Trapping/de-trapping of the charge carriers modulates the local V_{th} and also acts as a source of scattering, degrading the mobility. The occupation probability of the trap to be captured is independent of stress time [15]. The probability of trapping depends on capture time constant and that of de-trapping depends on emission time constant. Faster traps (i.e., shorter capture time constants) have a higher probability of getting filled as compared to slower traps. Furthermore, the trap occupation probability increases with gate bias and temperature. Such statistical nature of traps makes it complicated to develop a compact aging model.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TDMR.2014.2308140, IEEE Transactions on Device and Materials Reliability

The primary assumptions in deriving T-D based models are on the same lines as random telegraph noise [25]-[29]. Three primary assumptions in T-D modeling framework are:

- The number of traps in a device is Poisson distributed.
- Capture and emission time constants are uniformly distributed on the log scale.
- Trap energy is approximated as a U-shape function.

Using these basic trap properties, we aim to develop an improved compact aging model based on T-D theory that clearly explains the aging statistics and reduces error in long-term aging prediction from short-term stress measurements, assisting robust circuit design at an early stage.

The V_{th} shift is proportional to the average number of traps occupied by charge carriers, based on the trap properties, stressing conditions and stress time. Probability of a trap capturing a channel carrier and getting occupied in time t is represented as $P_{01}(t)$. The occupation probability of a trap getting occupied within small time interval (dt) after a given time t is written as [21]:

$$P_{01}(t+dt) = P_{01}(t)p_{11}(dt) + P_{00}(t)p_{01}(dt) \quad (2)$$

where, $p_{01}(dt)=1/\tau_c$ and $p_{11}(dt)=1-p_{10}(dt)=1/\tau_e$. τ_c and τ_e represent capture and emission time constants, respectively. They are dependent on the bias point and temperature. The values of time constants are determined by [27]:

$$\tau_c = 10^p(1+e^{-q}) \quad (3)$$

$$\tau_e = 10^p(1+e^{+q}) \quad (4)$$

where $p \in [p_{min}, p_{max}]$, where p_{min} and p_{max} define the time constants for the fastest and the slowest traps, respectively (p_{min}~1 and p_{max}>10). The logarithmic distribution of time constants due to uniform distribution of p has been published [18], [23]-[24]. Parameter q is dependent on trap energy and the Fermi level, incorporating voltage and temperature dependence.

The average number of occupied traps during the stress phase is given by:

$$n(t) = N.p_{01}(t, \tau_c, \tau_e) \quad (5)$$

where N is the Poisson parameter for trap distribution and p_{01} is the trap occupation probability and is given by

$$p_{01}(t) = \frac{\left[1-\exp(-t/\tau_{eq})\right]\tau_e}{\tau_e+\tau_c} \quad (6)$$

where $1/\tau_{eq}=1/\tau_c+1/\tau_e$. p_{01} is a function of stress time (t), capture and emission time constants (τ_c and τ_e). Using Eqs. (5) and (6) and substituting the distributions for time constants,

$$n(t) = \phi \int_{10^{-p\max t}}^{10^{-p\min t}} \frac{1-e^{-u}}{u} du \quad (7)$$

where ϕ is proportional to the number of available traps per device, stress voltage and temperature. Initial number of available traps accounts for the statistical variation in aging under BTI. p_{max} and p_{min} correspond to fastest and slowest traps, respectively [15]. By integrating the number of occupied traps over the stress time and assuming p_{min} ~ 1 and p_{max} > 10, the average number of traps occupied is:

$$\Delta V_{th} = \phi[A + \log(1+Ct)] \quad (8)$$

Above equation represent average number of occupied traps contributing to the overall threshold voltage increase. ΔV_{th} follows a logarithmic dependence with stress time, instead of the power law time dependence of t^n model. Model parameters A and C are dependent on trap's time constants. The variation in V_{th} shift is mainly due to ϕ, while A and C are relatively constant for a given process and stress condition.

Table I: Summary of R-D and T-D based aging models

Aging Model	V_{th} shift	Variation
R-D	$M+k\cdot t^n$	n: time exponent
T-D	$\phi[A+log(1+Ct)]$	$\phi \propto$ number of traps

IV. Statistical Device Aging Analysis

Statistical aging analysis of devices under BTI stress is performed on device level degradation data collected from the test chip described in section II. Accuracy and effectiveness of long-term prediction by both *log(t)* and t^n models are evaluated in this section. Silicon data are collected by stressing all PMOS devices at 1.8V for 200k seconds. Using the aging data, model parameters for both *log(t)* and t^n models are extracted. Fig. 6(a) shows the distribution of n and ϕ of respective models causing

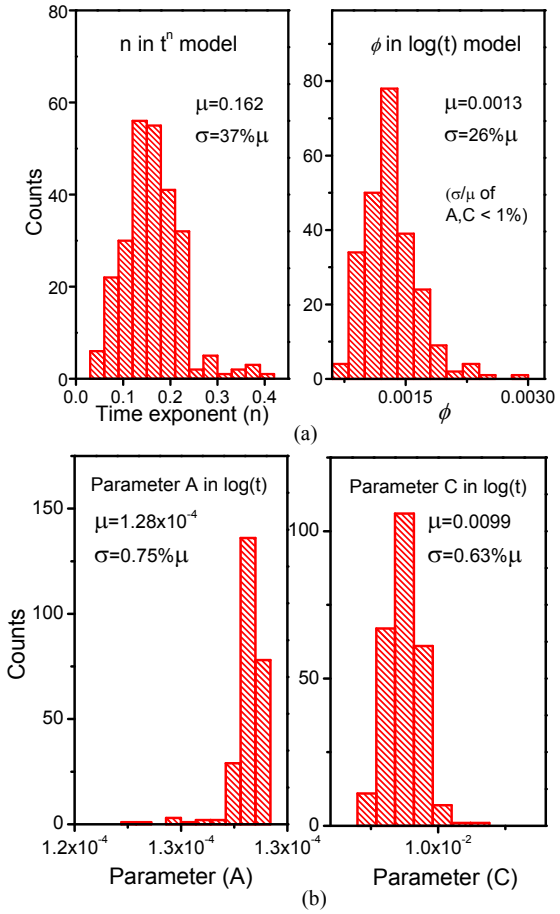

Fig. 6. (a) Parameters n and ϕ extracted from 65nm device data using t^n and *log(t)* models respectively. (b) Variation in parameters A and C for *log(t)* model.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TDMR.2014.2308140, IEEE Transactions on Device and Materials Reliability

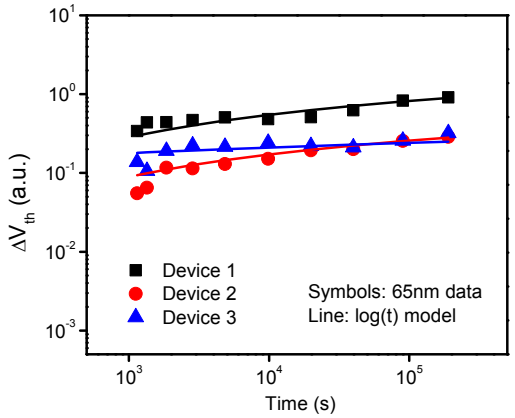

Fig. 6. (c) Prediction of T-D based *log(t)* model for individual devices. The LSE error for each device is: Device1=1.4323e-04, Device2=6.3560e-06 and Device3=1.4527e-05.

maximum variation in aging predictions. As t^n model predicts, the mean value of the time exponent is 0.16, but with excessive variation in its value. This variance in time exponent complicates the lifetime prediction in a circuit and forces to guard-band a design in a pessimistic manner. Although ϕ also exhibits variations, the mathematical relation with the stress time allows lifetime prediction with better stability. Parameters A and C for *log(t)* model are almost constant with variance of <1% across different devices. Fig. 6(b) shows the distribution of parameter A and C for T-D based *log(t)* model. Fig. 6(c) shows the prediction of T-D based *log(t)* model for 3 different devices with LSE errors within modeling error range.

Stress time plays an important role in extraction of the model parameters. It is desirable to extract the model parameters with minimum cost in terms of stress time. Thus it is important to evaluate the stability of model parameter with respect to stress time. Fig. 7 shows the stability of time exponent (n) for t^n model and parameters A, ϕ and C for T-D based *log(t)* model when extracted for different stress time. The value of n approaches 0.16 when the stress time used is long enough, which is consistent with R-D theory prediction. But it exhibits much higher values when shorter stress time is used. Parameters ϕ, A and C for T-D based *log(t)* model are considerably stable even

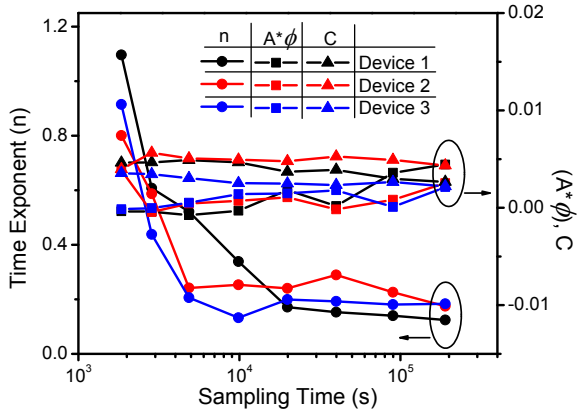

Fig. 7. Large variation in extracted time exponent (n) for t^n model using different stress time. Model parameters A, ϕ and C for T-D based *log(t)* model remains constant irrespective of extraction time.

for shorter stress time. Variation in parameter A is shielded by stability of the parameter ϕ. This constant nature of parameters at different stress time enables accurate aging prediction with minimum measurement cost.

The randomness in the initial V_{th} of different PMOS devices is reflected in the V_{th} shift under aging. The correlation plot in Fig. 8(a) shows that ΔV_{th} has almost no correlation with fresh V_{th} and device size [30]. The variability in initial V_{th} (t=0) and ΔV_{th} decreases as the device size increases. Further evaluation of variation as a function of device size is conducted, as shown in Fig. 8(b). The randomness is inversely proportional to the square root of the transistor area and the variation slope is $0.12\mu m^{-1}$. The relation is given as [10],

$$\sigma(\phi) = \frac{0.12um^{-1}}{\sqrt{WL}} \quad (9)$$

Above equation predicts that the aging variability increases with scaling of technology nodes.

To investigate more details of statistical aging, a single PMOS device is subjected to continuous stress and recovery cycle. The device is provided ample recovery time before stressed again. Similar experiment is performed on 32 devices on the same chip with the same area to evaluate the aging randomness. Fig. 9(a) shows the V_{th} distribution at the end of first stressing cycle for 32 different devices stressed at 1.8V and 125°C. As the number of initially available traps varies for different devices, the aging rate follows similar statistics. However, when the same device undergoes multiple stress and recovery cycles, initial number of traps will remain same. By doing this experiment, we eliminate major variation source and analyze the impact of other trap properties. Fig. 9(b) shows the

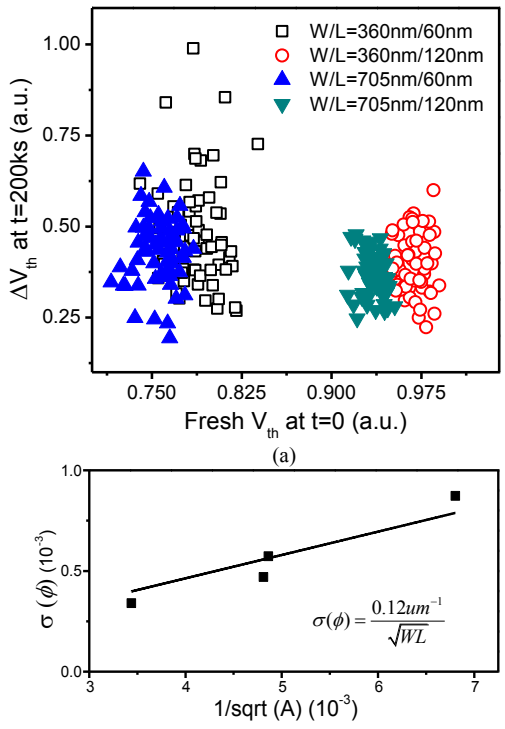

Fig. 8. (a) No correlation between fresh V_{th} (t=0) and V_{th} shift. (b) Decrease in ϕ variation with increase in transistor sizing.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TDMR.2014.2308140, IEEE Transactions on Device and Materials Reliability

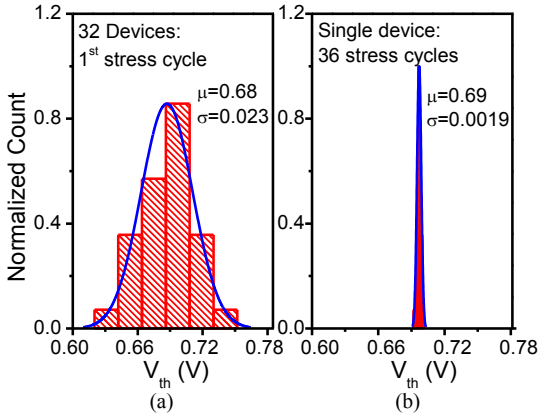

Fig. 9. Distribution of (a) V_{th} at end of the 1st stress cycle for 32 devices, (b) V_{th} of a single device for 36 stress cycles.

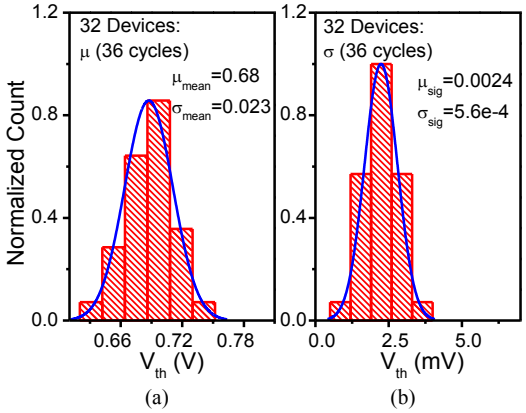

Fig. 10. Distribution of (a) $\mu(V_{th})$ for 36 cycles for 32 devices, (b) $\sigma(V_{th})$ for 36 cycles for 32 devices.

distribution of threshold voltage at the end of each 36 stress cycle for a single device. The mean of V_{th} is roughly same, but the variance reduces significantly. This deviation in V_{th} for the same device shows the stochastic nature of capture and emission time constants, which is not as significant as ϕ that represents the initial number of available traps. This statistical property confirms the stability of parameters A and C in *log(t)* model, which are functions of trap's time constants (τ_c and τ_e). Furthermore, Fig. 10(a) evaluates the mean of all 36 stress cycles for 32 devices, concurring with the mean and standard deviation for the first cycle. The variation in parameter ϕ dominates the aging statistics over other parameters, which is well demonstrated in Fig. 10b.

With a concrete validation of T-D based *log(t)* model for aging mean and variance, we focus on the impact on aging statistics on long-term device-level prediction. Conventionally, aging models are calibrated by collecting complete set of silicon data at different voltages and temperatures. Accumulating such a complete and accurate set of data for a very long time is expensive process. Due to time constraints, silicon data are collected for a short-term measurement operation. Leveraging this short-term data set aging model is calibrated and using these calibrated models, lifetime of circuit is extrapolated. Based on the aging prediction, circuits are designed with proper guard banding to ensure robust operation for the lifetime. It is thus

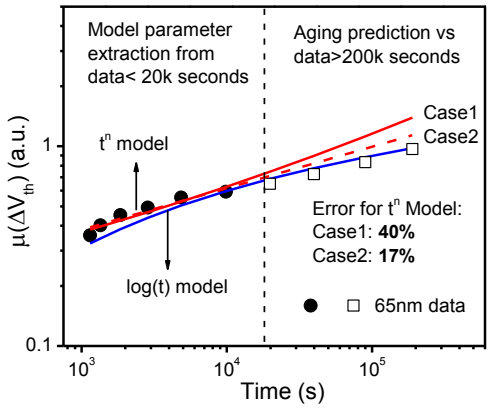

Fig. 11. Model prediction of mean of ΔV_{th} for 200k seconds using the model parameters extracted from time<20k seconds.

essential to evaluate the effectiveness of T-D based *log(t)* model with conventional t^n model for long-term prediction. In order to validate and compare trapping/de-trapping theory, two approaches are considered. In *first approach*, we first extract model parameters for t^n and *log(t)* model from statistical stress data collected for short time, i.e., <20k seconds for individual V_{th} shift of 32 transistors. The average value of the extracted parameters is used to predict long-term degradation for a stress time of 200k seconds. These model predictions are then compared with actual silicon data from 20k to 200k seconds. Fig. 11 shows the mean of ΔV_{th} prediction by t^n model that overestimates the degradation by 40% (case-1). In *second approach*, V_{th} shift of 32 stressed devices is averaged and this mean for stress time <20k seconds is used to calibrate t^n model. The calibrated model used for long-term prediction (200k seconds) overestimates V_{th} shift by 17% (case 2). This over-prediction is due to the high sensitivity of t^n model to time exponent. The value of time exponent extracted from a shorter stress time is higher than expected 0.16 (Fig.7) which results in prediction error at higher stress time. *log(t)* model accurately predicts the silicon behavior at higher stress time due to stability of model parameters.

As discussed previously, aging variability plays an important role for reliable design. Similar to mean, evaluation of variance

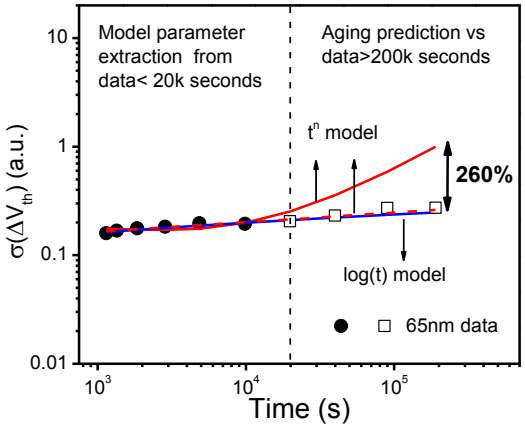

Fig. 12. Model prediction of variance of ΔV_{th} for 200k seconds using the model parameters extracted from time<20k seconds. t^n model overestimates variance by 260%.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TDMR.2014.2308140, IEEE Transactions on Device and Materials Reliability

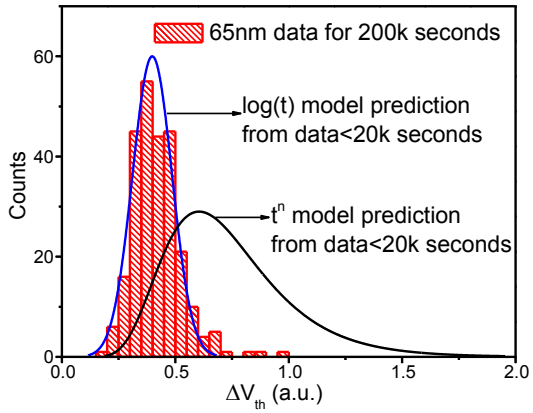

Fig. 13. T-D based model well predicts the statistical V_{th} shift for 200ks and matches the measurement aging data.

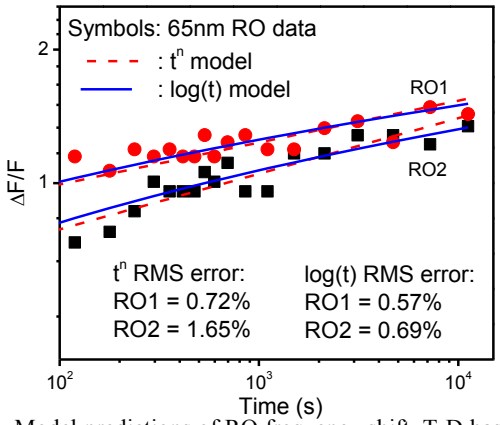

Fig. 14. Model predictions of RO frequency shift. T-D based *log(t)* model well captures frequency shift.

for both models (Fig. 12) are done by both approaches. The variance of ΔV_{th} predicted by t^n model by following *first approach* overestimates sigma by 260%. Such a large deviation of variance complicates the design protection strategies leading to overly pessimistic solutions. An empirical t^n model can be fitted by first estimating the variance from silicon data for smaller stress time (*second approach*), shown as dashed line in Fig. 12. Such approach gives better matching but fails to show the variance of model parameters. The *log*(*t*) model accurately captures the increase of both mean and variance with longer stress time. The variation is mainly attributed to the randomness in parameter ϕ, which is proportional to the fluctuation in number of available traps. Other model parameters (A and C) do not suffer high variation. The variation in parameter ϕ has only linear impact on V_{th} shift making it more reliable than conventional t^n model. Fig. 13 presents the distribution of measured ΔV_{th} after stress time of 200k and ΔV_{th} prediction using model parameters extracted from 20k. The logarithmic model from T-D theory correctly estimates the mean and variance of V_{th} shift, since degradation is less sensitive to model parameter variation from t^n model. The T-D model accurately predicts variability in aging due to variability in traps per device. The statistical aging analysis completed in this section helps localize critical model parameters that cause error in statistical lifetime prediction. The logarithmic modeling framework based on trapping/de-trapping theory enables efficient extraction of model parameters using short-term measurements and accurately predicts long-term statistical device aging.

V. Statistical Circuit Aging Analysis

With thorough understanding of aging statistics for devices, we analyze randomness in circuit degradation with stress time. This degradation of circuit performance is used to further evaluate the effectiveness of trapping/de-trapping based *log(t)* model and t^n model. To validate T-D theory in circuit aging, statistical aging data from 80 ring oscillators at 65nm bulk CMOS process, which is a different fabrication technology than process used for 65nm device characterization (Fig. 4) [31]. As the technology is not high-K metal gate, the concerns of positive bias temperature instability (PBTI) is nullified. The PMOS devices in ring oscillator being stressed are thin oxide devices, while other devices are thick oxide. Thus, the measured frequency degradation of ring oscillators is immune to peripheral devices aging. To get accurate frequency shift due to aging, two identical ring oscillators (RO) are used, of which one RO is stressed and the other RO acts as a reference source. Difference between reference and aged RO generates a beat frequency giving accurate degradation results by eliminating the mismatch and possible degradation of peripheral components. Statistical measurements of 80 RO are accompanied with BTI recovery due to changing stress conditions. To extract accurate aging data, unwanted BTI recovery due to stress interruption is eliminated with μs order measurements while frequency shift measurement resolution is as low as 0.07%. Using these accurate and efficient aging results, we perform statistical analysis on circuit aging data.

The ring oscillator is stressed at 2.0V at room temperature for 10k seconds. Aging data for initial 10k seconds is used to extract the model parameters for both t^n and *log(t)* model. Based on these model parameters, frequency shift for ring oscillator is predicted in Fig. 14 for two different ROs. As compared with silicon data, both t^n model and T-D based *log(t)* model well predict the frequency degradation. With the increase in the stress time, the overestimation of t^n model over actual data increases, similar as seen from the device data. Distributions of

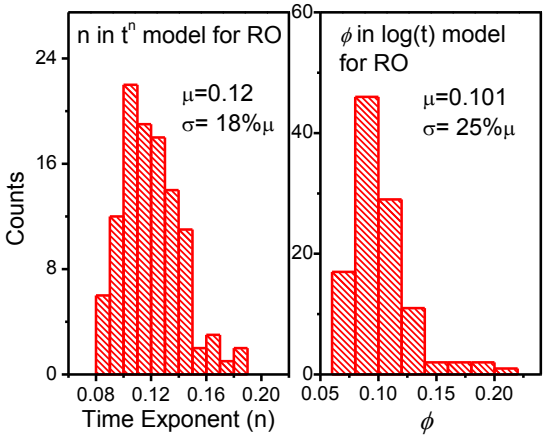

Fig. 15. Model parameters *n* and ϕ extracted using 65nm data for ring oscillators for t^n and *log(t)* models.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TDMR.2014.2308140, IEEE Transactions on Device and Materials Reliability

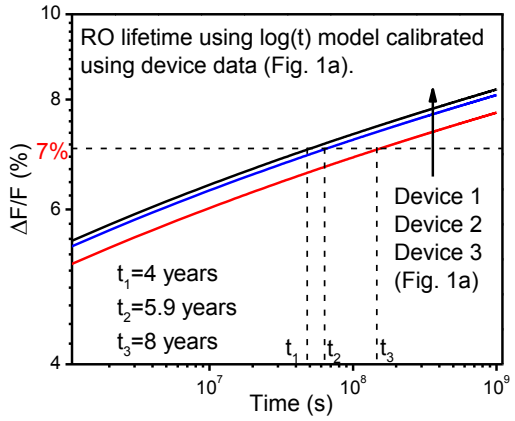

Fig. 16. Lower variation in T-D based lifetime prediction of a ring oscillator using the three test cases for discrete devices shown in Fig. 1(a).

critical parameters n and ϕ for t^n and *log(t)* model are presented in Fig. 15. The lifetime prediction can vary from few days to months to years depending on the distribution of time exponents. Trapping/de-trapping based *log(t)* model accurately captures the mean and variance for circuit aging. The deviation is less as compared to discrete device data (Fig. 6). This expected reduction in variance is due to the averaging effect of more transistors involved in circuit-level aging measurement. The variance is further moderated due to beat frequency generation used for accurate aging determination. Evaluation of σ^2/μ is constant with the stress time for device and circuit aging. This is consistent with σ/μ ratio reducing with stress time which is presented in previous publication [31].

Based on the extracted parameters of the *log(t)* model from the device data which shows higher variance in time exponent values, the lifetime of RO is predicted assuming some amount of frequency shift (7% in this case) at the end-of-life. Fig. 16 illustrates that the T-D model estimates the lifetime with much less variation within few years unlike the dramatic variation from few days to years using the t^n model (Fig. 2). The new aging model from the T-D theory facilitates accurate long-term lifetime prediction, helping develop a robust design methodology in the design cycle.

VI. Conclusion

This works advocates trapping/de-trapping theory to accurately explain aging prediction in scaled PMOS devices. T-D theory clarifies the unexplained behaviour of fast and discrete steps in recovery on removing the stress voltage. Leveraging 65nm aging data for multiple PMOS devices of different sizes, we gain valuable insight on statistical nature of aging, while t^n model is not able to capture NBTI variability due to high sensitivity on time exponent, overestimating circuit lifetime. Based on statistical device data set, we conclude that NBTI degradation follows a *log(t)* dependence with stress time as predicted by trapping/de-trapping theory. Parameter ϕ dominates model variance due to varying number of initial traps in devices, but it generates lower fluctuations in aging prediction due to linear relation to stress time. By extracting ϕ and its variance from short term measurements, *log(t)* model derived from the T-D theory correctly predicts nominal long-term V_{th} shift and the variability. *log(t)* model also correctly captures mean and aging variance in 65 nm ring oscillators. In summary, T-D based *log(t)* model provides accurate statistical aging prediction for reliable design practice.

Acknowledgement

This paper is partially supported by the DARPA – Integrity and Reliability of Integrated Circuits program. (Contract #: HR0011-11-C-0067).

References

[1] International Technology Roadmap of Semiconductors, 2009 (available at www.itrs.net).

[2] K. O. Jeppson and C. M. Svensson, "Negative bias stress of MOS devices at high electric fields and degradation of MNOS devices," *J. Applied Physics*, vol. 48, no. 5, pp. 2004-2014, 1977.

[3] D. K. Schroder and J. A. Babcock, "Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing," *J. Applied Physics*, vol. 94, no. 1, pp. 1-18, 2003.

[4] M. A. Alam, "A critical examination of the mechanics of dynamic BTI for PMOSFETs," *IEDM*, 14.4.1-14.4.4, 2003.

[5] W. Wang, V. Reddy, A. T. Krishnan, R. Vattikonda, S. Krishnan and Y. Cao, "Compact modeling and simulation of circuit relaibility for 65nm CMOS technology," *TDMR*, vol. 7,no. 4, pp. 509-517, 2007.

[6] T. Grasser, et al., "The paradigm shift in understanding the bias temperature instability: From reaction-diffusion to switching oxide traps," *TED*, vol. 58, no. 11, pp. 3652-3666, Nov. 2011.

[7] V. Huard, M. Denais, "Hole trapping effect on methodology for DC and AC negative bias temperature instability measurements in pMOS transistors," *IRPS*, pp. 40-45, 2004.

[8] J. Keane, W. Zhang and C. H. Kim, "An on-chip monitor for statistically significant circuit aging characterization," *IEDM*, pp. 4.2.1-4.2.4, 2010.

[9] T. Sato, et al., "A device array for efficient bias temperature instability measurements," *ESSDERC*, pp. 143-146, 2011.

[10] J. Velamala, K. Sutaria, T. Sato and Y. Cao, "Aging statistics based on trapping/detrapping: Silicon evidence, modeling and long-term prediction," *IRPS*, 2F.2.1-2F.2.5, 2012.

[11] S. Deora, V. Maheta, S. Mahapatra, "NBTI lifetime prediction in SiON p-MOSFETs by H/H_2 Reaction-Diffusion(RD) and dispersive hole trapping model," *Reliability Physics Symposium (IRPS), 2010 IEEE International* , vol.1105, no.1114, pp.2-6 May 2010.

[12] V. Huard, "Two independent components modeling for Negative Bias Temperature Instability," *Reliability Physics Symposium (IRPS), 2010 IEEE International* , vol.33 no.42 pp. 2-6, May 2010.

[13] T. Grasser, B. Kaczer, W. Goes, T. Aichinger, P. Hehenberger, M. Nelhiebel, "A two-stage model for negative bias temperature instability," *Reliability Physics Symposium, 2009 IEEE International* , vol.33, no.44, pp. 26-30, April 2009.

[14] T. Grasser, B. Kaczer, "Evidence That Two Tightly Coupled Mechanisms Are Responsible for Negative Bias Temperature Instability in Oxynitride MOSFETs," *Electron Devices, IEEE Transactions on* , vol.56, no.5, pp.1056,1062, May 2009.

[15] G. I. Wirth, R. da Silva, B. Kaczer "Statistical Model for MOSFET Bias Temperature Instability Component Due to Charge Trapping," *Trans. on Electron Dev.*, vol. 58, no. 8, pp. 2743-2751, 2011.

[16] M. A. Alam, H. Kufluoglu, D. Varghese and S. Mahapatra, "A Comprehensive Model for PMOS NBTI Degradation," *Microelectronics Reliability*, vol. 47, no. 6, pp. 853-862, June 2007.

[17] S. Mahapatra, et al., "A critical re-evaluation of the usefulness of R-D Framework in predicting NBTI Stress and Recovery," *IRPS*, pp. 6A.3.1 - 6A.3.10, April 2011.

[18] H. Reisinger, O. Blank, W. Heinrigs, A. Mühlhoff, W. Gustin, and C. Schlünder, "Analysis of nbti degradation- and recovery-behavior based on ultra-fast VT-measurement," *IRPS*, pp. 448-453, 2006.

[19] T. Grasser, et al., "Switching oxide traps as the missing link between negative bias temperature instability and random telegraph noise," *IEDM*, pp. 729-732, 2009.

[20] T. L. Tewksbury and H.-S. Lee, "Characterization, modeling, and minimization of transient threshold voltage shifts in MOSFETs," *J. Solid-State Circuits*, v. 29, pp. 239–252, Mar. 1994.

[21] R. da Silva and G. Wirth. "Logarithmic behavior of the degradation dynamics of metal oxide semiconductor devices," *J. Statistical Mechanics*, v. P04025, p. 01-12, April 2010.

[22] B. Kaczer, et al., "NBTI from the perspective of defect states with widely distributed times," *IRPS*, pp. 55-60, 2009.

[23] B. Kaczer, et al., "Ubiquitous relaxation in BTI stressing—new evaluation and insights," *IRPS*, pp. 20-27, 2008.

[24] T. Grasser, H. Reisinger, P.-J. Wagner, F. Schanovsky, W. Goes and B. Kaczer, "The time dependent defect spectroscopy (TDDS) for the characterization of the bias temperature instability," *IRPS*, pp. 16-25, 2010.

[25] G. I. Wirth, J. Koh, R. da Silva, R. Thewes, and Ralf Brederlow, "Modeling of statistical low-frequency noise of deep-submicron MOSFETs," *Trans. on Electron Dev.*, vol. 52, pp. 1576-1588, July 2005.

[26] A. van der Wel, et al. "Low-frequency noise phenomena in switched MOSFETs," *J. Solid-State Circuits*, vol. 42, pp. 540-550, Mar. 2007.

[27] M. J. Kirton and M. J. Uren, "Noise in solid-state microstructures: A new perspective on individual defects, interface states and sow-frequency (1/f) noise", *Advances in Physics*, vol. 38, p. 367-468, 1989.

[28] G. Wirth, R. da Silva and R. Brederlow, "Statistical model for the circuit bandwidth dependence of low-frequency noise in deep-submicrometer MOSFETs," *Trans. on Electron Dev*, vol. 54, pp.340-345, Feb. 2007.

[29] G. Wirth, R. da Silva, P. Srinivasan, J. Krick and R. Brederlow. "Statistical model for MOSFET low-frequency noise under cyclo-stationary conditions," *IEDM*, p.30.5.1-4, 2009.

[30] S. Pae, J. Maiz, C. Prasad, "Effect of NBTI degradation on transistor variability in advanced technologies," Integrated Reliability Workshop, pp.18-21, Oct. 2007.

[31] J. Keane, W. Zhang and C. H. Kim, "An array-based odometer system for statistically significant circuit aging characterization," JSSC, vol.46, pp. 2374-2385, Sept. 2011.

Ketul B. Sutaria (S'11) received the B Tech. degree in Electronics and Communication Engineering from Nirma University in 2007. He received the M.E. degree in Microelectronics from Birla Institute of Technology and Science, Pilani, India in 2009. He is currently pursuing Ph.D. degree in electrical engineering from Arizona State University. He was Intern with Texas Instruments, Bangalore, India, in 2009 and Samsung, Milpitas, CA, in 2013-14. From 2009 to 2010, he was a Senior Research Fellow with DA-IICT, Gandhinagar, India. His research interests include reliability modeling and simulation in AMS circuits and silicon characterization for reliability.

Jyothi Bhaskarr Velamala (S'09) received the B Tech. degree in Electronics and Communication Engineering from Indian Institute of Technology, Guwahati in 2008. He received the M.S. degree and the Ph.D. degree in electrical engineering from Arizona State University, Tempe, AZ in 2010 and 2012, respectively. He was with Global Foundries, Sunnyvale, CA in 2011 and Intel Corporation, Santa Clara in 2012 as a summer intern. He has authored and co-authored 18 journal and conference publications, and one book chapter. His research interests include Reliability effects in scaled CMOS technology and circuits; design and test solutions for resilience.

Chris H. Kim (M'04, SM'10) received his B.S. and M.S. degrees from Seoul National University and a Ph.D. degree from Purdue University. He spent a year at Intel Corporation where he performed research on variation-tolerant circuits, on-die leakage sensor design and crosstalk noise analysis. He joined the electrical and computer engineering faculty at the University of Minnesota, Minneapolis, MN, in 2004 where he is currently an associate professor.

Prof. Kim is the recipient of an NSF CAREER Award, a Mcknight Foundation Land-Grant Professorship, a 3M Non-Tenured Faculty Award, DAC/ISSCC Student Design Contest Awards, IBM Faculty Partnership Awards, an IEEE Circuits and Systems Society Outstanding Young Author Award, ISLPED Low Power Design Contest Awards, and an Intel Ph.D. Fellowship. He is an author/coauthor of 100+ journal and conference papers and has served as the technical program committee chair for the 2010 International Symposium on Low Power Electronics and Design (ISLPED). His research interests include digital, mixed-signal, and memory circuit design in silicon and non-silicon (organic TFT and spin) technologies.

Takashi Sato (M'98) received B.E. and M.E. degrees from Waseda University, Tokyo, Japan, and a Ph. D. degree from Kyoto University, Kyoto, Japan. He was with Hitachi, Ltd., Tokyo, Japan, from 1991 to 2003, with Renesas Technology Corp., Tokyo, Japan, from 2003 to 2006, and with the Tokyo Institute of Technology, Yokohama, Japan. In 2009, he joined the Graduate School of Informatics, Kyoto University, Kyoto, Japan, where he is currently a professor. He was a visiting industrial fellow at the University of California, Berkeley, from 1998 to 1999. His research interests include CAD for nanometer-scale LSI design, fabrication-aware design methodology, and performance optimization for variation tolerance. Dr. Sato is a member of the IEEE and the Institute of Electronics, Information and Communication Engineers (IEICE). He received the Beatrice Winner Award at ISSCC 2000 and the Best Paper Award at ISQED 2003.

Yu Cao (S'99-M'02-SM'09) received the B.S. degree in physics from Peking University in 1996. He received the M.A. degree in biophysics and the Ph.D. degree in electrical engineering from University of California, Berkeley, in 1999 and 2002, respectively.

He worked as a summer intern at Hewlett-Packard Labs, Palo Alto, CA in 2000, and at IBM Microelectronics Division, East Fishkill, NY, in 2001. After working as a post-doctoral researcher at the Berkeley Wireless Research Center (BWRC), he is now an Associate Professor of Electrical Engineering at Arizona State University, Tempe, Arizona. He has published numerous articles and two books on nano-CMOS modeling and physical design. His research interests include physical modeling of nanoscale technologies, design solutions for variability and reliability, and reliable integration of post-silicon technologies.

Dr. Cao was a recipient of the 2010 and 2012 Top 5% Teaching Award, Schools of Engineering, Arizona State University, 2009 ACM SIGDA Outstanding New Faculty Award, 2009 Promotion and Tenure Faculty Exemplar, Arizona State University, 2009 Distinguished Lectured of IEEE Circuits and Systems Society, 2008 Chunhui Award for outstanding oversea Chinese scholars, the 2007 Best Paper Award at International Symposium on Low Power Electronics and Design, the 2006 NSF CAREER Award, the 2006 and 2007 IBM Faculty Award, the 2004 Best Paper Award at International Symposium on Quality Electronic Design, and the 2000 Beatrice Winner Award at International Solid-State Circuits Conference. He has served as Associate Editor of the IEEE Transactions on CAD, and on the technical program committee of many conferences. He is a member of the IEEE EDS Compact Modeling Technical Committee.