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Large-Area, Low-Voltage, Antiambipolar Heterojunctions from Solution-Processed Semiconductors

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Supporting Information

ABSTRACT: The emergence of semiconducting materials with inert or dangling bond-free surfaces has created opportunities to form van der Waals heterostructures without the constraints of traditional epitaxial growth. For example, layered two-dimensional (2D) semiconductors have been incorporated into heterostructure devices with gate-tunable electronic and optical functionalities. However, 2D materials present processing challenges that have prevented these heterostructures from being produced with sufficient scalability and/or homogeneity to enable their incorporation into large-area integrated circuits. Here, we extend the concept of van der Waals heterojunctions to semiconducting p-type single-walled carbon nanotube (s-SWCNT) and n-type amorphous indium gallium zinc oxide (a-IGZO) thin films that can be solution-processed or sputtered with high spatial uniformity at the wafer scale. The resulting large-area, low-voltage p−n heterojunctions exhibit antiambipolar transfer characteristics with high on/off ratios that are well-suited for electronic, optoelectronic, and telecommunication technologies.

KEYWORDS: *p−n heterojunction, carbon nanotube, indium gallium zinc oxide, van der Waals heterostructure, frequency doubler, phase shift keying*

The growing inventory of layered 2D semiconductors with diverse electronic characteristics has allowed atomically thin and dimensionally abrupt heterostructures to be realized.[1,2] Several device types including tunneling field-effect transistors (FETs),[3,4] Schottky junctions,[5] photovoltaic devices,[6,7] p−n junction diodes,[8−10] inverters,[11] and nonvolatile memory cells[12] have been demonstrated with these van der Waals heterostructures. The weak interlayer bonding in these structures provides strain-free and defect-free interfaces without the constraints of epitaxy, which has accelerated the demonstration of novel device concepts and charge transport behavior. Prominent among these phenomena is antiambipolarity, first observed in gate-tunable, carbon-nanotube/single-layer MoS_2 p−n heterojunctions[9] and more recently in 2D/2D p−n heterojunctions.[10] While the examples above have employed layered 2D semiconductors using processing methods with limited scalability and uniformity, the concept of a van der Waals heterojunction can be extended to any two materials with native oxide-free surfaces[13,14] that do not covalently bond when brought in intimate contact.[15−17] Using this concept, we demonstrate here a scalable path to antiambipolar p−n heterojunctions by integrating two dissimilar solution-processable, air-stable materials: p-type single-walled carbon nanotube (s-SWCNT) and n-type amorphous indium gallium zinc oxide (a-IGZO). Conventional photolithography is used to fabricate large-area heterojunction arrays with high-k gate dielectrics, thereby providing low-voltage operation and device statistics at the cm^2 level. The antiambipolar behavior enables demonstration of telecommunications applications such as frequency doublers and phase shift keying circuits with reduced number of circuit elements compared to conventional field-effect transistor technology.

Wafer-scale heterojunction p−n diodes were fabricated using solution-processed, p-type s-SWCNTs[18] and n-type a-IGZO thin films[19−21] via standard photolithographic and etching techniques (Figure 1a; see Methods and Supporting Information Sections S1 and S2 for more details). The resulting device structure has an s-SWCNT FET, s-SWCNT/a-IGZO p−n heterojunction, and a-IGZO FET in series (Figure 1b from left to right). In particular, the p−n heterojunction region between the Mo and Au electrodes comprises partially overlapping patterned a-IGZO and s-SWCNT films (Figure 1c−f).

This device architecture enables electrical characterization of the p−n heterojunction in addition to control FETs from the individual semiconductors. Figure 2a,b shows output curves of a representative p−n heterojunction at different gate biases (V_G). Rectifying behavior is observed with rectification ratios exceeding 10^3 for V_G = 3 V (Supporting Information Section S3). The forward current at V_G = 4 V is low (~20 nA) but

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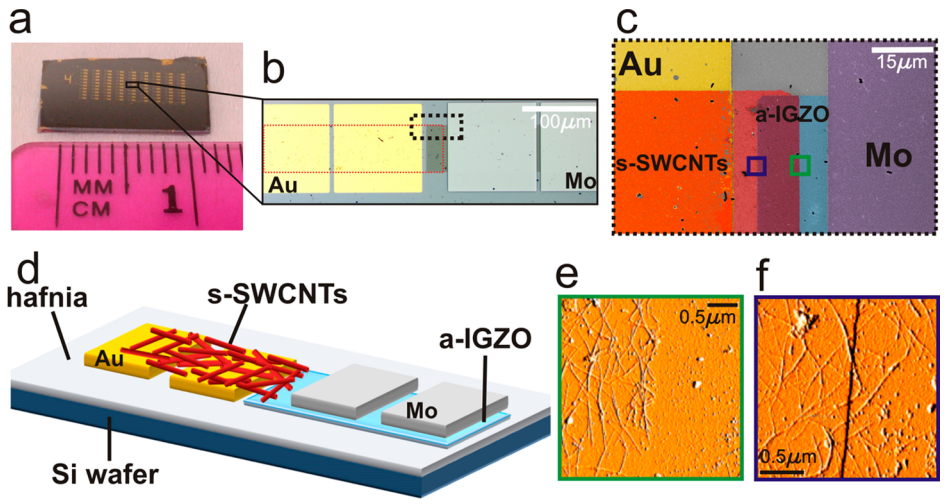

Figure 1. Structure of the s-SWCNT/a-IGZO p−n heterojunctions. (a) Optical image of a fully fabricated p−n heterojunction device array. (b) Expanded optical micrograph of a representative individual device in the array. (left to right) p-type s-SWCNT FET, s-SWCNT/a-IGZO p−n heterojunction, and n-type a-IGZO FET. The dashed red outline indicates the patterned s-SWCNT thin film, while the dark rectangular region in the channel is the patterned a-IGZO thin film. (c) False-color SEM image of the dashed black outline in panel b. The different layers are appropriately colored and labeled. The Au electrode (drain) is biased, while the Mo electrode (source) is grounded. (d) Schematic diagram of an individual unit of the array shown in panel a with appropriately labeled layers. (e,f) Atomic force micrographs (amplitude error) of the regions denoted by the green and purple squares in panel c. The patterned boundary of the s-SWCNT thin film is visible in panel e, while the black line in panel f represents the patterned edge of the a-IGZO film.

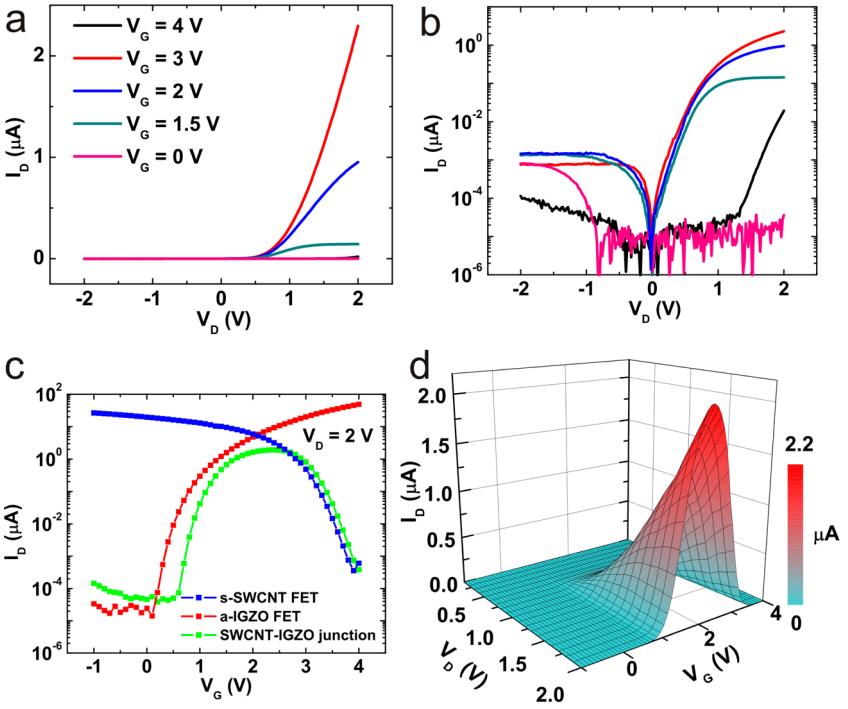

Figure 2. Electrical properties of the s-SWCNT/a-IGZO antiambipolar p−n heterojunctions. (a,b) Output characteristics of a representative device at different gate voltages on linear (a) and semilog (b) *y*-axis. The device is in a nearly insulating state at V_G = 4 and 0 V, while it shows a highly rectifying state at the intermediate gate voltages. The weak gate modulation of the reverse saturation current magnitude can be seen in panel b. The plot colors in panels a and b represent the same gate voltage values as indicated in the legend of panel a. (c) Semilog transfer characteristics of a p-type s-SWCNT FET (blue), n-type a-IGZO FET (red), and s-SWCNT/a-IGZO p−n heterojunction (green). (d) Three-dimensional representation of the antiambipolar transfer characteristics at varying drain biases. The grid lines running along the V_D axis represent the forward output characteristics at the indicated gate voltage (V_G).

abruptly increases for intermediate V_G values and then falls to the instrumental noise floor (∼10 pA) at V_G = 0 V. This behavior is also evident in the p−n heterojunction transfer plots (I–V_G) (Figure 1c, green). This antiambipolar transfer plot shows one current maximum (on-state) in between two off-states at either extremes of the gate voltage range.[9] The voltage dependence of the antiambipolar plot is approximately a superposition of the transfer plots of the p-type and n-type unipolar FETs in red and blue, respectively (Figure 2c). An antiambipolar response can also be produced by connecting the

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two unipolar FETs in series (Supporting Information Section S4). However, this series geometry presents fabrication, scaling, and speed issues compared to the p−n heterojunction.

Because of screening from the ∼20 nm thick a-IGZO, the junction itself is less modulated by the gate field compared to p−n heterojunctions based on 2D materials,[9,10] thus simplifying the charge transport mechanism and facilitating the realization of reproducible and spatially homogeneous characteristics. For example, Figure 2b shows that the reverse saturation current possesses a relatively weak gate-dependence. In Figure 2d, three-dimensional plots of current (I_D) as a function of V_G and forward bias voltage (V_D) illustrate that the charge transport is primarily a result of two semiconductors with opposite carrier types in series. For example, cross sections along the V_D axis at V_G > 2.2 V (point of maximum current) resemble the output plots of s-SWCNT FETs under positive bias, whereas V_G < 2.2 V shows a saturating behavior that correlates with the output plots of a-IGZO FETs (Supporting Information Section S5). The V_G dependence of the rectification ratios, band alignments, and further details on the conduction mechanism are discussed in Supporting Information Section S6.

The large array of devices examined here (Figure 1a) enables assessment of the uniformity in performance by statistical means. As observed in Figure 3a, consistent antiambipolar behavior is observed among 115 devices measured on two separate chips (Figure 3a). Two important performance metrics for an antiambipolar device are the position of the current maximum in terms of gate voltage (V_{max}) and the on/off current ratio. Since V_{max} dictates the operational parameters of integrated circuits (vide infra), it is important for this parameter to be spatially homogeneous. As seen in Figure 3b, the histogram of V_{max} peaks at 2.2 V with a tight distribution (the standard deviation is approximately 8% of the V_G sweep range). Antiambipolar devices possess two off states, and thus, Figure 3c provides two histograms for the on/off ratio. In both cases, the $\log_{10}(I_{on}/I_{off})$ histograms have mean values >3 with relative standard deviations of 20% and 15% for the a-IGZO and s-SWCNT sides, respectively. The high (>1000) and consistent value of these on/off ratios suggests that these devices are suitable for digital electronic applications. Details on device dimensions and variations in the junction area in the array are discussed in Supporting Information Section S7.

The most important characteristic of the antiambipolar response curve is the presence of positive and negative transconductances on the left and right sides of the current maximum, respectively. The change in the sign of the transconductance can be exploited for analog circuit applications such as frequency doubling circuits (Figure 4a). Frequency doubling (or multiplying) circuits have broad applications ranging from analog communications to radio astronomy and THz sensing.[22] When an antiambipolar device is biased such that V_{offset} < V_{max}, the transconductance is positive with the current (I_{DS}) rising and the output voltage (V_o) across the resistor (R) increasing with the positive phase of the input signal. The case where V_{offset} > V_{max} is similar except that the output signal is out of phase with the input since the input signal experiences a negative transconductance with increasing voltage. Also, when V_G = V_{max}, the transconductance is zero, resulting in local maxima and minima in the output signal whenever the input signal crosses V_{max} in either direction. The overall effect is frequency doubling when V_{offset} is set equal to V_{max} (Figure 4c). If V_{offset} is moved away from V_{max}, the frequency doubling is incomplete, which supports our circuit

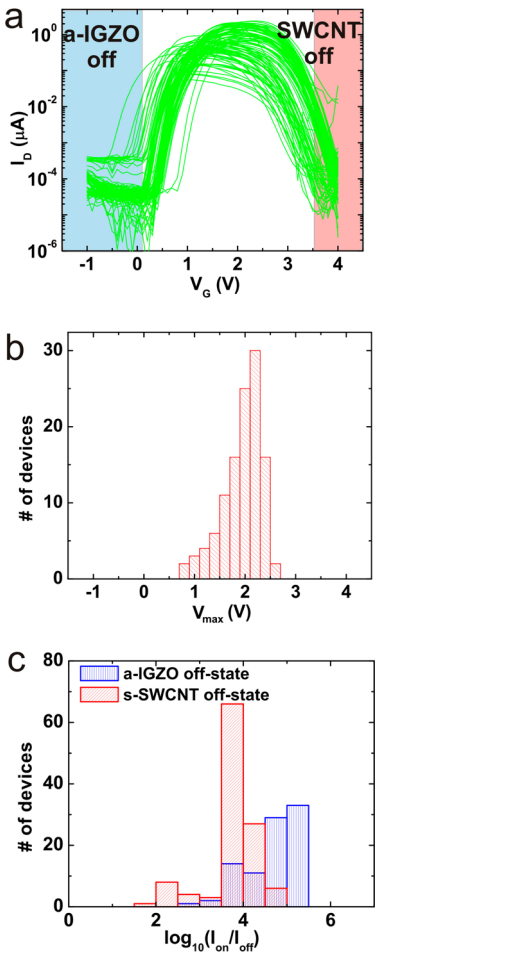

Figure 3. Performance metric statistics of the s-SWCNT/a-IGZO antiambipolar p−n heterojunctions. (a) Antiambipolar transfer characteristics of 115 separate devices. Each curve has two off states and a current maximum (on-state) between them. (b) Histogram of the gate voltages corresponding to the current maxima (mean = 1.89 V; standard deviation = 0.38 V). (c) Histograms of the on/off current ratios. The red and blue histograms correspond to the ratios derived using off-currents for the s-SWCNT (mean = 3.76; standard deviation = 0.94) and a-IGZO (mean = 4.55; standard deviation = 0.94), respectively. The average on/off ratio on the a-IGZO off side is higher due to the lower off-currents in the a-IGZO off-state as seen in panel a.

operation model and enables further tunability of the output signal. Note also that the power spectral purity of the frequency doubled output signal is ∼95%, which exceeds the performance of graphene-based frequency doublers[22,23] (Supporting Information Section S8). Refinements such as scaling down device dimensions and local gating are likely to further enhance the antiambipolar frequency doubling performance (e.g., enabling higher operating frequencies).

Antiambipolarity facilitates the realization of other analog signal processing circuits including binary phase shift keying (BPSK) circuits that are used for passband data transmission in digital communication systems.[24] These circuits map the conceptual symbols digital 0 and digital 1 into physical quantities that can be carried by alternating current (AC) signals. In this manner, BPSK is widely used for telecommunications and wireless data transmission technologies such as in the IEEE 802.11 standard,[25] commonly known as WiFi. Its main function is to modulate the carrier AC signal with no phase shift for digital 0 transmission and with a 180°

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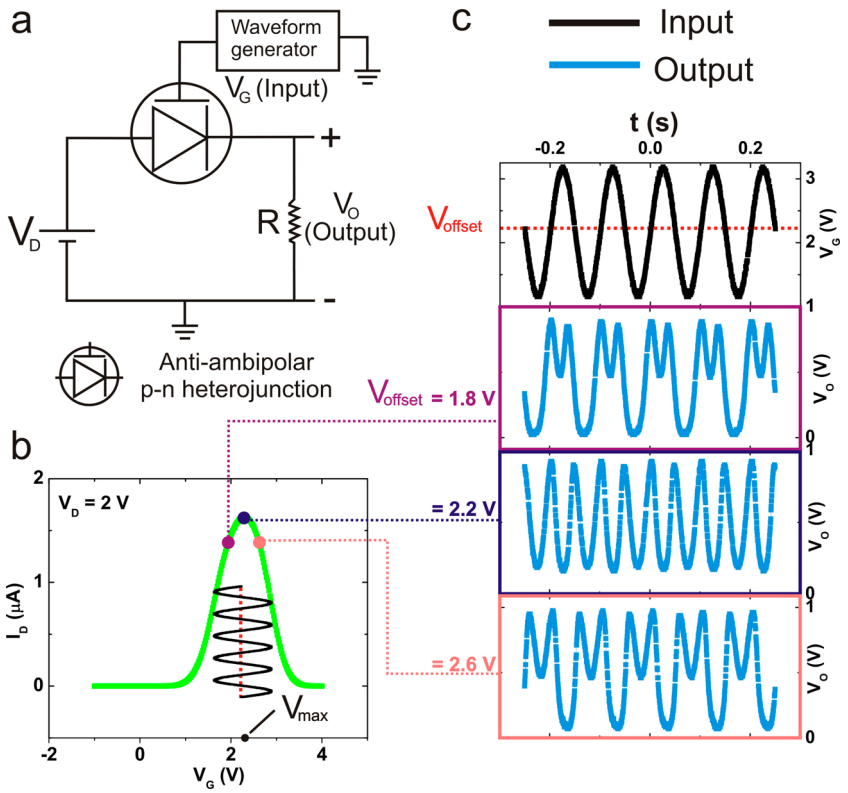

Figure 4. Frequency doubling circuit based on s-SWCNT/a-IGZO antiambipolar p−n heterojunctions. (a) Schematic of the circuit employing an antiambipolar heterojunction for frequency doubling. The circuit uses a single antiambipolar heterojunction in series with a resistor across which the output voltage (V_o) is measured using an oscilloscope. Series resistance R = 1 MΩ. The resistance was chosen to maintain an output voltage of 1 V when the junction resistance is minimized. (b) Representative transfer characteristic of an antiambipolar heterojunctions. The offset voltage that is applied to the sinusoidally varying input is indicated by the differently colored circles. (c) Input signal (black) and output signal (blue) for the three different values of the offset voltage indicated in panel b. Complete frequency doubling is observed when V_{offset} = V_{max}. More complicated signal conditioning occurs when V_{offset} is tuned away from V_{max}.

phase shift for digital 1 transmission. The input is typically a sine wave superimposed on a modulating square wave signal that possesses the desired data pattern. In the antiambipolar BPSK circuit (Figure 5a,b; Supporting Information Section S8), the output undergoes a phase shift at every edge of the square wave when the input V_{offset} is aligned with V_{max}. In contrast to conventional Si integrated circuit technology that achieves this circuit function using a Gilbert cell consisting of at least 7 FETs,[26,27] the antiambipolar implementation requires only one p−n heterojunction in series with one resistor. By changing V_{offset} and the input amplitude, another keying operation, namely, binary frequency shift keying (BFSK), is demonstrated (Figure 5c). BFSK achieves frequency doubling of the output AC signal in response to the input square wave and is a special case of frequency modulation with applications in microwave radio and satellite transmission systems.[24] Again, the antiambipolar implementation requires considerably fewer circuit elements compared to conventional Si technology, thus simplifying circuit design and implementation.

The present s-SWCNT/a-IGZO p−n heterojunction demonstrates that van der Waals heterostructures are not limited to 2D semiconductors, which considerably broadens the potential of this device concept. For example, the solution processability and ambient stability of s-SWCNTs and a-IGZO allow reproducible antiambipolar devices to be achieved over large areas on arbitrary substrates using well-established manufacturing methods. In this manner, a suite of telecommunications circuits have been implemented and found to possess improved simplicity compared to established Si technology. Furthermore, this p−n heterojunction device geometry allows engineering of the antiambipolar transfer curve by appropriate choice of the constituent semiconductors and their respective threshold voltages, thus presenting additional opportunities for customization of the antiambipolar response for other circuits and systems. Future work will focus on optimizing the device geometry to minimize its lateral footprint and fringe capacitance, which will enable improvements in integration density and operating speed.

Methods. *Materials Synthesis and Deposition.* a-IGZO films were grown by spin-coating a combustion precursor solution and annealing on a hot plate at 300 °C for 10 min.[19] The precursor solution consisted of In, Ga, and Zn nitrates dissolved in 2-methoxyethanol (0.05 mol L^{-1}) with the addition of acetylacetone as a fuel and NH_4OH to improve acetylacetone coordination to the metal. The In/Ga/Zn ratio of 72.5:7.5:20 was chosen to optimize transistor performance.[28] The total required film thickness (~20 nm) was achieved by four repeated spin-coating/annealing steps. The s-SWCNTs were sorted using density gradient ultracentrifugation (DGU). Sorted s-SWCNT thin films were prepared by vacuum filtration followed by thorough cleaning with DI water. SWCNT films were then transferred from a cellulose membrane onto device substrates using an acetone bath transfer technique.[29]

Device Fabrication and Measurements. Hafnia (15 nm) was deposited on a degenerately doped silicon wafer using atomic layer deposition followed by solution deposition of a-

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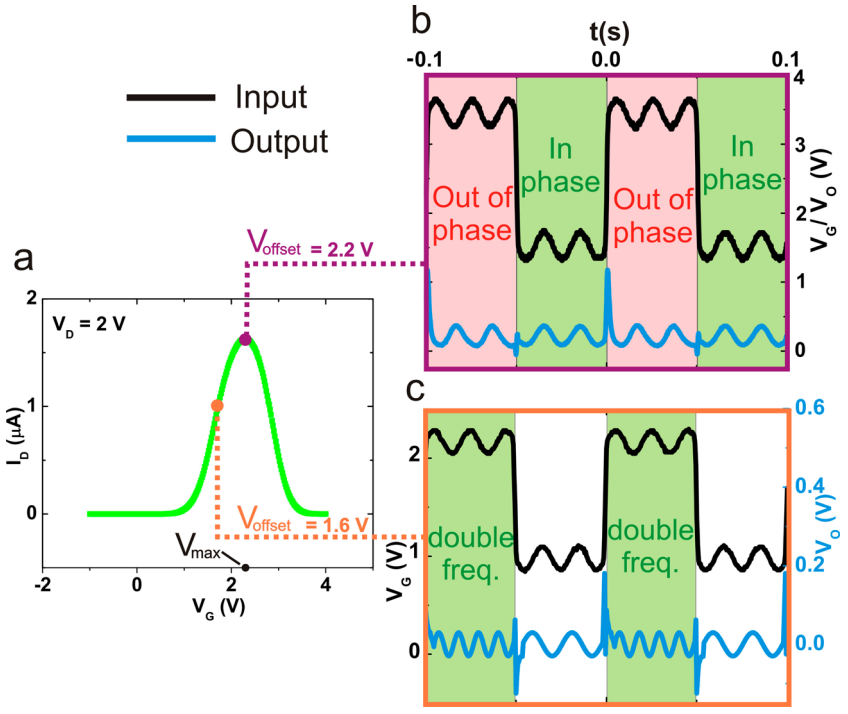

Figure 5. Phase and frequency shift keying using s-SWCNT/a-IGZO antiambipolar p−n heterojunctions. (a) Representative antiambipolar transfer characteristic with the voltage offsets of the input signals (sine wave superimposed on modulating square waves) indicated by the differently colored circles. (b) Binary phase shift keying (BPSK) operation using a square + sine input (black) with a voltage offset corresponding to V_{max}. The output sine wave (blue) shows a phase shift compared to the input sine wave for each half of the square wave modulation. (c) Binary frequency shift keying (BFSK) operation using a square + sine input (black) with a voltage offset away from the current maximum as indicated by the red circle in panel a. The frequency of the output signal (blue) is doubled for every alternate modulation of the square wave.

IGZO. Four steps of photolithography were used to (1) define Mo (100 nm) electrodes; (2) define a-IGZO channels using oxalic acid (10% in water); (3) define Ti/Au (2 nm/50 nm) electrodes; and (4) define s-SWCNT channels via reactive ion etching (RIE) in O_2. After the final step of s-SWCNT RIE etching, the devices were immersed in *N*-methyl-2-pyrrolidone at 80 °C for 40 min to further remove photoresist and other photolithography residues. All electrical measurements were performed under ambient conditions in the dark using source-meter (Keithley 2400), waveform generator (Agilent 33500B), and oscilloscope (Agilent 54624A) instrumentation. The gate voltage was limited to 4 V on the positive side to avoid irreversible breakdown of the hafnia dielectric.

Structural Characterization of Devices. All atomic force microscopy (AFM) images were acquired in tapping mode using a Bruker Dimension ICON system. Scanning electron microscopy (SEM) images were acquired with Hitachi SU8030 system at 2 kV using the secondary electron detector.

■ ASSOCIATED CONTENT

Supporting Information

Additional details on material synthesis and electrical characterization. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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