

Fast Characterization of PBTI and NBTI Induced Frequency Shifts under a Realistic Recovery Bias Using a Ring Oscillator Based Circuit

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Abstract—A ring oscillator based circuit for separately characterizing PBTI and NBTI induced frequency shifts is demonstrated in a high-k metal gate process. The proposed design, for the first time, supports AC stress with a realistic recovery condition. Other benefits over the previous works include sub-400 nanosecond measurement time, sub-picosecond resolution and a simple calibration procedure. Detailed stress and recovery measurements under different voltage and temperature test conditions are presented and analyzed.

Keywords – Aging; high-k metal gate; positive bias temperature instability (PBTI); negative bias temperature instability (NBTI)

I. INTRODUCTION

Positive Bias Temperature Instability (PBTI) has become equally significant compared to Negative Bias Temperature Instability (NBTI) in high-k metal gate technologies. Due to the difference in their physical origin, the magnitude and behavior of PBTI and NBTI can be drastically different. Hence, there has been a growing need to develop test

structures that are capable of separately characterizing the circuit level impacts from these two aging mechanisms.

Ring oscillator (ROSC) has been widely used to characterizing the device level impact on logic delay degradation due to its simplicity. To separately characterize each of the two BTI effects, a modified ROSC design was proposed which uses a keeper circuit to isolate the stress in each stage (Fig. 1) [1]. In this implementation, AC stress can be applied by toggling the V_{DD} and ground signals but this limits the stress frequency to a few MHz. This limitation was addressed in subsequent design which applies the AC stress to the header or footer [2]. However, there are three major drawbacks in both previous works. First and foremost, neither design can achieve the correct recovery bias in Fig. 2 whereby the source-to-gate voltage is zero while the source-to-drain voltage is high. Providing a recovery bias that is closer to reality is particularly important given that a larger V_{ds} has proven to enhance recovery [3]. Secondly, a simple counter based scheme results in significant unwanted recovery due to

	[1]	[2]	This work
ROSC Stage Diagram (NBTI Stress Mode Shown)			
Stress Capability	DC No AC data	DC Unrealistic AC (i.e. $V_{ds}=0$)	DC Realistic AC (i.e. $V_{ds}=-V_{STR}$)
Meas. Scheme	Simple counter	Simple counter	Beat frequency scheme with phase alignment
*Meas. Time for 0.01% Resolution	10,000 ROSC periods	10,000 ROSC periods	100 ROSC periods (<1 μ s)
Use Condition Test Data	No (poor resolution)	No (poor resolution)	Yes (high resolution)
Result Credibility	Stressed devices do not have switching input during transition	Stressed devices do not have switching input during transition	Delay caused by additional unstressed switches can be simply calibrated out

Figure 1. Comparison of ROSC based circuits for separately monitoring NBTI and PBTI induced frequency shifts.

II. ROSC BASED MONITOR WITH REALISTIC RECOVERY BIAS

	PMOS		NMOS	
	Stress Mode	Recovery Mode	Stress Mode	Recovery Mode
Actual				
Ref [1] & [2]				
This work				

Figure 4. PMOS and NMOS bias conditions in stress and recovery modes. An actual inverter has a V_{ds} of V_{DD} in recovery mode, but previous monitor designs fail to capture this as V_{ds} is typically set as 0V.

the long measurement times. Lastly, the additional switches for providing stress bias to the Devices Under Test (DUT) affect the circuit delay corrupting the aging measurement data. In this work, we address these issues by proposing a PBTI/NBTI odometer which supports a realistic recovery bias, sub- μ s measurement time, sub-ps resolution, and simple calibration that eliminates the impact of the additional switches on the measurement data.

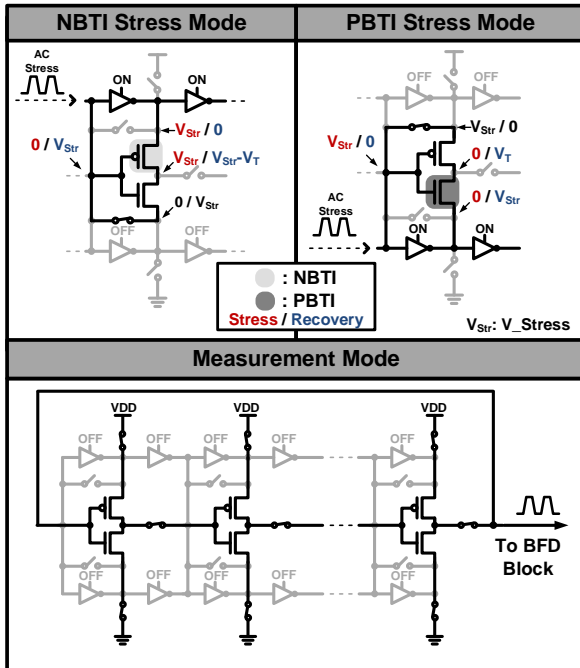


Figure 3. Operation modes of the proposed PBTI/NBTI odometer. Additional drivers and pass gates are used to apply realistic AC stress biases. Their delays can be calibrated out as shown in Fig. 18. Degradation in the supporting drivers does not affect the data since those circuits are switched off during measurement mode.

In order to separately stress the NMOS and PMOS transistors, we utilize two sets of tri-state drivers and switches between the gate and source of PMOS and NMOS in each inverter stage as shown in Fig. 3. For NBTI stress, a V_{gs} bias is applied to all PMOS devices while the gate and source voltages of NMOS devices are shorted. By doing so, all NMOS devices are kept fresh while the PMOS devices undergo AC stress. Note that we allow a V_t drop to occur in the V_{ds} bias during recovery mode since otherwise the circuit structure had to become overly complicated. In measurement mode, degradation in the additional drivers and switches will not affect the main path delay as those devices are switched off. The beat frequency detection scheme [4, 5] is adopted for fast characterization of BTI. As shown in the block diagram (Fig. 4), a flip-flop measures the frequency difference between the stressed and reference ROSCs. The final output count corresponds to the number of reference ROSC periods constituting a single beat period. The beat frequency detection scheme is particularly sensitive when the two ROSC frequencies are closer to each other. For instance, when the frequency difference between the two ROSCs increases from 1% to 2% due to aging, the output count changes from 100 to 50, as illustrated in Fig. 4. Conversely, a count change from 100 to 99 translates into a 0.01% shift in the ROSC frequency. The high resolution beat frequency based sensing scheme allows our test circuits to achieve a sub-ps delay measurement resolution with sub- μ s measurement time.

To further reduce the measurement time, a phase alignment technique was used in the test vehicle design. In the previous odometer designs [4, 5], the phase difference between the stressed and reference ROSCs signals was unknown when they start to oscillate, resulting in an arbitrary first beat frequency count. This increases the measurement interruption time by at least 2 times as the monitor has to wait for the valid second count to be measured. To overcome this limitation, a simple phase alignment scheme shown in Fig. 5 was employed. The STR_EN signal presets the stressed and the reference ROSC inputs to '0', regardless of the previous state. After a short delay period to ensure all internal signals are stable for each ROSC stage, the tri-state inverters driving both

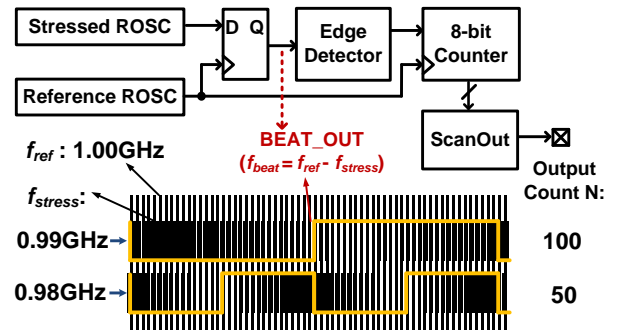


Figure 2. Principle of beat frequency detection technique adopted in this work. By measuring the beat frequency rather than the raw frequency, the measurement resolution can be greatly enhanced (e.g. <math><1\text{ps}</math>) while minimizing the measurement time (e.g. <math><1\mu\text{s}</math>).

ROSC inputs are switched to a high-Z state (i.e. RO_EN=0), while at the same time the two ROSC loops are closed to trigger an oscillation. The frequency outputs of the stressed and reference ROSCs are tapped out from the first and third stages, respectively. This way, the rising edge of the faster reference ROSC signal will always overtake the output of the slower stressed ROSC after a few delay stages, reducing the beat frequency measurement time from over a microsecond to less than 400 nanoseconds.

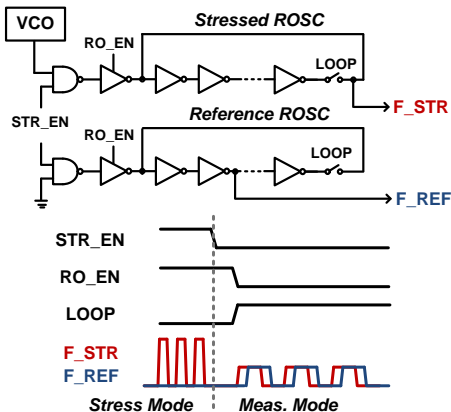


Figure 7. Phase alignment technique to reduce measurement time. The small initial phase difference between F_STR and F_REF guarantees the first count from the beat frequency detection block is valid.

III. PBTI AND NBTI MEASUREMENT RESULTS

A test chip was implemented in a high-k metal-gate process (Fig. 6). We first measured the frequency degradation induced by PBTI and NBTI separately under DC stress. Experimental data in Fig. 7 show that PBTI and NBTI induced frequency shifts closely follow a power law dependency on stress time. Measurements taken for stress times shorter than 1 millisecond reveal that time slopes can change during the course of the stress experiment. The magnitude of PBTI is 5X to 10X larger than that of NBTI at any given stress time for this process.

The time exponent value n extracted from the data in Fig. 5 for PBTI ranges from 0.09 to 0.12, which is slightly lower than the values reported in [2, 6, 7]. This can be attributed to the short measurement time of the proposed monitor circuit

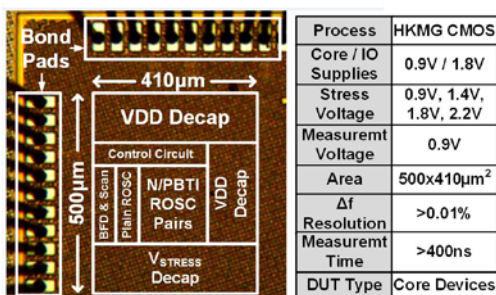


Figure 8. Testchip die photo and chip feature summary. The chip was fabricated in a high-k metal-gate process.

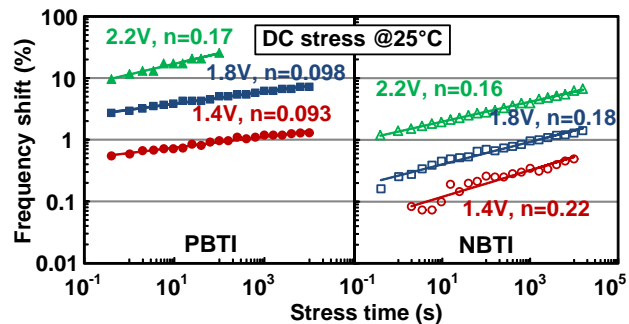


Figure 5. Measured PBTI and NBTI induced frequency shift under different DC stress voltages.

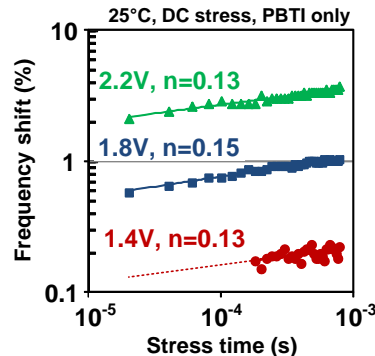


Figure 6. Short term frequency measurement results under DC PBTI stress.

which eliminates the unwanted recovery in the early stress sample points resulting in a lower overall n value [5, 9]. In order to characterize the impact of the measurement time on the overall frequency degradation, we conducted a series of stress tests using measurement interrupt times ranging from 400ns to 5000 μ s as shown in Fig. 9 (a). This was achieved by switching the supply to a nominal V_{DD} and waiting for a predetermined time before taking measurements. Experimental data in Fig. 9 shows that for longer measurement times, the frequency degradation magnitude is reduced while the time exponent n is increased due to unwanted recovery present during measurements. This becomes particularly noticeable for measurement times greater than 50 μ s. A dramatic change for n was observed between 50 μ s and 100 μ s as shown in Fig. 9 (b), which indicates the time constant for the recovery mechanism is in that range. It is observed that the time slope for PBTI increases with increasing stress voltage, while the opposite trend was seen for the NBTI case.

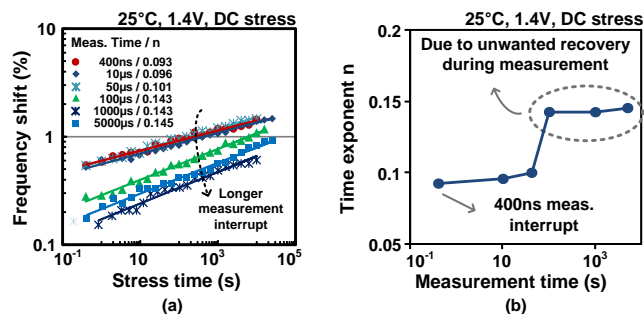


Figure 9. (a) PBTI induced frequency shift vs. stress time measured using different measurement times. (b) Time exponent n vs. measurement time.

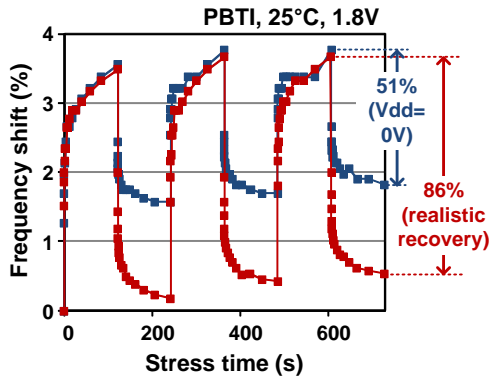


Figure 11. Periodic stress/recovery measurement results for power down and realistic recovery.

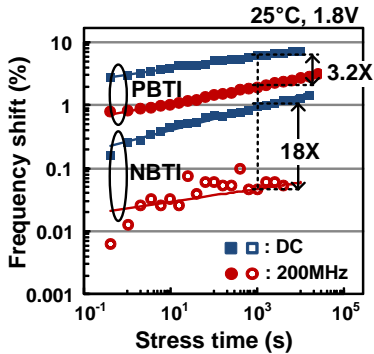


Figure 12. Comparison between DC and AC stress data.

Repetitive stress-recovery sequences under two different recovery modes are compared in Fig. 10. Here, the realistic recovery is when a transistor is in an off state as given in Fig. 2, while the power down mode is when the supply is completely shut down. The realistic recovery bias gives a significantly stronger recovery rate compared to the power down case (86% vs. 51% after the third cycle), which can be attributed to the accelerated recovery induced by the larger V_{ds} [3, 6, 9]. The stronger recovery under a realistic AC stress can also be seen in the DC to realistic AC stress frequency shift ratio in Fig. 11. The measured ratio for PBTI and NBTI were 3.2X and 18X, respectively. PBTI shows a smaller DC to AC ratio as compared to NBTI which is consistent with previous reports [7, 8]. Frequency shift measurements under a 200 MHz AC stress for different stress voltages are shown in Fig. 12 indicating that the PBTI time slope has a stronger voltage

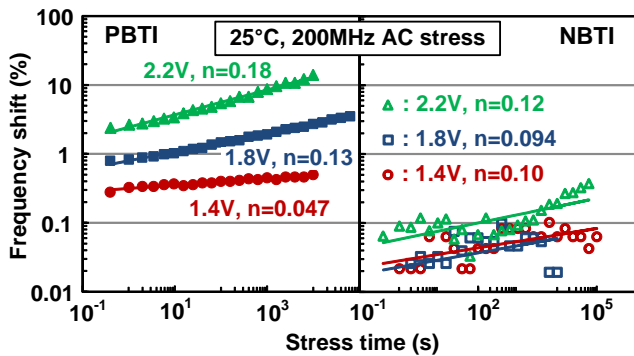


Figure 14. Measured PBTI and NBTI induced frequency shift under a 200MHz AC stress at different voltages.

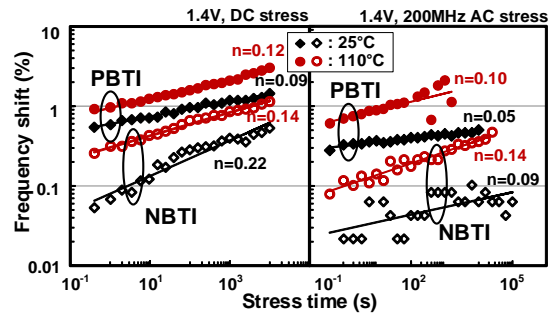


Figure 10. DC and AC stress data at 25°C and 110°C. The circuit was stressed at 1.4V and measured at 0.9V.

dependence compared to the DC stress case.

Frequency shifts measured at two different temperatures (25°C and 110°C) are plotted in Fig. 13, from which we can see that NBTI is more sensitive to temperature compared to PBTI. At 110°C, which is the worst case operating temperature for logic circuits, the temperature acceleration effect for AC BTI is more severe compared to the DC case. In particular, the power law exponent increases with temperature in AC stress case for both PBTI and NBTI, suggesting the temperature dependency of time slope is more significant for short term aging.

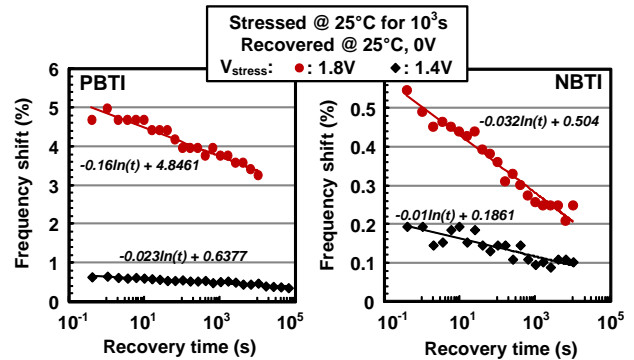


Figure 13. Frequency shift for PBTI and NBTI after the stress voltage is shut down. The recovery follows a $-\log(t)$ dependence. The time slope depends on the stress voltage.

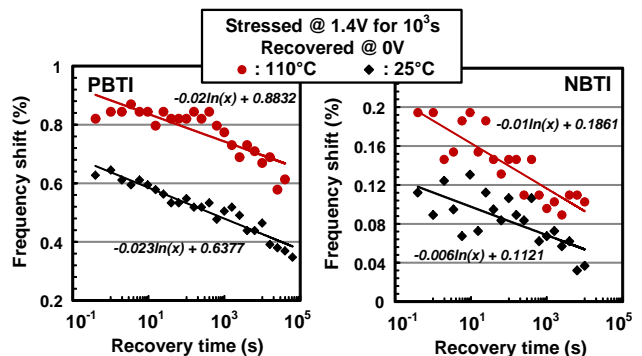


Figure 15. Frequency shift recovery data for two different temperatures. Recovery time slope shows a weak dependence on temperature.

The frequency shift relaxation during long term recovery in power off mode roughly follows a $-\log(t)$ curve for both PBTI and NBTI for the given recovery conditions in Fig. 14 and Fig.

15. Both the magnitude and time slope for recovery increase with stress voltage, which is consistent with data presented in [6, 9]. Fig. 15 shows that recovery has a weak dependence on temperature which is in line with previous observations [6, 10]

IV. CALIBRATION METHOD TO CALCULATE PLAIN ROSC DEGRADATION

In the proposed inverter design, additional switches and pass gates are used to separate the impact of PBTI and NBTI. For accurate aging estimation of logic circuits, it is important to calibrate out any systematic error introduced by the additional switches.

The schematic of the modified inverter stage used in this design and the plain inverter stage is compared in Fig. 16. The propagation delay of a standard inverter stage can be expressed using the Elmore delay model as follows:

$$t_d \propto (R_p + R_n)C_L \quad (1)$$

where R_p and R_n are equivalent resistance of PMOS and NMOS during transition, C_L is the load capacitance at the output node.

The NBTI and PBTI induced shift can be expressed using the change in equivalent transistor resistance, namely ΔR_p and ΔR_n . The drive currents of NMOS and PMOS are typically equalized by proper sizing, i.e. $R_p=R_n=R_{eq}$. The resulting percentage delay shift of the plain inverter is:

$$\frac{\Delta t_{inv}}{t_{inv}} = \frac{\Delta R_p + \Delta R_n}{2R_{eq}} \quad (2)$$

Next, we derive the expression for the propagation delay of the proposed design. In the measurement mode, the additional switches are turned on, so the total main path delay can be expressed as:

$$t_d = R_{xg}C_3 + (R_p + R_n + R_h + R_f)(C_2 + C_3) + (R_h + R_f)(C_1 + C_2 + C_3) \quad (3)$$

Here, R_h and R_f are the drive resistances of the header PMOS and footer NMOS, respectively. C_1 , C_2 and C_3 are the capacitances denoted in Fig. 16. R_{xg} is the drive resistance of the transmission gate connected to the inverter output.

After stress, either R_p or R_n is shifted by ΔR_p or ΔR_n , and all the other devices are in an off-state thus free of any BTI stress during the stress mode. Assuming the equalized pull-up and pull-down delay, i.e. $R_p=R_n=R_{eq}$, $R_f=R_h=R_{sw}$, the percentage delay shift caused solely by PBTI can be written as:

$$\frac{\Delta t_{PBTI}}{t} = \frac{\Delta R_p(C_2 + C_3)}{R_{xg}C_3 + (R_{sw} + R_{eq})(C_2 + C_3) + R_{eq}(C_1 + C_2 + C_3)} \quad (4)$$

while the NBTI only delay shift:

$$\frac{\Delta t_{NBTI}}{t} = \frac{\Delta R_n(C_2 + C_3)}{R_{xg}C_3 + (R_{sw} + R_{eq})(C_2 + C_3) + R_{eq}(C_1 + C_2 + C_3)} \quad (5)$$

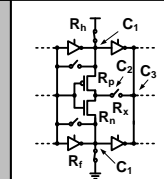
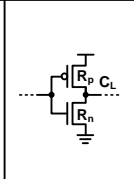
Schematic		
Measurable	$(\frac{\Delta f}{f})_{PBTI}, (\frac{\Delta f}{f})_{NBTI}$	$\frac{\Delta f}{f}$
Relationship	$\frac{\Delta f}{f} = \beta [(\frac{\Delta f}{f})_{PBTI} + (\frac{\Delta f}{f})_{NBTI}]$	
β	$\frac{1}{(R_h + R_f)(C_2 + C_3) + R_{eq}(C_1 + C_2 + C_3) + (R_h + R_p + R_f + R_n)(C_2 + C_3) + R_g C_3}$	

Figure 17. Overall degradation of a plain ROSC can be calculated using the separate PBTI and NBTI data by calibrating out the delay coefficient factor β introduced by the additional pass gates and switches.

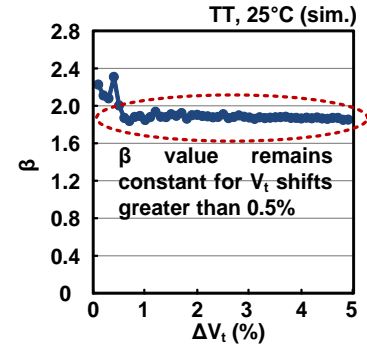


Figure 16. HSPICE simulation results show that β is independent of threshold voltage shift induced by aging.

Examining equations (2), (4), and (5), the percentage delay shift of a plain ROSC can be expressed as the sum of the PBTI and NBTI shifts from the proposed circuit as follows:

$$\frac{\Delta t_{inv}}{t_{inv}} = \beta \left(\frac{\Delta t_{PBTI}}{t} + \frac{\Delta t_{NBTI}}{t} \right), \quad (6)$$

where, the constant prefactor β is the ratio between the combined PBTI/NBTI delay shift and the plain ROSC delay shift, representing the additional delay introduced by the pass gates.

$$\beta = \frac{R_{xg}C_3 + (R_{sw} + R_{eq})(C_2 + C_3) + R_{eq}(C_1 + C_2 + C_3)}{\alpha R_{eq}(C_2 + C_3)} \quad (7)$$

Here, $\alpha=1$ for AC stress and $\alpha=2$ for DC stress. For DC stress, alternating PMOS and NMOS devices are stressed along an actual logic path, while each PMOS or NMOS is stressed in the proposed ROSC design. This discrepancy can be accounted for by setting α to be 2. For AC stress however, every single device undergoes stress for both ROSC designs and hence α should be equal to 1.

β is independent of aging as suggested by the above Elmore delay calculation as well as simulation results. HSPICE simulation results in Fig. 17 shows that the β value is almost constant for V_t shifts greater than 0.5%. A plain ROSC was implemented in the same test chip in order to experimentally obtain the β value. The frequency shift results

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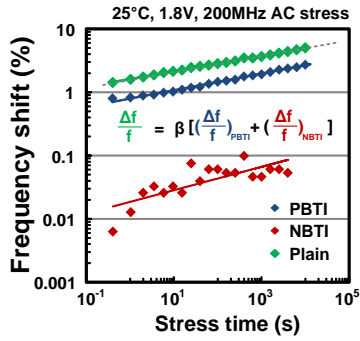


Figure 18. The β value can be calculated based on measurement data from the PBTI/NBTI RO SC and standard RO SC.

for the plain RO SC, and the proposed circuit are measured from the same die under a 1.8V, 200MHz AC stress condition at 25°C. The results displayed in Fig. 18 indicate that the β value is indeed insensitive to the amount of stress applied to the circuit as theoretically predicted by (7). The β value extracted from measured data can be readily used to translate the individual PBTI and NBTI frequency data to the plain RO SC frequency shift.

V. CONCLUSIONS

PBTI and NBTI effects are different in terms of physical origin, magnitude, voltage and temperature dependencies, etc., and hence their impact on circuit performance must be characterized and analyzed separately. In this work, we demonstrated a RO SC based on-chip monitor circuit capable of separately characterizing the impact of PBTI and NBTI on logic circuit frequency. Furthermore, the realistic recovery condition is taken into account for the first time by using a special RO SC structure. The proposed monitor has other major advantages over previous designs such as ultra-short 400ns measurement interrupt and picosecond order timing resolution. Experimental data from test chips built in a high-k metal gate technology verifies that both PBTI and NBTI induced frequency shifts follow the power law dependence (t^n) on stress time. The time exponent n measured from our test chips was smaller than previously reported values presumably due to the short measurement time. PBTI in this particular technology was 5X to 10X larger than NBTI with a smaller recovery rate. Recovery follows a $-\log(t)$ dependency which was consistent across different stress voltages and temperatures. A stronger recovery effect was observed when a realistic drain-to-source bias was applied confirming our hypothesis.