Silicon Odometers: Compact In Situ Aging Sensors for Robust System Design

This article reviews several test-chip designs that demonstrate the benefits of utilizing on-chip logic and a simple test interface to automate circuit aging experiments. This new class of compact on-chip sensors can reveal important aspects of circuit aging that would otherwise be impossible to measure, facilitate the collection of reliability data from systems in the field, and lead us to real-time aging compensation in future processors.

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Circuit failure due to device aging mechanisms, such as bias temperature instability (BTI), hot carrier injection (HCI), time-dependent dielectric breakdown (TDDB), electromigration (EM), and random telegraph noise (RTN), has become increasingly problematic with shrinking device geometries and smaller voltage margins. Traditionally, designers have dealt with this problem by adding a conservative frequency guardband based on the worst-case degradation scenario. The semiconductor industry has used guardbanding extensively to mitigate lifetime issues; however, the associated power and performance overhead is expected to increase in future process technologies. The circuit and architecture communities have been exploring an alternative design paradigm based on in situ aging monitors that could fundamentally change the way we deal with lifetime issues in future processors. Figure 1 illustrates the overall concept, in which a feedback loop triggered by a collection of aging sensors proactively compensates for any wear-out issues the system experiences. Researchers have studied implementation of the compensation circuit itself (for example, dynamic voltage and frequency scaling), so the recent effort has focused on designing accurate and compact monitor circuits or developing architecture-level mitigation strategies.[1]

This article focuses on a series of on-chip reliability monitors designed by our group that can provide several important benefits that would otherwise be impossible to achieve using previous designs (for more information on earlier work in on-chip aging monitors, see the "Related Work in On-Chip Reliability Monitoring" sidebar). Those benefits are picoseconds timing resolution for usage condition stress, microsecond measurement interrupt to prevent unwanted recovery, and excellent immunity to voltage and temperature drifts. The proposed odometer designs use standard logic gates and a simple

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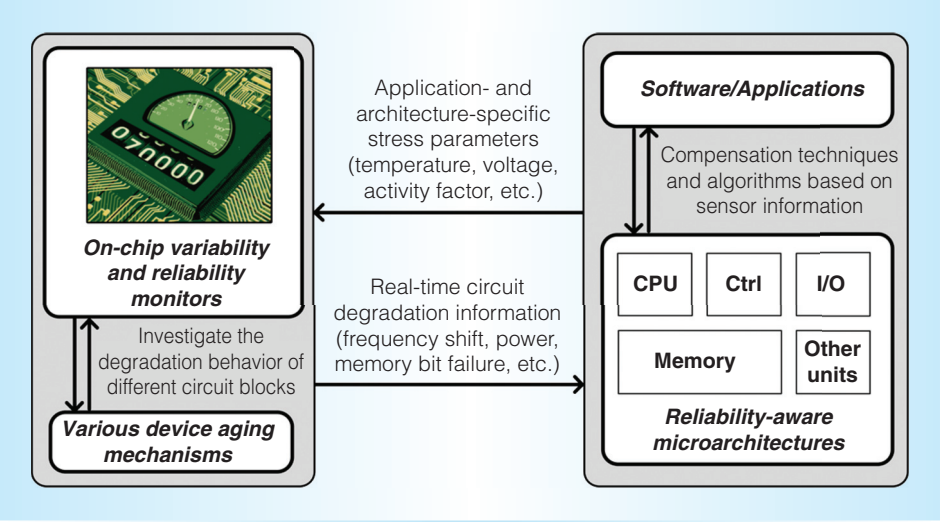

Figure 1. A cross-layer aging-compensation framework based on in situ reliability monitors. On-chip aging sensors provide real-time circuit degradation information that could trigger the compensation of aging at the architecture and application level.

scan-based interface, so they are suitable for integrating into an actual processor system. In this article, we refer to our proposed circuits as silicon odometers, because they are analogous to odometers in cars that indicate the wear and tear on the vehicle. Since we embarked on this project, we have implemented eight unique odometer designs in six test chip projects in process technologies ranging from 130 nm down to 32 nm. We will review six of the eight odometer designs in this article.

Design considerations

Although this article focuses on introducing the innovative features of each odometer design and demonstrating their circuit-level capabilities (see Figure 2), it is worth mentioning the various design considerations and practical issues designers must consider when applying these sensors to a real processor system (see Table 1). These issues include, but are not limited to, the type of aging mechanism, the temporal and spatial granularity of the measurements, stress and measurement condition, firmware design, test methodology, and sensor calibration. Most of these design parameters can be readily determined once the system-level requirements, the area budget, and the interface protocol are known.

Table 1 shows the actual design parameters used for an aging monitor system recently deployed in IBM zEnterprise 196 mainframe systems aimed at in-field data collection. To the best of our knowledge, this is the first time an on-chip reliability monitor system was used in a commercial product, and it therefore serves as a useful guideline for future odometer system designs. In this design, aging data was collected every week from five ring-oscillator-based sensors located across the die that were exposed to the same stress pattern as the main processor chip. One challenge we faced was that unlike in a lab environment where the stress can be precisely controlled, the initial fresh frequency difference between the reference and stressed circuits could not be measured until the system was due for its first check-up routine. This so-called time zero problem and other practical issues could pose interesting test and calibration challenges for this emerging class of on-chip monitors.

CMOS reliability mechanisms

Before we delve into the various odometer circuits' details, we briefly review the four major CMOS device reliability mechanisms that our research has focused on.

BTI is characterized by a positive shift in the absolute value of the metal-oxide-

Related Work in On-Chip Reliability Monitoring

Researchers have proposed several aging-measurement systems in the past decade to demonstrate the effectiveness of using compact on-chip circuits for reliability monitoring. Karl et al. designed two separate compact circuits to measure negative-bias temperature instability (NBTI) and time-dependent dielectric breakdown (TDDB) for real-time characterization.[1] A monitor by Singh et al. captures the onset of TDDB using test chip data and an empirical formula.[2] Hofmann et al. measured bias temperature instability (BTI) and hot carrier injection from critical-path circuits using a single-ended ring-oscillator-based system.[3] Saneyoshi et al. and Chen et al. proposed monitors for measuring the BTI impact on logic delay.[4,5] Kim et al. proposed a method to separate positive-bias temperature instability (PBTI) and NBTI impact on frequency degradation in a high-*k* metal gate (HKMG) process.[6] More recently, Lu and Jenkins presented details of a ring-oscillator-based reliability sensor that was successfully deployed in IBM z196 servers.[7] That work reported product aging data collected for an operation period of over 500 days.

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semiconductor field-effect transistor (MOSFET) threshold voltage (V_t), which occurs when a device is biased in strong inversion (when the channel is formed). The V_t shift is generally attributed to hole or electron trapping in the dielectric bulk, and/or to the breaking of silicon-hydrogen bonds at the gate dielectric interface by holes in the inversion layer, which generates positively charged interface traps for *p*-channel MOS (PMOS) (see Figure 3a). When a stressed device is turned off, it immediately enters the recovery phase, where trapped holes are released, thereby reducing the absolute value of the V_t. HCI degradation appears when a large drain-to-source voltage and gate-to-source voltage is applied (Figure 3b). Hot carriers (that is, those with high kinetic energy) accelerated toward the drain by the corresponding lateral electric field across the channel create traps at the silicon substrate and even inside the gate dielectric interface, as well as dielectric bulk traps, and hence degrades device characteristics such as V_t. RTN is generally understood as the random capturing and emitting of carriers by traps in gate-oxide, as Figure 3c shows. The V_t consists of sudden step-like fluctuations between two or more discrete voltage levels. High voltage on the gate can create traps within the dielectric. These defects could eventually join together and form a conductive path through the stack in a process called TDDB, or oxide breakdown (Figure 3d).

Original silicon odometer: Detecting beat frequency

For accurate and efficient characterization of reliability mechanisms, an odometer circuit must be capable of measuring extremely small shifts in operating frequency within a short measurement time. For a typical stress experiment, the stress voltage applied to the monitor circuit during long stress periods is briefly lowered using on-chip power gates to

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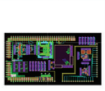
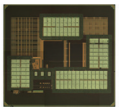
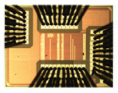
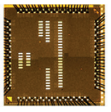
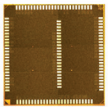
Die photo						
Process	130 nm	65 nm	65 nm	65 nm	32 nm	32 nm
Odometer projects	Original silicon odometer	All-in-one odometer	Statistical, duty-cycle, and RTN odometer	Interconnect odometer	PBTI and SRAM odometer	SRAM and RTN odometer
Focused reliability issues	NBTI-induced frequency degradation	Separately monitoring NBTI, HCI and TDDB	Statistical behavior of NBTI; RTN on logic circuit	Impact of interconnect on BTI and HCI aging	Monitoring PBTI in HKMG process; BTI impact on SRAM read/write	SRAM timing issues due to BTI; RTN impact on ring oscillator

Figure 2. Past odometer test chips from our group. We implemented the eight odometer designs in six test chip projects focusing on characterizing the impact of different aging mechanisms on circuit performance. These test chips are implemented in process technology nodes from 130 nm to 32 nm.

Table 1. Design considerations and practical issues of on-chip aging sensors. The right column shows details of a sensor implementation in an IBM z196 mainframe server.

Design considerations	Examples of practical issues	Aging sensor implementation in an IBM z196 server[2]
Type of sensor	Bias temperature instability (BTI), hot carrier injection (HCI), time-dependent dielectric breakdown (TDDB), random telegraph noise (RTN), transient errors, memory bit failures, and so on	Ring-oscillator-based BTI monitor for long-term frequency degradation measurement
Temporal granularity	Sensing period, threshold setting, dynamic range, and so on	Sampling period: once a week
Spatial granularity	Per CPU/GPU/memory, per functional unit, per sub-block, and so on	Total: five sensors per chip; one sensor per core (×4 cores) plus one sensor in the level-2 cache
Stress and measurement condition	AC versus DC, accelerated versus usage condition, fast measurement	AC stress, usage condition, 0.5-ms measurement time
Communication	Between data gathering sensors, across sensors, between sensors and processor	Sensors are integrated with IBM z196 pervasive infrastructure with firmware support
Interface and protocol	Interrupt based, polling, event alarms, performance counter based, and so on	Interrupt-based in-field frequency degradation measurement
Testing and calibration	Similar to any other on-chip monitor circuit	Time zero frequency shift unknown since first sample is taken after some stress

characterize the degradation at a nominal supply voltage. In order to capture the precise aging data before BTI recovery takes place, frequency measurements must be completed in a few microseconds. Furthermore, a practical aging monitor should also be fully digital, support various stress modes, occupy a small silicon area, use a simple test interface for

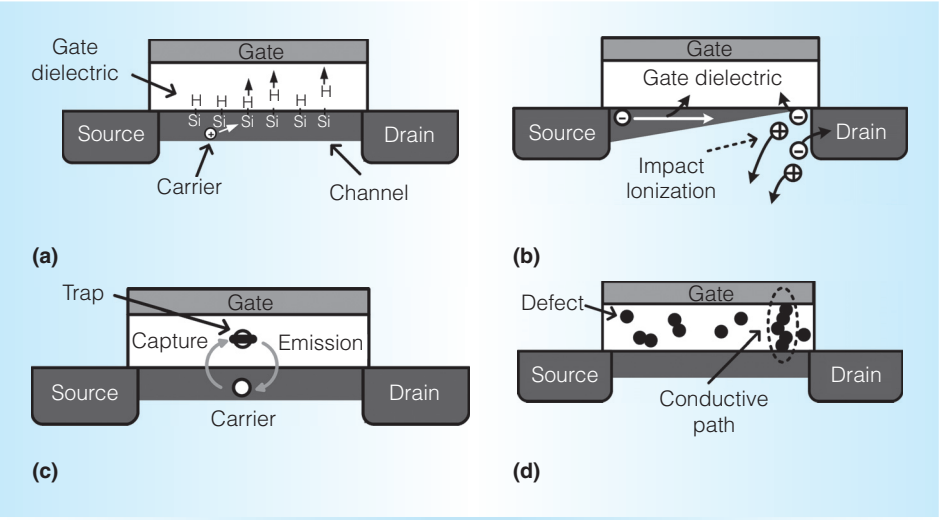


Figure 3. Transistor cross sections illustrating negative-bias temperature instability (NBTI) (a), HCI (b), RTN (c), and TDDB (d). Positive-bias temperature instability (PBTI) is equivalent to NBTI but occurs in an *n*-channel metal oxide semiconductor (NMOS) device.

convenient data collection, and allow independent characterization of the different aging mechanisms.

All these requirements can be met using a novel beat frequency detection concept (see Figure 4).[3,4] During the short measurement periods, a D-flip-flop uses a fresh reference *ring oscillator* (ROSC) to sample the output of an identically stressed ROSC. In this configuration, the stressed ROSC's output is sampled at every rising edge of the reference ROSC output, producing a signal that exhibits the beat frequency. The beat frequency is measured using a counter circuit clocked by the reference ROSC's output. This beat frequency count is recorded after each stress period to calculate the actual shift in the stressed ROSC frequency. Consider the example in Figure 4, where the frequency of the reference ROSC is 1 GHz and the frequency of the stressed ROSC degrades from 0.99 to 0.98 GHz. In this case, the count value changes from 100 to 50 for a 0.01-GHz (1 percent) shift in frequency, achieving an extremely high measurement sensitivity. Similarly, the frequency corresponding to a count change from 100 to 99 is just 0.0001 GHz (0.01 percent). Note that the measurement time, which is the product of the count and the ROSC period, is less than 1 microsecond in most of our designs, which practically eliminates any unwanted BTI recovery. Because the reference and stressed ROSCs are identical structures placed next to each other in the same power domain, the proposed monitor circuit has a high immunity to voltage and temperature drifts.

All-in-one silicon odometer: Separately monitoring HCI and BTI

To examine the contribution of HCI and BTI to overall circuit degradation, we devised an on-chip monitor capable of separating the two aging components. We used the backdrive concept,[5] in which only one ROSC ages from both BTI and HCI, whereas the other suffers only from BTI. We adopted the beat frequency detection method to take submicrosecond measurements to avoid unwanted device recovery during stress interruption. Figure 5 shows a block diagram of the proposed odometer for separately measuring HCI and BTI.[5] This circuit contains four ROSCs: two stressed and two unstressed (to maintain fresh reference points). Each stressed oscillator is paired with its identical, fresh reference during measurements, and its frequency degradation is monitored with the beat frequency detection circuit. The measured BTI- and HCI-

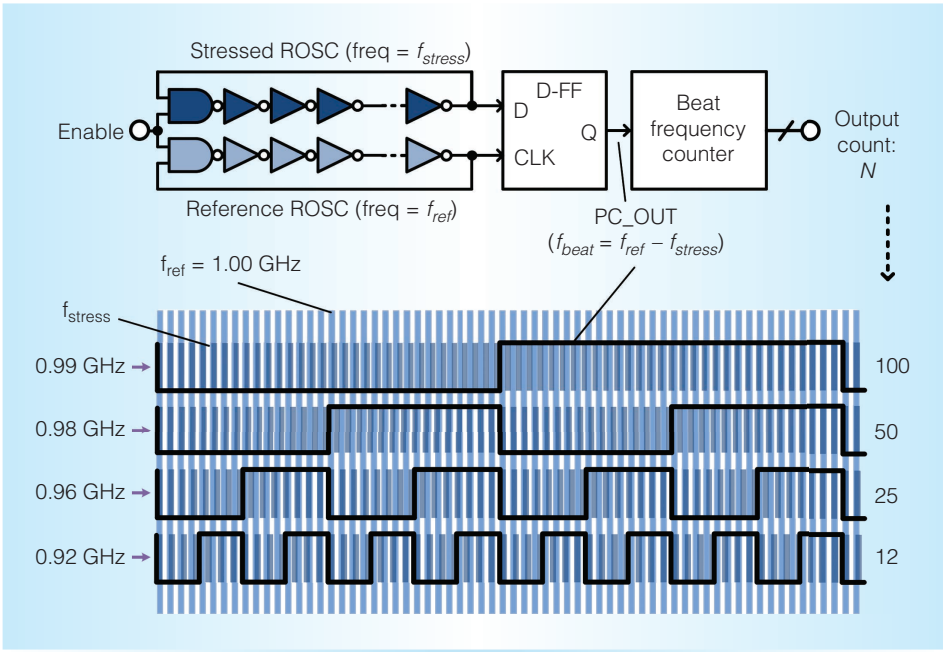


Figure 4. Concept behind the beat frequency detection system. Small frequency shifts induced by circuit aging are magnified by measuring a single ring oscillator's beat frequency (that is, Δf) rather than its raw frequency.

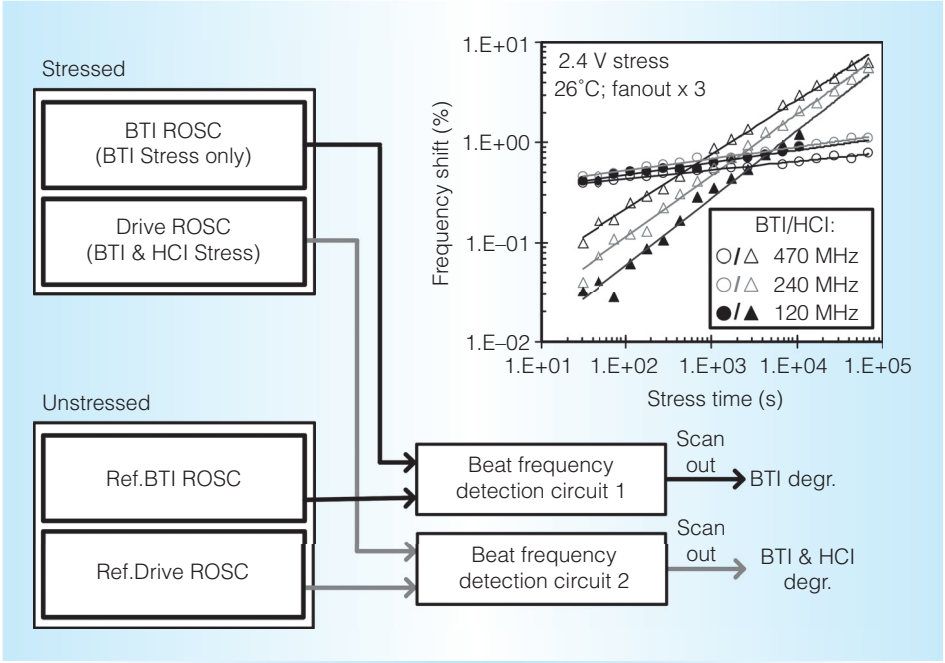


Figure 5. All-in-one odometer system for separately monitoring BTI- and HCI-induced frequency degradation. The inset shows measured data from a 65-nm test chip.

induced frequency degradations in Figure 5 show a power law dependency, with HCI dominating the overall aging at longer stress times because of its steeper time slope. Furthermore, the data measured at different AC stress frequencies confirms that BTI is at most weakly dependent on frequency, whereas HCI worsens at higher switching frequencies.

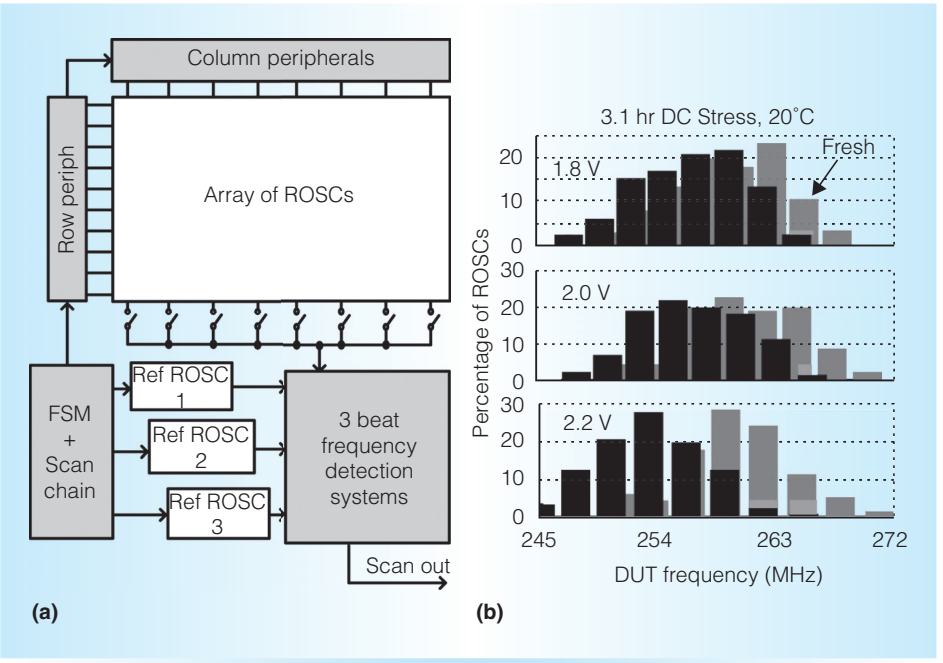


Figure 6. Statistical odometer for understanding aging variability. Top-level system diagram (a). The shift in frequency distributions can be efficiently measured using an array-based circuit (b).

Statistical odometer: Collecting aging variability data

Variability in transistor aging has received increasing attention as transistor dimensions approach the atomic scale.[6] In this section, we present the first array-based system to accurately study variations in aging involving BTI and HCI in stressed ROSC. This statistical odometer consists of a 10 × 8 array of cells containing ROSCs to be stressed, a finite state machine (FSM), a scan chain, and three beat frequency detection blocks with their reference ROSCs (Figure 6a).[7] The distribution of frequencies is monitored by a set of three beat frequency detection systems working in parallel. Unwanted BTI recovery during stress interruptions is avoided with measurement interrupts of ≤ 1 μs. Figure 6b shows distributions of fresh device-under-test (DUT) frequencies, with the resulting distributions after 3.1 hours of DC stress at different voltage levels.

Interconnect odometer: Studying impact on BTI and HCI

Interconnect fabrics used in clock networks, signal buses, networks on chip, memory wordlines and bitlines, and high-speed I/Os are critical components in modern integrated circuits. The BTI and HCI aging behavior of interconnect-dominated paths could drastically differ from that of logic-dominated paths because of the slow voltage transition and lower peak current. Understanding the impact of interconnect length on circuit degradation is critical in designing reliable interconnect circuits. To this end, we designed an odometer circuit based on the all-in-one concepts described earlier to uncover the dependence of BTI- and HCI-induced aging on wire length.[8] Figure 7a shows BTI-induced frequency shifts measured from the interconnect odometer chip for different interconnect lengths.[8] The amount of BTI aging decreases monotonically with longer interconnects for all three stress conditions. This can be explained by the longer transition time observed in longer wires, which translates into a shorter amount of time that the PMOS transistor is exposed to a full static BTI stress bias, or the *BTI duty cycle* as shown in Figure 7b. Figure 7c shows that HCI degradation has a nonmonotonic relationship with wire length. This phenomenon is explained by two competing factors:

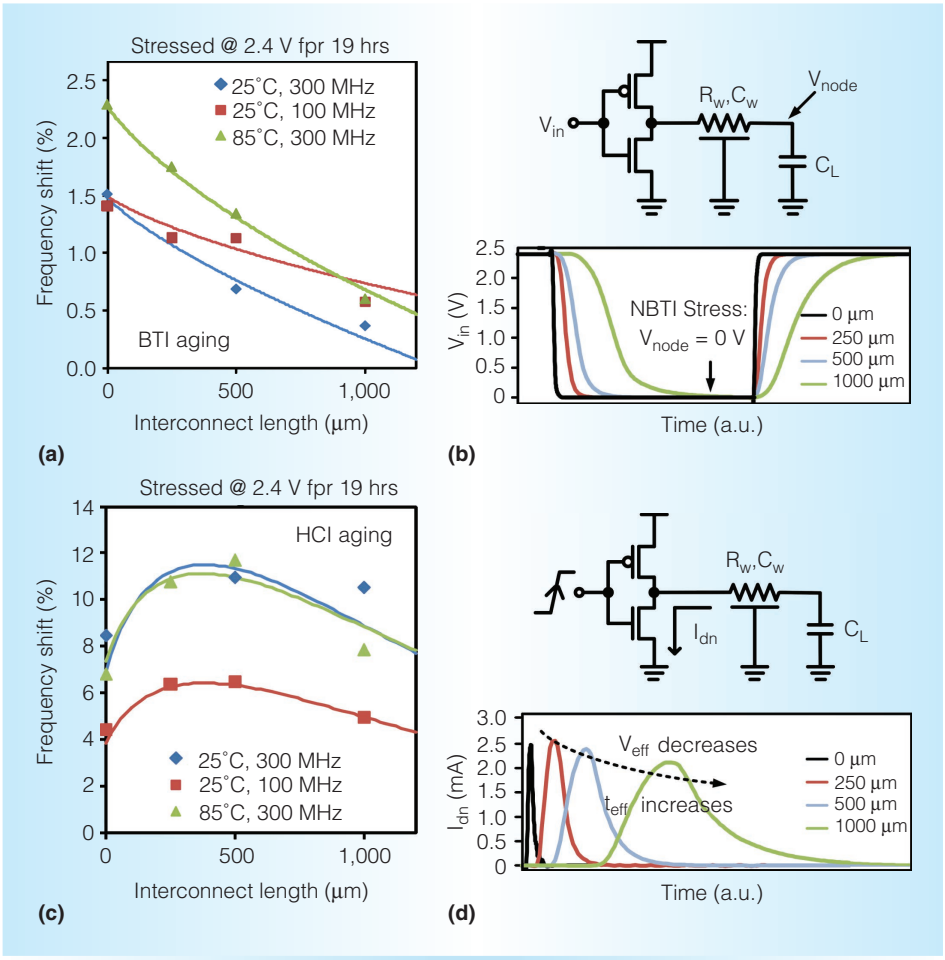


Figure 7. Interconnect length dependence of BTI and HCI aging. BTI-induced frequency degradation measured from the interconnect odometer (a). The smaller BTI degradation in drivers with longer interconnects can be attributed to the longer signal transition, which in turn reduces the effective stress time (b). Measured HCI-induced frequency degradation (c). The effective stress time increases in longer interconnects while the effective stress voltage decreases, resulting in a nonmonotonic HCI degradation characteristic (d).

a reduction of the effective stress voltage and the increase in current pulse duration, both with longer wire loads. A driver with a longer wire load has a smaller peak current due to the voltage division between the wire resistance and the driver's equivalent resistance, as shown in Figure 7d. The second factor contributing to this nonmonotonic characteristic is the wider current pulse caused by the increased RC loading of longer wires. A longer current pulse width results in a longer HCI stress time, which leads to a more-severe degradation for longer interconnects for the same effective stress voltage.

Duty-cycle odometer: Measuring duty-cycle degradation

Low-power static RAMs (SRAMs), dynamic register files, and domino gates rely on both the rising and falling edges of the clock to generate internal timing signals. Unlike flip-flop-based pipelines, where only the primary clock edge (such as the rising edge) is utilized, the performance of these circuits is directly affected by any change in the clock duty cycle. BTI stress in the clock signal path during idle or clock-gated mode results in an aging-induced duty-cycle shift, as Figure 8a shows in a typical clock-buffer chain scenario.

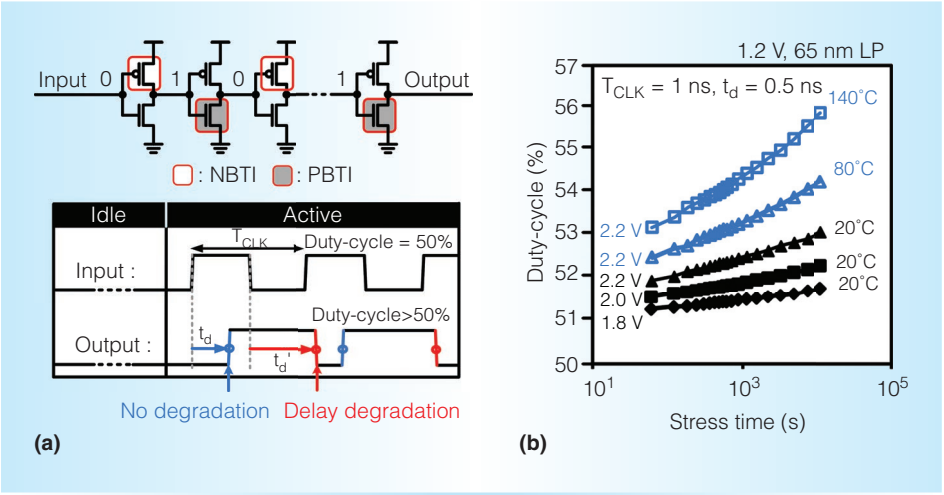


Figure 8. Duty-cycle degradation in a buffer chain due to alternating NBTI and PBTI stress. Asymmetric delay degradation of rising and falling edges results in duty-cycle shifts (a). Duty-cycle shift of a logic path under different stress voltages and temperature (b).

In an idle or clock-gated mode, the input clock signal is not switching, which results in a DC stress condition with negative-bias temperature instability (NBTI) and positive-bias temperature instability (PBTI) occurring in alternative gates. When the circuit is switched back to an active mode, the first rising edge of the clock propagates through unstressed fresh devices, whereas the second edge traverses through the stressed devices. Consequently, the delay of the second edge becomes longer compared to that of the first edge due to BTI under DC stress, resulting in a duty-cycle shift. We can use our beat frequency detection framework, which can measure a small amount of speed degradation in a ROSC, to estimate percentage change in the duty cycle of a clock driving a chain of inverters under stress.[9] Figure 8b plots duty-cycle shifts based on the odometer test chips under different stress conditions. The duty-cycle shifts increase with both stress voltage and temperature. For the inverter path with 500-ps delay driven by a 1-GHz clock, the duty cycle increases by up to 6 percent after 10,000 seconds of stress at 2.2 V and 140°C.

SRAM odometer: Evaluating memory read failures

BTI is a primary reliability concern in sub-32-nm SRAMs.[10] NBTI and PBTI under the DC stress condition that dominates in SRAM bitcells lead to an increase in the read bit failure rate (BFR) and a decrease in the write BFR.[11] Although there is a pressing need for an in situ statistical characterization of BTI on large memory arrays, the phenomenon of fast BTI recovery can lead to inaccurate results if the measurement time, T_{MEAS}, is not in the microsecond scale. The test structure we present here is the first to facilitate recovery-free evaluation of the progression of NBTI- and PBTI-induced degradation on an SRAM macro. Figure 9a shows the proposed SRAM reliability macro. Overall, SRAM-specific components are designed to be representative of a product subarray. The on-chip FSM and voltage-controlled oscillator handle the complicated part of the built-in self test, such as controlling the supply switches for measurement and stress modes, measurement times, pulse width control, read/write commands, and address sequencing. The off-chip signal analyzer handles the slower timings, such as scans and BFR readout. Figure 9b shows read BFR with stress time at different T_{MEAS}, showing expected degradation trends. A few-millisecond T_{MEAS} causes errors of as much as 10 to 100 times in terms of BFR, owing to the BTI recovery during the measurement period.

RTN odometer: Measuring frequency fluctuations

Parametric shifts caused by RTN have become a growing concern in extremely scaled

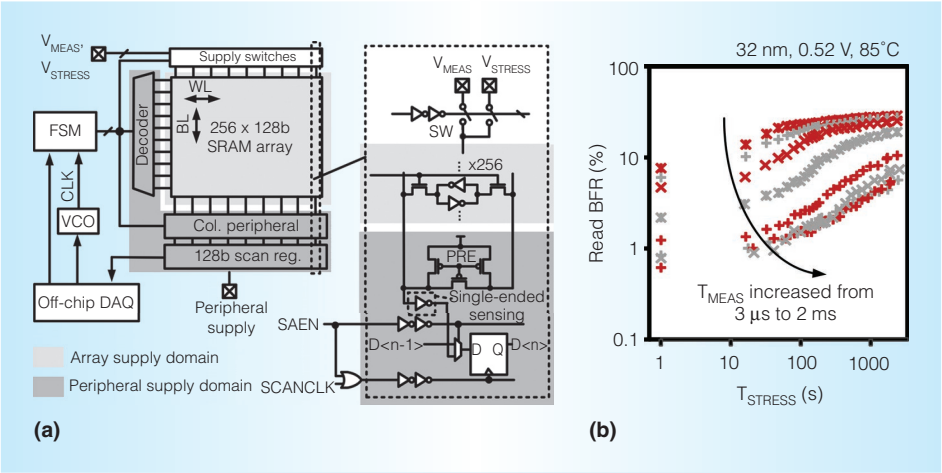


Figure 9. Static RAM (SRAM) odometer for characterizing bit cell failure. Chip diagram (a). Read bit failure rate (BFR) degradation measured using different measurement times (b).

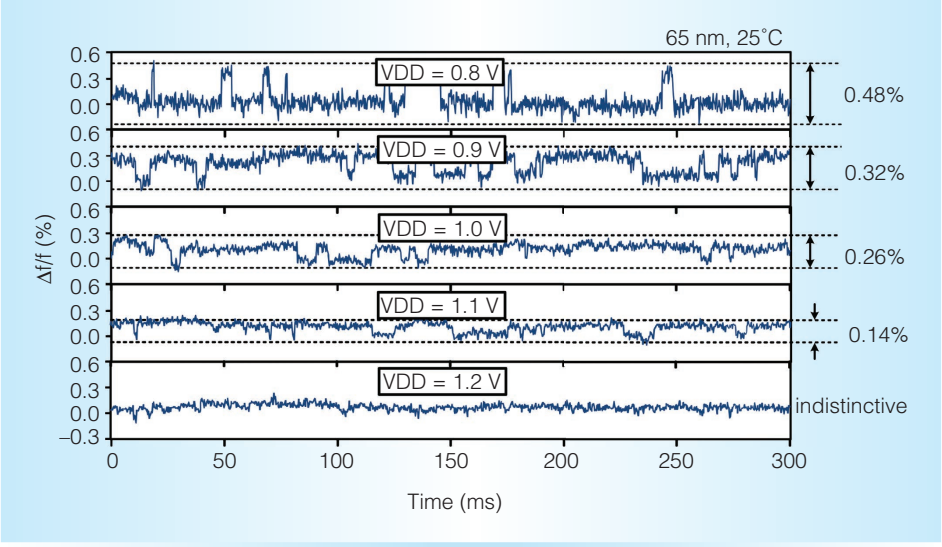


Figure 10. Frequency fluctuation due to RTN at different supply voltages. The amplitude of the frequency shift decreases with increasing V_{DD}. The capture time (the time in low-frequency states) and the emission time (the time in high-frequency states) have a positive and negative dependence on voltage, respectively.

CMOS circuits. However, researchers have made few attempts at assessing the true RTN impact in logic circuits. This, we believe, is primarily because of the difficulty of taking high-precision measurements in a short measurement time from realistic circuits such as ROSCs. Using the beat-frequency-based odometer circuit, which can measure frequency shifts with a resolution as high as 0.01 percent, RTN's signature trapping and detrapping behavior can be measured as shown in Figure 10.[12] The frequency shift caused by a single RTN trap was approximately 0.4 percent for the 11-stage ROSC operating at 0.8 V and 25°C. As the supply voltage increased from 0.8 to 1.1 V, the RTN-induced frequency shift decreased from 0.48 to 0.14 percent. We can clearly see that for the higher voltage, the ROSC tends to run at the low-frequency state, whereas as the voltage increases, the frequency is more likely to stay at the high-frequency state. Eventually, RTN becomes indistinctive at 1.2 V, the nominal operating voltage of this

process. These results are in line with previous studies that have reported a stronger RTN signal at lower supply voltages.[13]

We hope this article will give our colleagues in computer architecture and systems design an opportunity to learn about the latest work on our group's odometer project. Possible topics for our future odometer designs include focusing on emerging or deteriorating reliability mechanisms in next-generation multigate transistors; studying reliability implications of advanced power-management schemes, such as near-threshold computation, turbo mode operation, and fast dynamic voltage and frequency scaling; and understanding the impact of advanced fabrication techniques, such as double patterning, strain silicon, and plasma processing, on circuit reliability effects. MICRO

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