Scaling Analysis of In-plane and Perpendicular Anisotropy Magnetic Tunnel Junctions Using a Physics-Based Model

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Spin transfer torque magnetoresistive random access memory (STT-MRAM) technology has been gaining interest as an alternative to SRAM as it possesses unique properties such as nonvolatility, higher density, and good scalability. Magnetic tunnel junctions (MTJs) based on shape anisotropy, interface anisotropy and crystal anisotropy have been demonstrated with the common goal of reducing the switching current while maintaining sufficient nonvolatility. However, the research community has yet to reach a strong consensus on which MTJ technology will prevail in deeply scaled technology nodes such as 8nm. To answer this open ended question, this paper presents a comprehensive study on the scalability of STT-MRAM based on various MTJ technologies: namely, in-plane MTJ (IMTJ), crystal perpendicular MTJ (c-PMTJ), and interface perpendicular MTJ (i-PMTJ). For a practical analysis, our simulation model captures key physics of STT switching in various MTJs by incorporating dimension-dependent effective anisotropy field (H_{Keff}) into the Landau-Lifshitz-Gilbert (LLG) equation and considering realistic material parameters.

Our scaling analysis is based upon maintaining the same degree of thermal stability (Δ) as shown in Fig.1. The required Δ estimated from system specification can be met by adjusting MTJ dimensions in different ways according to anisotropy sources. Once the material parameters and free layer dimensions are set for the target Δ, the proposed physics-based MTJ model estimates the critical switching current density (J_c) for a given switching time (t_{sw}). Based on the simulated J_c, the scalability of the other critical performance metrics can be obtained for different technology nodes. As shown in Fig. 2, our model demonstrates realistic dynamic spin motions showing good agreement with the 50% switching probability contour of measured data [1]. The MTJ dimensions while meeting the Δ requirement over the scaled technologies are listed in Table I. Here, we assume the L3 cache density will double every two technology nodes. The 7.95e-7 chip failure rate is set by the repair capability and the corresponding Δ for 10 year of retention is estimated for each technology [2]. As for the IMTJ, thermal stability is achieved by increasing aspect ratio (AR) up to 3 with scaling down to 45nm node (for manufacturability) and increasing free layer thickness (t_F) for further scaling [3]. For c-PMTJ, K_u is increased up to $6.6\times10^6 J/m^3$ (FePtX) with 0.45nm of t_F to maintain Δ and magnify out-of-plane demagnetizing field for low J_c [4]. Beyond 11nm node, t_F is increased. As for i-PMTJ, t_F is decreased to increase interface anisotropy [5]. However, i-PMTJ cannot meet the Δ below 20nm node since a smaller t_F decreases MTJ volume also. Thickness dependency of damping (α) in CoFeB is considered for both IMTJ and i-PMTJ [5], [6].

Fig. 3 shows the scaling trend of J_c and switching current (I_c) for the three MTJ types under a constant t_{sw} of 4ns. As shown in Fig. 3(b), I_c of IMTJ decreases rapidly with scaling and eventually becomes lower than that of c-PMTJ and i-PMTJ below the 15nm node. Note that a sharp increase in I_c of i-PMTJ is due to exponential increase in α when thickness of CoFeB is below 2nm. In order to estimate MTJ switching energy (E_{MTJ_SW}), RA is determined assuming that $J_c \cdot RA/VDD$ is set to 0.28, which provides optimal balance between the read and write. Fig. 4(a) shows RA must be reduced with scaling to compensate for the increase in J_c, which potentially lead to severe breakdown issues. Finally, Fig. 4(b) displays the scaling of E_{MTJ_SW} showing a similar trend to the scaling of I_c. As for bit-cell area scaling, Table 2 shows the theoretical minimum transistor width (W_{TX}) required for a robust MTJ switching considering current drivability of each technology. To estimate the limit of the cell area, we consider the 2T-1MTJ layout style over the 1T-1MTJ layout as shown in Fig. 5 since the former is more suitable for embedded applications [7]. As shown in Fig. 6(a), the bit-cell size of IMTJ has to be $32F^2$ for robust switching throughout the scaling while that of c-PMTJ needs to be increased up to $40F^2$. This can be attributed to the faster decrease in I_c for IMTJ compared to relatively constant I_c for c-PMTJ. Therefore, c-PMTJ requires improved $I_{d,sat}$ using high mobility transistors or/and wordline voltage boosting techniques. Results shown in Fig. 6(b) indicate that a 1.2x higher $I_{d,sat}$ would be required for c-PMTJ to have the same bit-cell size as IMTJ at the 8nm technology node.

In conclusion, PMTJs are expected to suffer from the high I_c requirement in deeply scaled technology nodes requiring further innovations such as new perpendicular magnetic anisotropy material with a lower damping factor.

References:

[1] H. Zhao, et. al., *JAP*, 2011, pp. 07C720. [2] K. C. Chun, et. al., *JSSC*, 2013, pp. 2240-2243. [3] D. Apalkov, et. al., *IEEE Trans. Magn.*, 2010, pp. 2240-2243. [4] S. Mizukami, et al., *APL*, 2011, pp.052501. [5] S. Ikeda, et. al., *Nature mater.*, 2011, pp. 721-724. [6] X. Liu, et. al., *JAP*, 2011, pp. 033910. [7] R. Takemura, *JSSC*, 2010, pp.869-879.

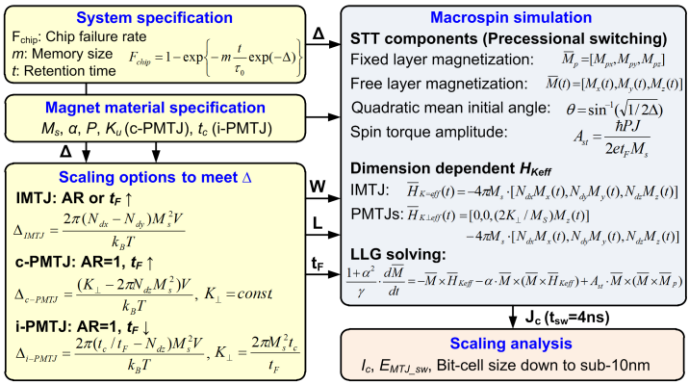


Fig. 1. Scaling analysis using a physics-based MTJ model.

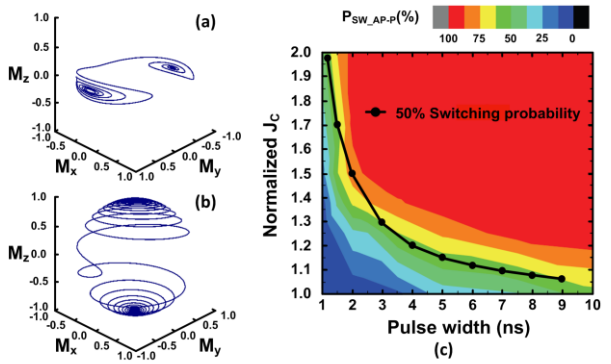
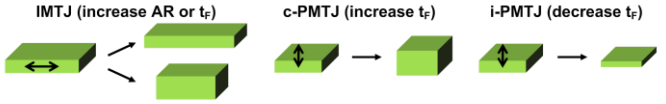


Fig. 2. Model verification results. (a) Dynamic spin motion for IMTJ. (b) Dynamic spin motion for PMTJ. (c) Comparison with experimental data.



Technology node (nm)			65	45	32	22	15	11	8
L3 cache memory size (MB)			16	24	32	48	64	96	128
Thermal stability (10yrs)			73	74	74	75	75	76	76
IMTJ (CoFeB)	M_s=1100, P=0.52	AR	2	2.6	3	3	3	3	3
		t_F (nm)	2.00	2.00	2.24	2.96	4.06	5.37	7.60
		α	0.007	0.007	0.0065	0.006	0.0055	0.005	0.0048
		Remark	AR ↑		t_F ↑, t_F dependent α				
c-PMTJ (FePtX)	M_s=1140, P=0.4, α=0.055	K_u	0.95	1.12	1.45	2.18	3.80	6.6	6.6
		t_F (nm)	0.45	0.45	0.45	0.45	0.45	0.45	0.83
		Remark	constant t_F, K_u ↑						t_F ↑
i-PMTJ (CoFeB)	Ms=1100, P=0.52, t_c=1.5nm	t_F (nm)	1.49	1.42	1.23	0.73	N/A	N/A	N/A
		α	0.013	0.015	0.04	0.12	N/A	N/A	N/A
		Remark	t_F ↓, t_F dependent α				Insufficient Δ		

*M_s: Saturation magnetization (10^3A/m), K_u: Crystal anisotropy (10^6J/m^3)

Table 1. Scaling methods for various MTJs with realistic material parameters under iso-retention condition.

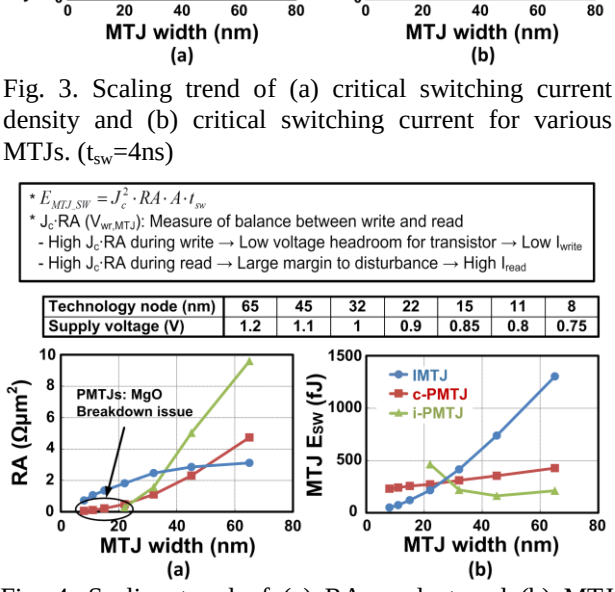


Fig. 3. Scaling trend of (a) critical switching current density and (b) critical switching current for various MTJs. (t_{sw}=4ns)

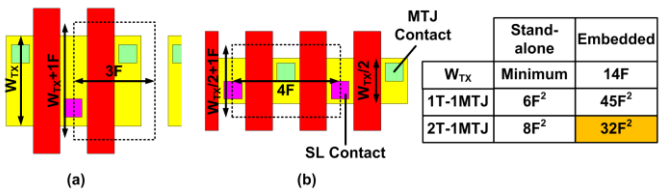
Technology node (nm)		65	45	32	22	15	11	8
Improvement of Transistor performance		Planar bulk			Multi-gate			
		Strained-Si						
		Poly gate		High-K metal gate				
** $I_{d,sat}$ (mA/μm)		1.1	1.3	1.48	1.6	1.75	1.87	2.03
W_{TX} (F)	IMTJ	13.18	9.95	7.59	5.90	4.65	3.85	3.55
	c-PMTJ	4.31	4.77	5.66	7.44	9.95	12.68	16.35
	i-PMTJ	2.13	2.18	4.00	12.69	-	-	-

*Switching time, t_{SW}=4ns **ITRS roadmap

$$I_{d,sat}[mA/\mu m] \times Tech\_node[nm/F] \times W_{TX}[F] > I_c[\mu A]$$

Table 2. Transistor width required for successful MTJ switching. The W_{TX} here is the theoretical minimum value based on the transistor drive current constraint.

Fig. 4. Scaling trend of (a) RA product and (b) MTJ switching energy for various MTJs based on read/write operation margin.



W_{TX}	Stand-alone	Embedded
	Minimum	14F
1T-1MTJ	$6F^2$	$45F^2$
2T-1MTJ	$8F^2$	$32F^2$

Fig. 5. Comparison of STT-MRAM bit cell layout styles. (a) 1T-1MTJ cell layout for stand-alone applications. (b) 2T-1MTJ cell layout for embedded applications. The W_{TX} is adjusted to be a multiple of 2 for 2T-1MTJ case.

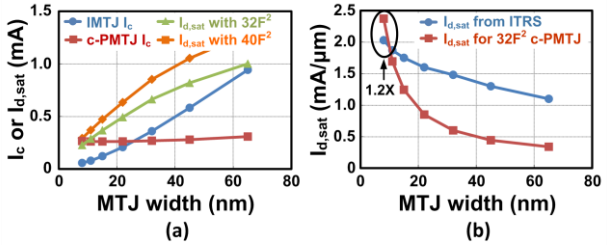


Fig. 6. (a) Bit-cell size for sufficient switching current throughout the MTJ scaling. (b) Drive current required for c-PMTJ to have the same bit-cell size as IMTJ. Higher drive current than ITRS projection is needed at 8nm node.