Design and Analysis of MoS_2-Based MOSFETs for Ultra-Low-Leakage Dynamic Memory Applications

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Introduction: Transition metal dichalcogenides (TMDs) have been of tremendous interest recently for a wide range of electronic and photonic device applications. One of the most promising TMD for scaled transistors is molybdenum disulfide (MoS_2) [1], and several recent reports have shown promising performance and scalability for MoS_2 MOSFETs [2-3]. However, one aspect of these devices that has not received significant attention is their potential for extremely-low leakage operation. Monolayer MoS_2 is an ideal material for use in static and dynamic random access memories since its large effective mass and wide band gap are expected to suppress gate induced drain leakage (GIDL) arising from band-to-band tunneling (**Fig. 1**), while its monolayer nature should enable improved scalability compared to silicon. In order to realize its potential for low-leakage applications, careful modeling and design space analysis is needed. In this work, we describe the design space required to realize two-dimensional (2D) MoS_2 low-leakage MOSFETs. We combine TCAD electrostatic simulations with an analytical transport model to predict the subthreshold performance of MoS_2 MOSFETs. We further apply this model to a dynamic memory cell design and benchmark the performance advantages compared to conventional low-leakage silicon technology.

Device Description and Model Development: The device geometry investigated in this study (**Fig. 2**) utilized a HfO_2 gate dielectric thickness, T_{ox}, of 10.3-15.4 nm (EOT = 2-3 nm) and gate length, L_g, in the range of 15-40 nm. In this regime, conventional models for the scaling length [4] are not valid (**Figs. 3 and 4**) due to the nearly 1:1 aspect ratio of the gate-to-drain and gate-to-channel separations. Instead, TCAD simulations using Synopsys Sentaurus Device™ were used to extract the electrostatic scaling parameters utilized in the analytical device model. The TCAD simulations were compared to results using NEGF simulations [5,6] and found to give comparable results for the subthreshold performance. Based on these simulations, the drain induced barrier lowering (DIBL) and sub-threshold slope (SS) values were calculated (**Figs. 5 and 6**) for L_g and t_{ox} range described above. The simulated DIBL and SS results were then fit using an empirical model (**Fig. 7**) that was found to provide a good fit over the range of L_g and t_{ox} values of interest. Finally, in order to determine the subthreshold current, a 2D analytical model composed of three separate current components was utilized: i) subthreshold current, ii) band-to-band tunneling and iii) Shockley-Reed-Hall (SRH) generation from drain to the body (**Fig. 7**). In order to calculate the GIDL current, the peak electric field in the drain, E_{drain}, was extracted from TCAD and the results were subsequently used to calculate the band-to-band tunneling rate. SRH current utilized a generation time constant of 200 psec, and the gate leakage current was calculated by fitting and extrapolation of leakage currents in commercial high-K Si DRAM devices, but was only calculated for the storage transistor in the three-transistor DRAM cell as described below.

Simulation Results and Discussion: The drain current vs. gate voltage characteristics at different drain voltages (**Fig. 8**) show that, at low V_{ds}, the current is limited by either sub-threshold or SRH current and not GIDL, while at higher V_{ds}, GIDL becomes a factor. To further explore the design space for these devices, a three-transistor based gain cell unit has been analyzed (**Fig. 9**) [7]. Here, the storage node is connected by an access pass transistor and transistor-based storage capacitor. In this type of cell, sub-threshold leakage and GIDL for the pass transistor are critical parameters due to the small amount of stored charge, while gate leakage is important when a '1' is stored in the cell. We utilize CV/I_{min} (where I_{min} is the minimum current) as a performance benchmark for this circuit, which provides an estimate of the maximum possible discharge time, and this parameter should be as large as possible. We have calculated CV/I_{min} and plotted it against different values of L_g and T_{ox} (**Figs. 10 and 11**). We find that an optimum V_{ds} exists that provides the highest retention time, the maximum retention times are found to be orders-of-magnitude higher than conventional Si-based circuits (~250 μs) at comparable dimensions [7].

Conclusion: In conclusion, a semi-empirical analytical model for 2D MoS_2-channel MOSFETs has been developed, and it is found that MoS_2 can greatly enhance the retention time / scalability trade-off of dynamic memory circuits.

[1] B. Radisavljevic, et al., *Nature Nanotech.* **6**, 147 (2011); [2] B. Radisavljevic, et al., *ACS Nano* **5**, 9934 (2011); [3] W. Zhu, et al., *Nature Commun.* **5**, 3087 (2014); [4] W. Y. Lu and Y. Taur, *IEEE Trans. Elect. Dev.* **53**, 1137 (2006); [5] V. Mishra, et al., *Proc. IEDM*, 2013; [6] L. Liu, et al., *IEEE Trans. Elect. Dev.* **60**, 4133 (2013); [7] K. Chun, et al., *IEEE J. Solid-State Circ.* **47**, 2517 (2012).

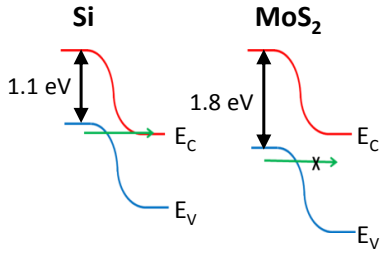
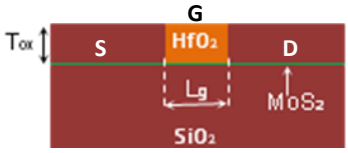


Fig. 1. Diagram depicting motivation for MoS_2 as a low-leakage transistor channel material.



Parameter	Value
Gate dielectric thickness (T_{ox})	10.3-15.4 nm
Oxide dielectric constant	20
Gate Length (L_g)	16 - 40 nm
MoS_2 band gap	1.8 eV
Electron Affinity	4 eV
Carrier Mobility (μ)	250 cm^2/Vs

Fig. 2. Diagram of device geometry utilized for electrostatic simulations. Note that $T_{ox} \sim L_g$ for low-leakage applications.

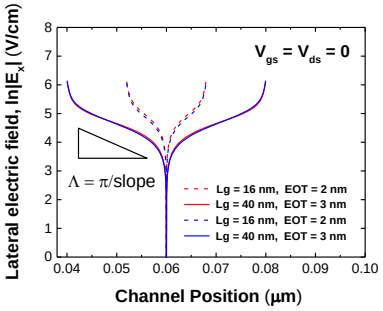


Fig. 3. Diagram of traditional scaling length extraction based upon the slow of the lateral electric field in the device channel.

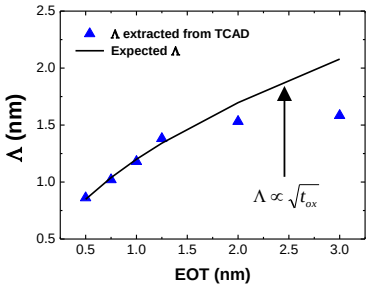


Fig. 4. Comparison of scaling parameter, Λ, from TCAD vs. standard theory. The deviation at high EOT indicates that standard scaling theory does not apply in this regime.

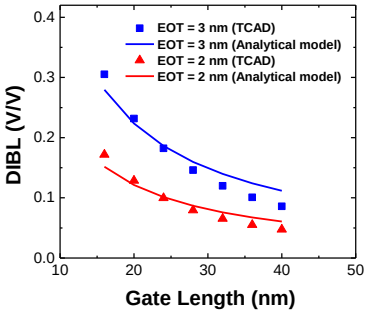


Fig. 5. Comparison of analytical model and extracted drain induced barrier lowering (DIBL) from TCAD.

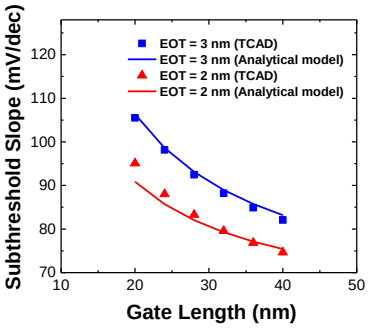


Fig. 6. Comparison of analytical model and extracted subthreshold slope (SS) from TCAD.

Subthreshold current

$$I_{subth} = \mu \cdot \frac{2q^2 m^* W_g}{\pi \hbar^2 L_g} \cdot V_T^2 \cdot \exp\left(\frac{V_{GS} - V_{th} + \eta \cdot V_{DS}}{m V_T}\right) \cdot \left[1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right] \qquad V_T = kT/q \qquad m^* = 0.57 m_0$$

GIDL current

$$I_{b-b} = q W_g A \cdot \exp\left(-\frac{B}{E_{drain}}\right) \cdot \left(\frac{V_{DS} - V_{GS} + V_{th} - E_G/q}{E_{drain}}\right), \quad V_{DS} - V_{GS} + V_{th} > E_G/q$$

$$I_{b-b} = 0, \quad V_{DS} - V_{GS} + V_{th} \le E_G/q$$

$$A = \frac{\sqrt{2}}{18} \cdot \left(\frac{q E_{drain}}{\hbar}\right)^{3/2} \cdot \left(\frac{m_r}{E_g}\right)^{1/4} \qquad B = \frac{\pi^2}{qh} \sqrt{m_r} E_g^{3/2} \qquad m_r = 0.31 m_0$$

SRH current model

$$I_{SRH} = \frac{q n_i W_g \cdot \left(\frac{V_{DS} - V_{GS} + V_{th}}{E_{drain}}\right)}{2\tau_0} \qquad \tau_0 = 200\text{ps} \qquad n_i = 2.7512 \times 10^{-2}\ \text{cm}^{-2}$$

DIBL

$$\eta = 0.205 \cdot \left(\frac{t_{ox}}{L_g} \cdot \sqrt{\frac{\varepsilon_S t_{ox} t_S}{\varepsilon_{ox}}}\right)$$

Body factor

$$m = 1 + 2.79 \cdot \left(\frac{t_{ox}}{L_g} \sqrt{\frac{\varepsilon_S}{\varepsilon_{ox}} t_S}\right)$$

Fig. 7. Equations used to model various components of the leakage currents.

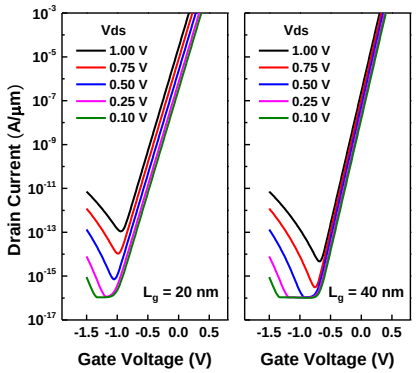


Fig. 8. Modeled subthreshold currents for MoS_2 MOSFETs for T_{ox} = 3 nm at L_g = 20 nm and L_g = 40 nm.

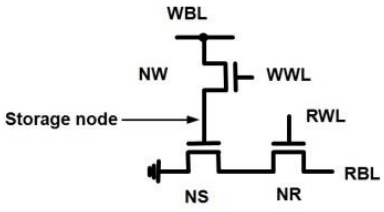


Fig. 9. Diagram showing 3-transistor gain cell utilized for subsequent performance analysis. Charges are transferred into the storage node via transistor NW, which can utilize a negative WWL voltage to minimize the sub-threshold leakage [7].

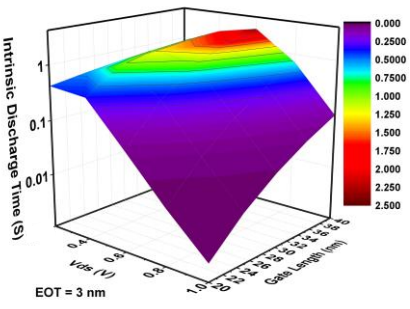


Fig. 10. Intrinsic discharge time plotted vs. supply voltage and gate length at fixed EOT of 3 nm.

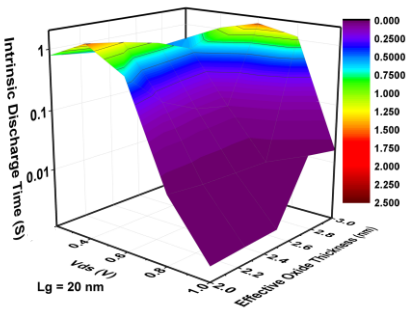


Fig. 11. Intrinsic discharge time plotted vs. supply voltage and EOT at fixed gate length of 20 nm.

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