SRAM Read Performance Degradation under Asymmetric NBTI and PBTI Stress: Characterization Vehicle and Statistical Aging

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Asymmetric BTI Aging Effects

- When input is static, PMOS and NMOS in a signal path are alternately stressed.
- In active mode, the $1^{st}$ edge propagates through unstressed devices while $2^{nd}$ edge propagates through stressed devices only → Asymmetric BTI aging.
SRAM Timing Path Aging

- Internal timing signal paths for SRAM operation are DC stressed when clock is gated off.
- Affects the duty-cycle of critical signals such as WL, SAE, precharge, etc. → lower operating frequency.
SRAM Read Frequency Odometer Structure

- One of the two identical 16kb SRAM arrays is stressed, the other one is kept fresh.
- The dataout signal is looped back to generate self-oscillating signal.
Loop Back Self-Oscillation Read Waveforms
Use Beat Frequency to Detect Aging (1/3)

- Phase comparator is used to generate the beat frequency.
- At time zero the stressed ROSC is trimmed to be slightly slower than the reference ROSC.
Use Beat Frequency to Detect Aging (2/3)

- Phase comparator output: \( f_{\text{beat}} = f_{\text{ref}} - f_{\text{stress}} \)
- Counter counts the number of reference cycle in one period of the beat signal
  \[
  N = \frac{f_{\text{str}} - f_{\text{ref}}}{f_{\text{ref}}}
  \]
Use Beat Frequency to Detect Aging (3/3)

- $f_{\text{stress}}$ (GHz):
  - 0.99 $\rightarrow$ N=100
  - 0.98 $\rightarrow$ N=50

- $f_{\text{ref}}$: 1.00GHz
- $f_{\text{beat}} = f_{\text{ref}} - f_{\text{stress}}$

- 1% frequency difference before stress $\rightarrow$ N=100
- 2% frequency difference after stress $\rightarrow$ N=50
- $\Delta f$ or $\Delta T$ sensing resolution is 0.01%
32nm SRAM Test Chip and Features

<table>
<thead>
<tr>
<th>Process</th>
<th>HKMG SOI CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD/IO Supplies</td>
<td>0.9V / 1.8V</td>
</tr>
<tr>
<td>Each SRAM Array Size</td>
<td>128X128</td>
</tr>
<tr>
<td>SRAM Cell Device Type</td>
<td>Floating-body device</td>
</tr>
<tr>
<td>Peripheral Device Type</td>
<td>Body-contact device</td>
</tr>
<tr>
<td>Area</td>
<td>500x455μm²</td>
</tr>
<tr>
<td>Meas. Δf Resolution</td>
<td>0.01%~0.1%</td>
</tr>
<tr>
<td>Meas. Interrupt</td>
<td>~ 1μs</td>
</tr>
</tbody>
</table>
Degradation of $f_{\text{read}}$ with Stress Time

- Mean value ($\mu$) of $f_{\text{read}}$ decreases with stress time while its standard deviation ($\sigma$) increases
- BTI induced $\sigma$ is comparable to that of process variation induced $\sigma$ for given stress condition
Distribution of $f_{\text{read}}$ at Different Stress Voltage

- Mean value ($\mu$) of $f_{\text{read}}$ decreases with higher stress voltage while its standard deviation ($\sigma$) increases.

**Stressed @25°C for 1500s**

- $f_{\text{read}}$ (GHz): 1.25, 1.3, 1.35
- Occurrences (%):
  - 1.4V: $\mu=1.34$, $\sigma=0.0048$
  - 1.6V: $\mu=1.33$, $\sigma=0.0065$
  - 1.8V: $\mu=1.28$, $\sigma=0.01$

$\mu$ decreases; $\sigma$ increases.
Degradation of $f_{\text{read}}$ with Stress Voltage

- $\sigma$ of the SRAM read frequency degradation ($\Delta f_{\text{read}}$) follow power law dependence ($t^n$) as $\mu$, due to discrete random charge fluctuation
- Larger degradation at higher stress voltages
Impact of Temperature on the Degradation of $f_{\text{read}}$

- The magnitudes of both $\mu$ and $\sigma$ of $\Delta f_{\text{read}}$ at 135°C are more than twice of those at 25°C.
Slope distribution of $f_{\text{read}}$ Aging

- The voltage and temperature have little impact on the BTI time slope distribution.
Reduced SRAM Read Error Rate

- Bit failure rate is reduced after stress due to the relaxed WL pulse width.
Summary

• Impact of asymmetric BTI aging on SRAM read speed studied for the first time
• An SRAM read speed odometer based on the beat-frequency detection concept was implemented in HKMG technology with ps resolution and μs measurement interruption
• SRAM read speed degrades due to the delayed SAE signal
• SRAM read failure rate decreases after stress due to the relaxed WL pulse width