SRAM Read Performance Degradation under Asymmetric NBTI and PBTI Stress: Characterization Vehicle and Statistical Aging

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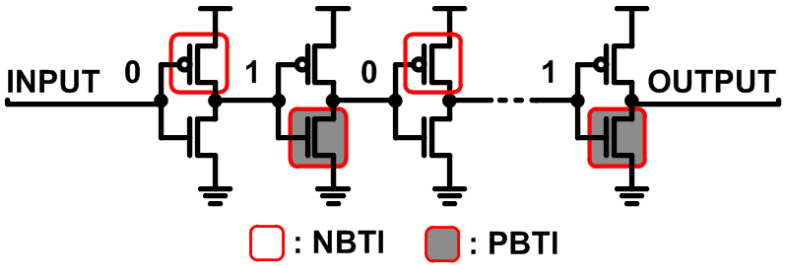
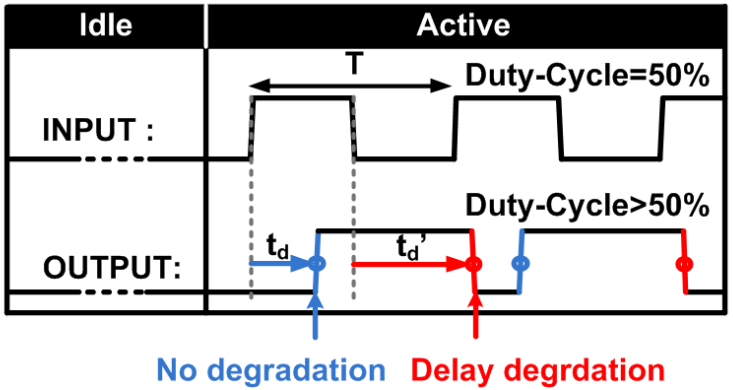
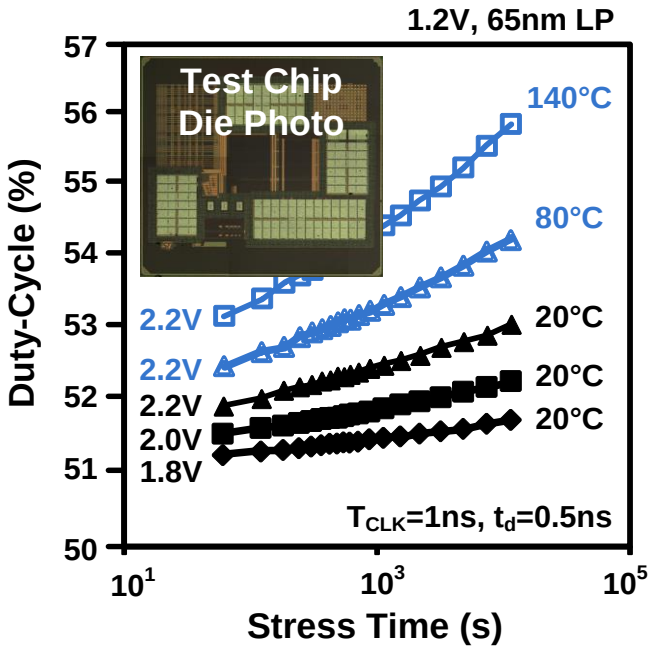
Asymmetric BTI Aging Effects

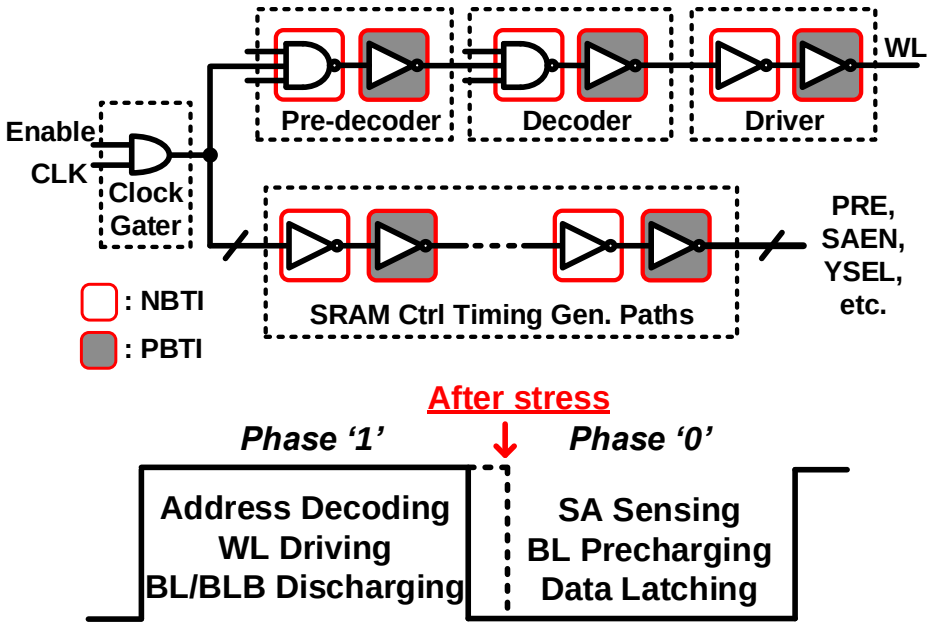


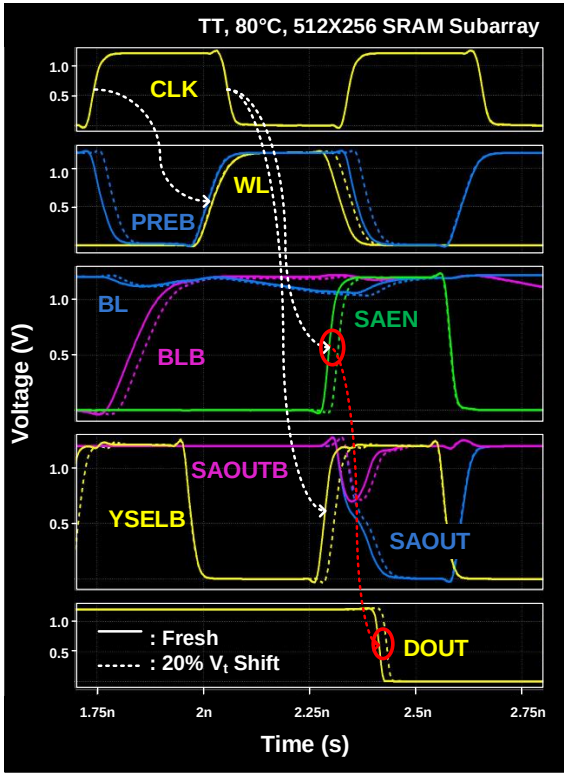




- When input is static, PMOS and NMOS in a signal path are alternately stressed
- In active mode, the 1st edge propagates through unstressed devices while 2nd edge propagates through stressed devices only → Asymmetric BTI aging

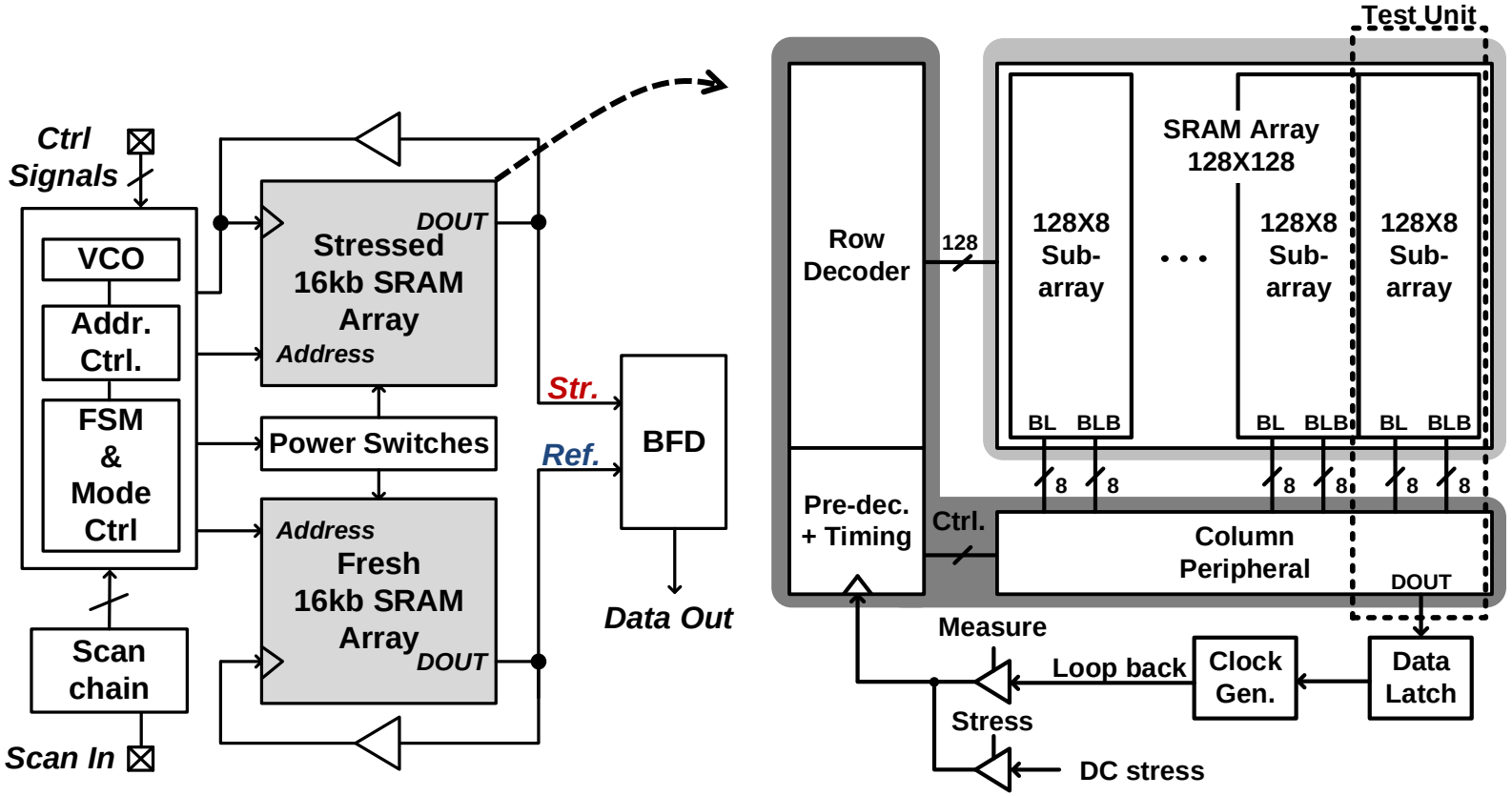
SRAM Timing Path Aging





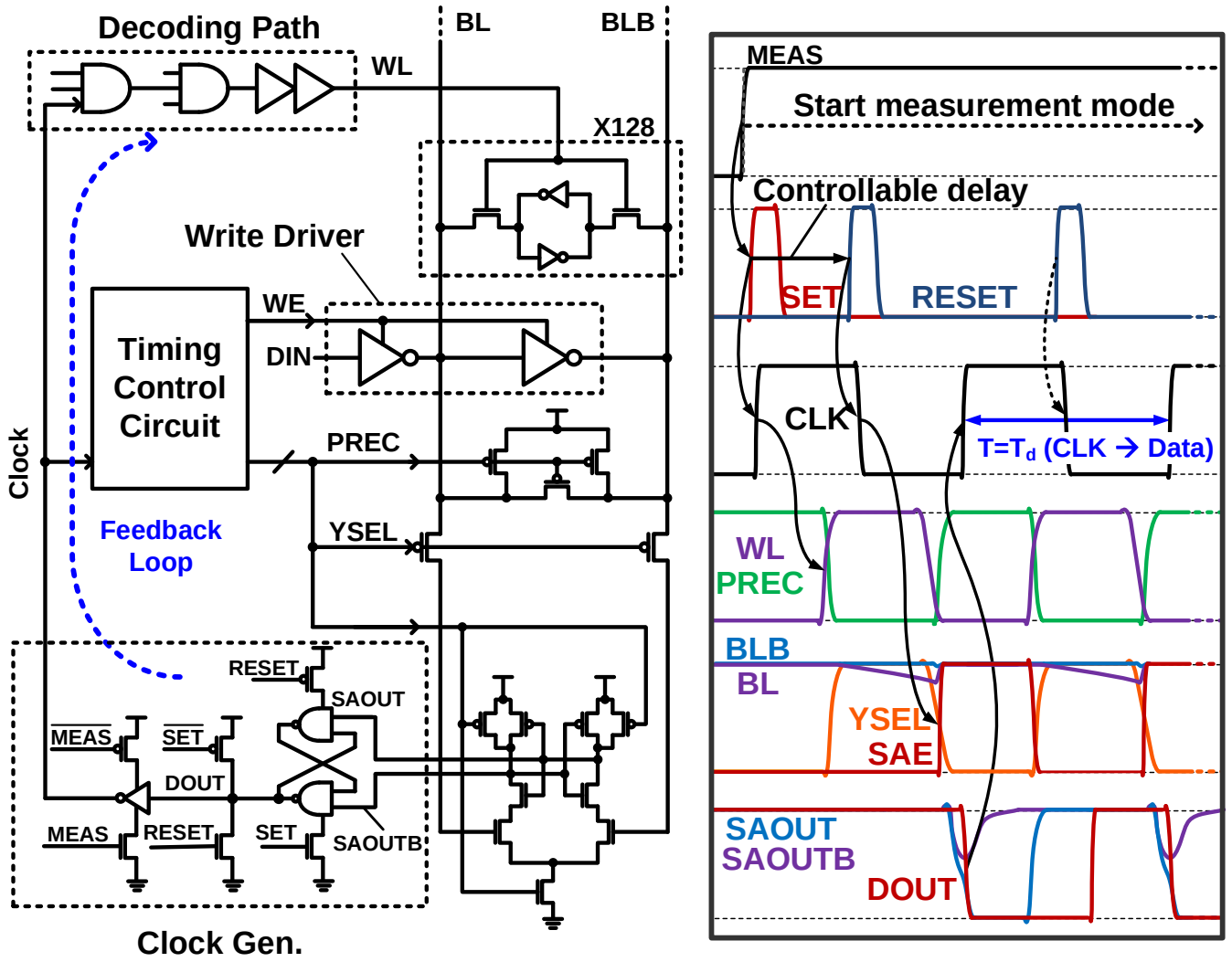
- **Internal timing signal paths for SRAM operation are DC stressed when clock is gated off**
- **Affects the duty-cycle of critical signals such as WL, SAE, precharge, etc. → lower operating frequency**

SRAM Read Frequency Odometer Structure

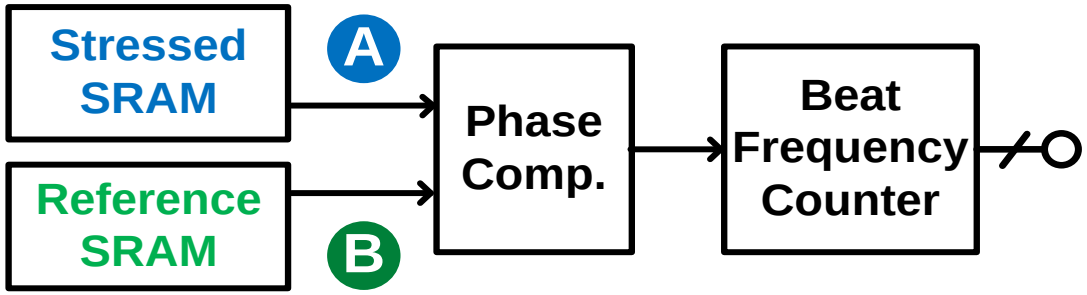


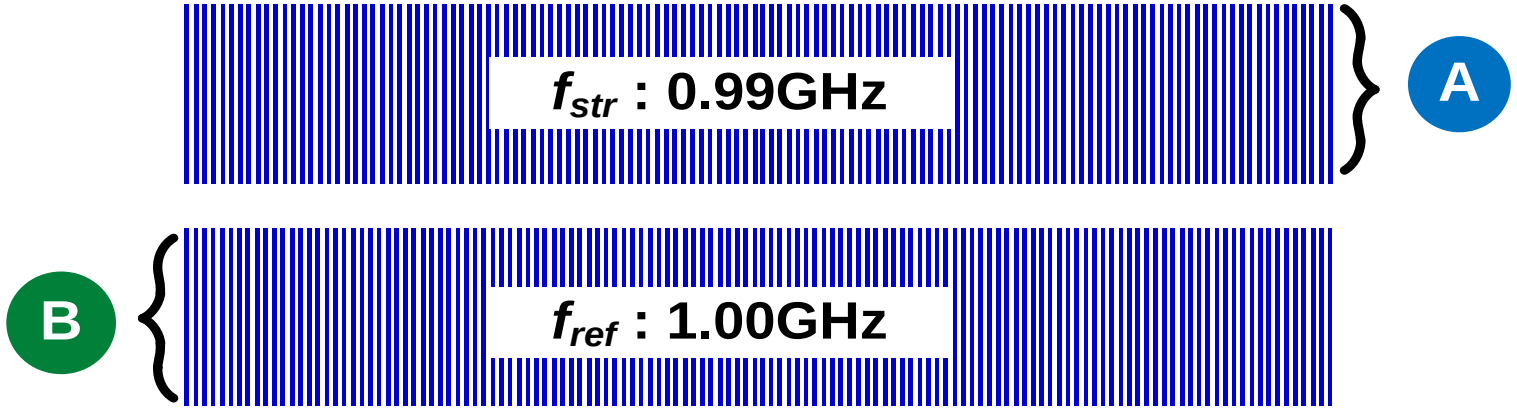
- One of the two identical 16kb SRAM arrays is stressed, the other one is kept fresh
- The dataout signal is looped back to generate self-oscillating signal

Loop Back Self-Oscillation Read Waveforms



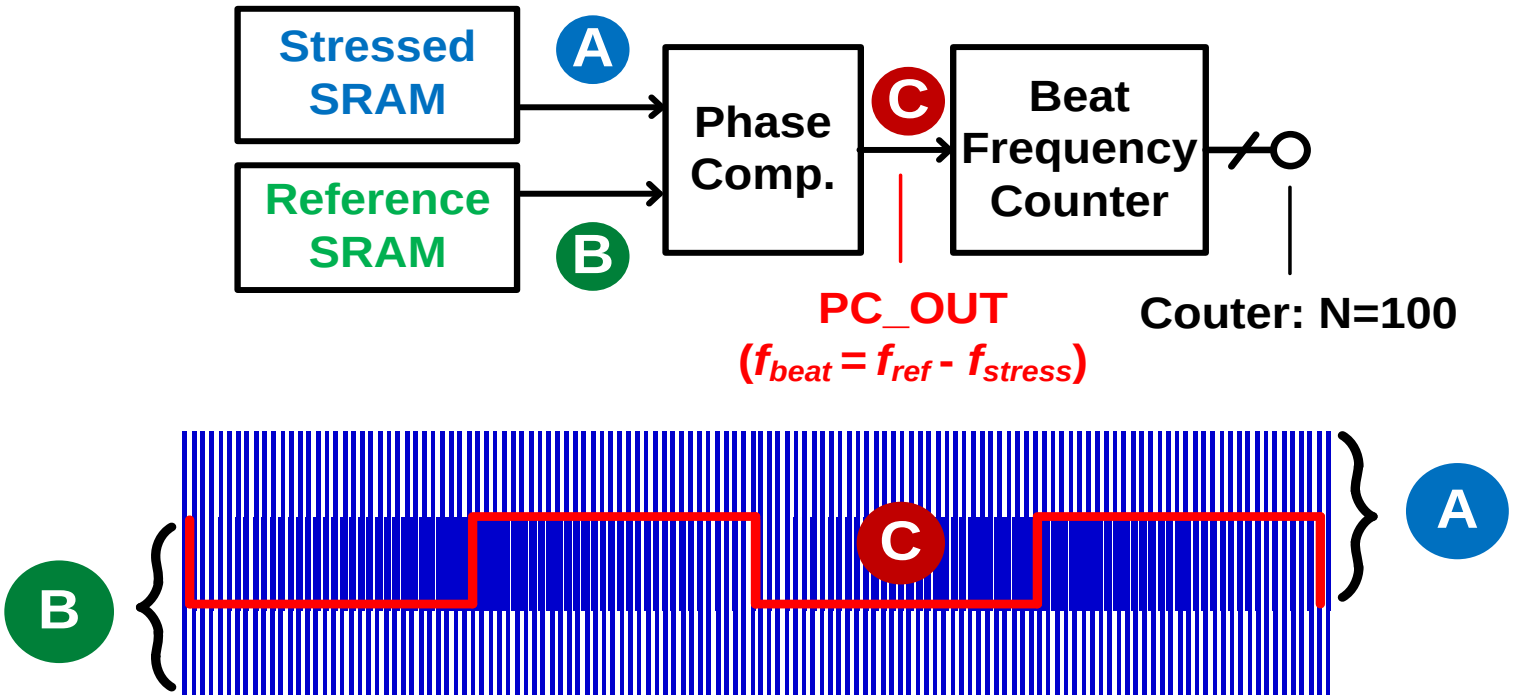
Use Beat Frequency to Detect Aging (1/3)





- Phase comparator is used to generate the beat frequency
- At time zero the stressed ROSC is trimmed to be slightly slower than the reference ROSC

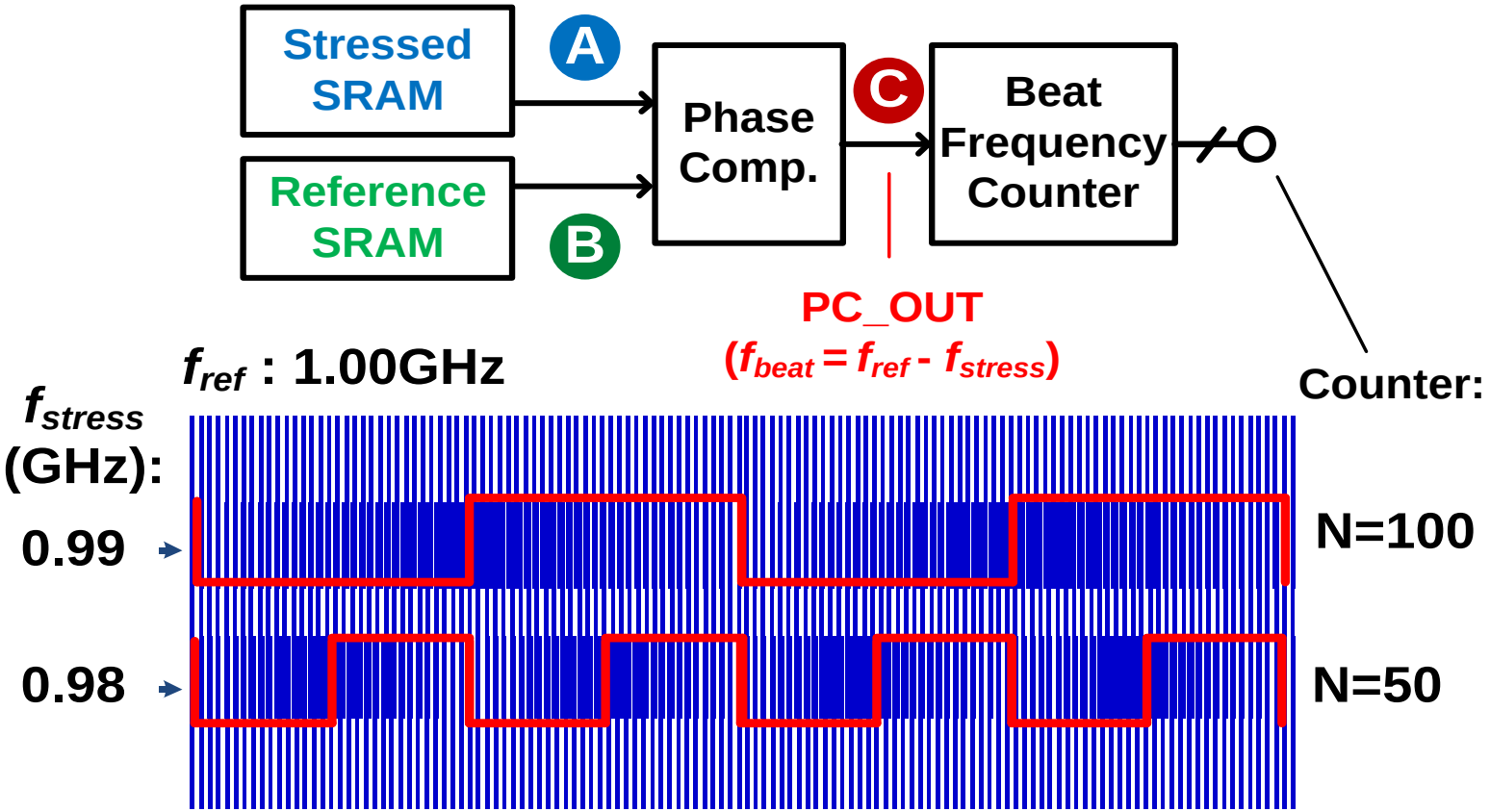
Use Beat Frequency to Detect Aging (2/3)



- Phase comparator output: $f_{beat}=f_{ref}-f_{stress}$
- Counter counters the number of reference cycle in one period of the beat signal

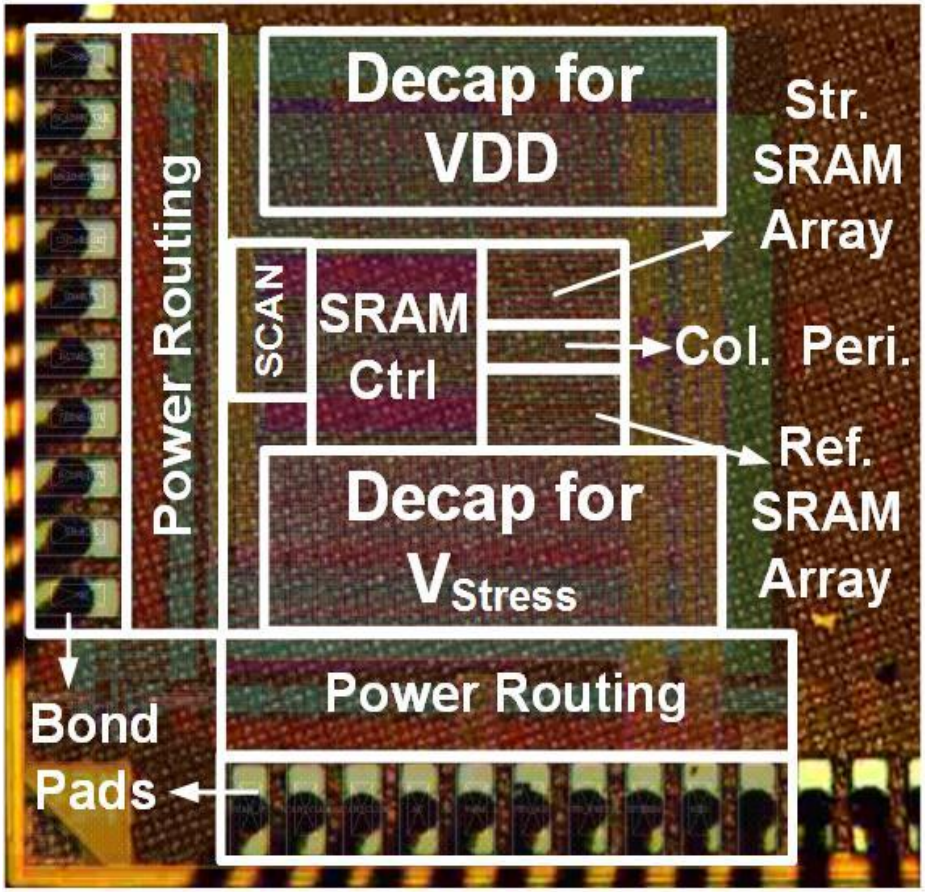
$$N=(f_{str}-f_{ref})/f_{ref}$$

Use Beat Frequency to Detect Aging (3/3)



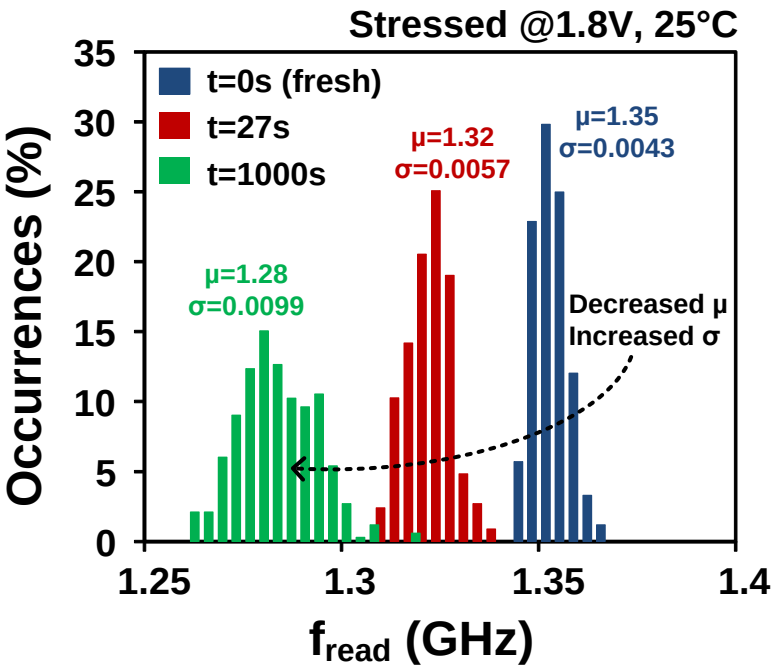
- 1% frequency difference before stress → N=100
- 2% frequency difference after stress → N=50
- Δf or ΔT sensing resolution is 0.01%

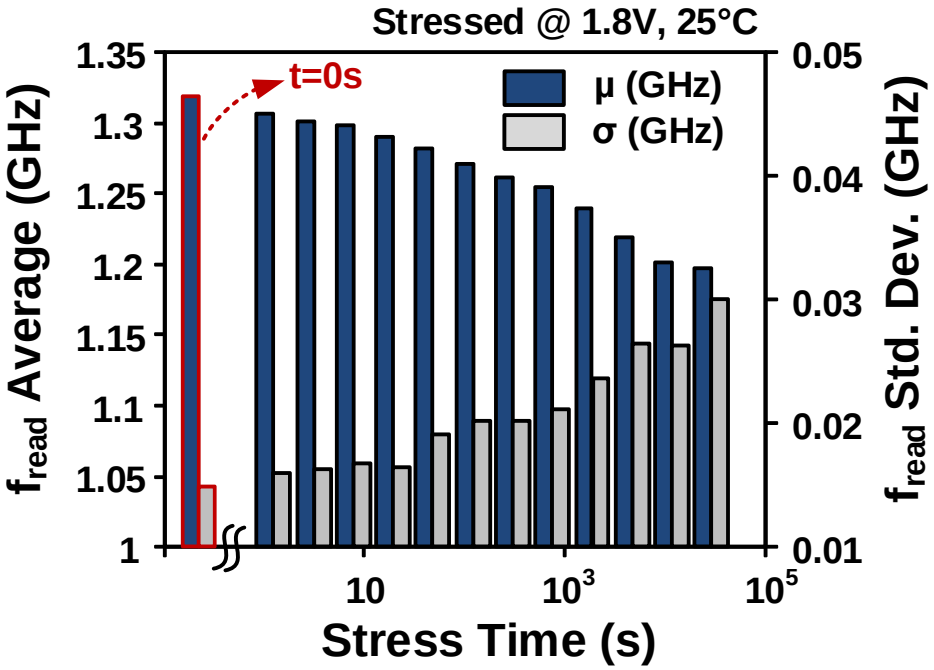
32nm SRAM Test Chip and Features



Process	HKMG SOI CMOS
VDD / IO Supplies	0.9V / 1.8V
Each SRAM Array Size	128X128
SRAM Cell Device Type	Floating-body device
Peripheral Device Type	Body-contact device
Area	500x455μm^2
Meas. Δf Resolution	0.01%~0.1%
Meas. Interrupt	~ 1μs

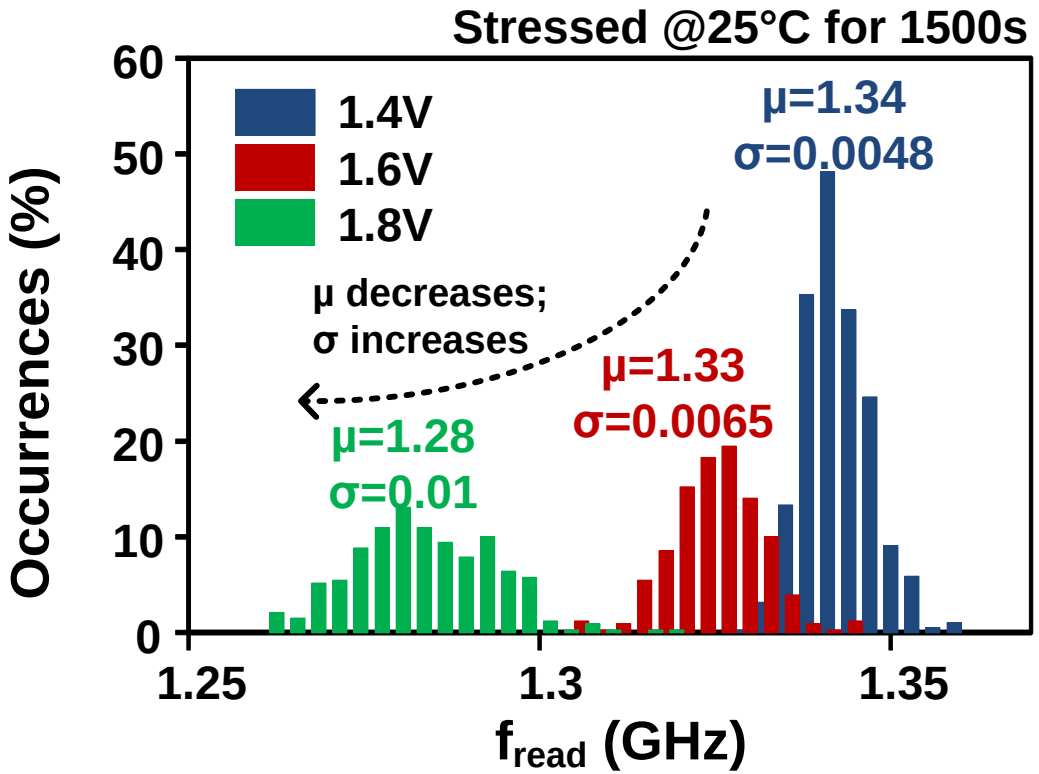
Degradation of f_{read} with Stress Time





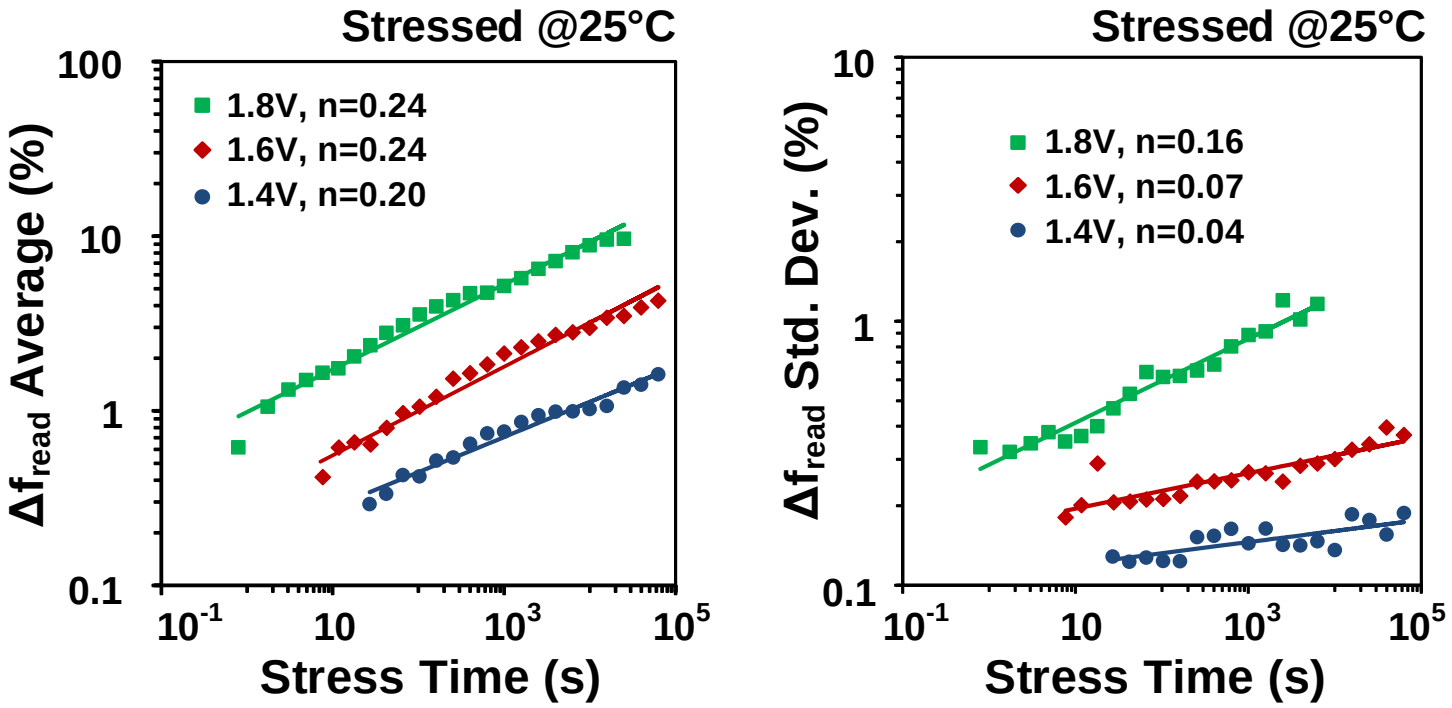
- Mean value (μ) of f_{read} decreases with stress time while its standard deviation (σ) increases
- BTI induced σ is comparable to that of process variation induced σ for given stress condition

Distribution of f_{read} at Different Stress Voltage



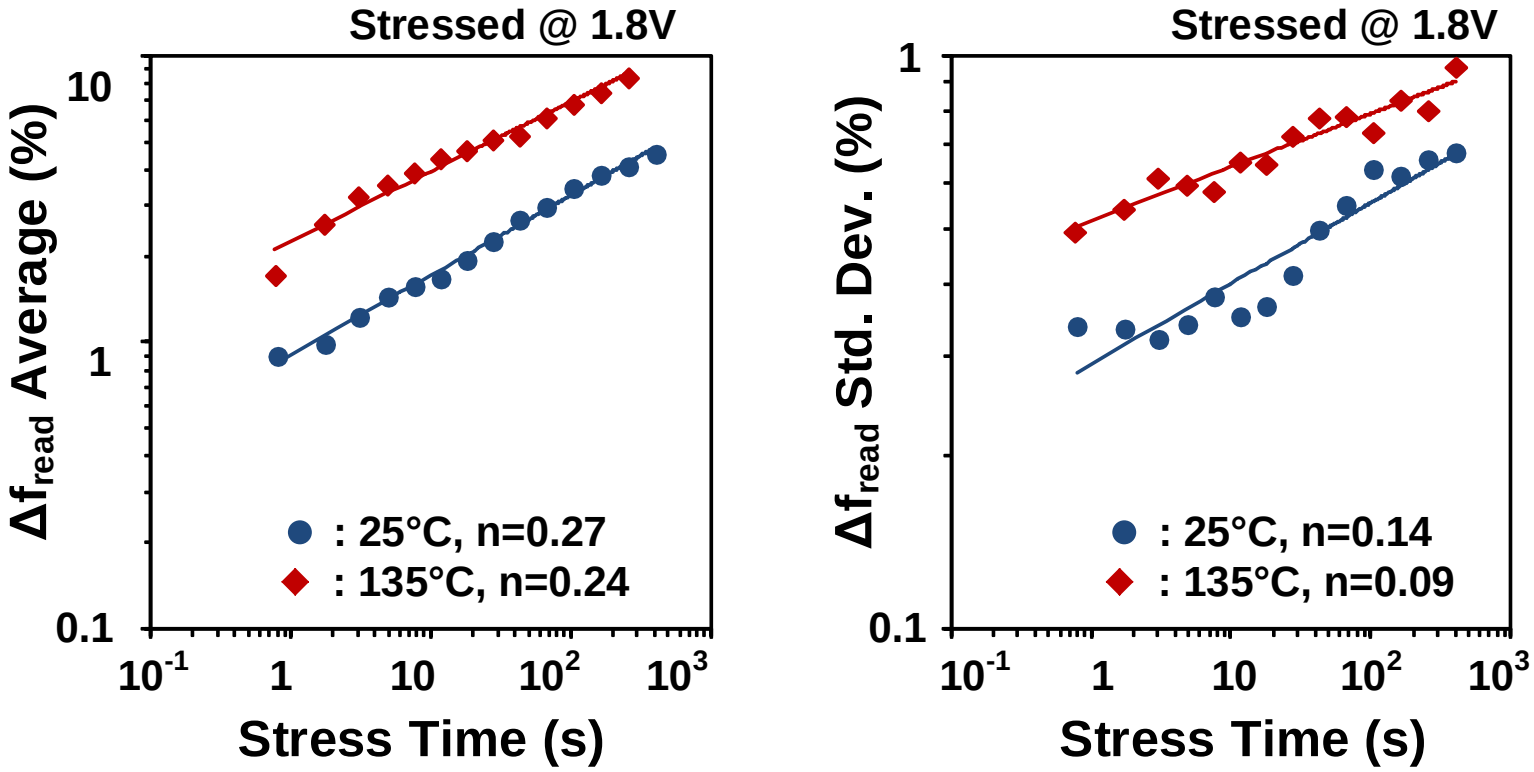
- Mean value (μ) of f_{read} decreases with higher stress voltage while its standard deviation (σ) increases

Degradation of f_{read} with Stress Voltage



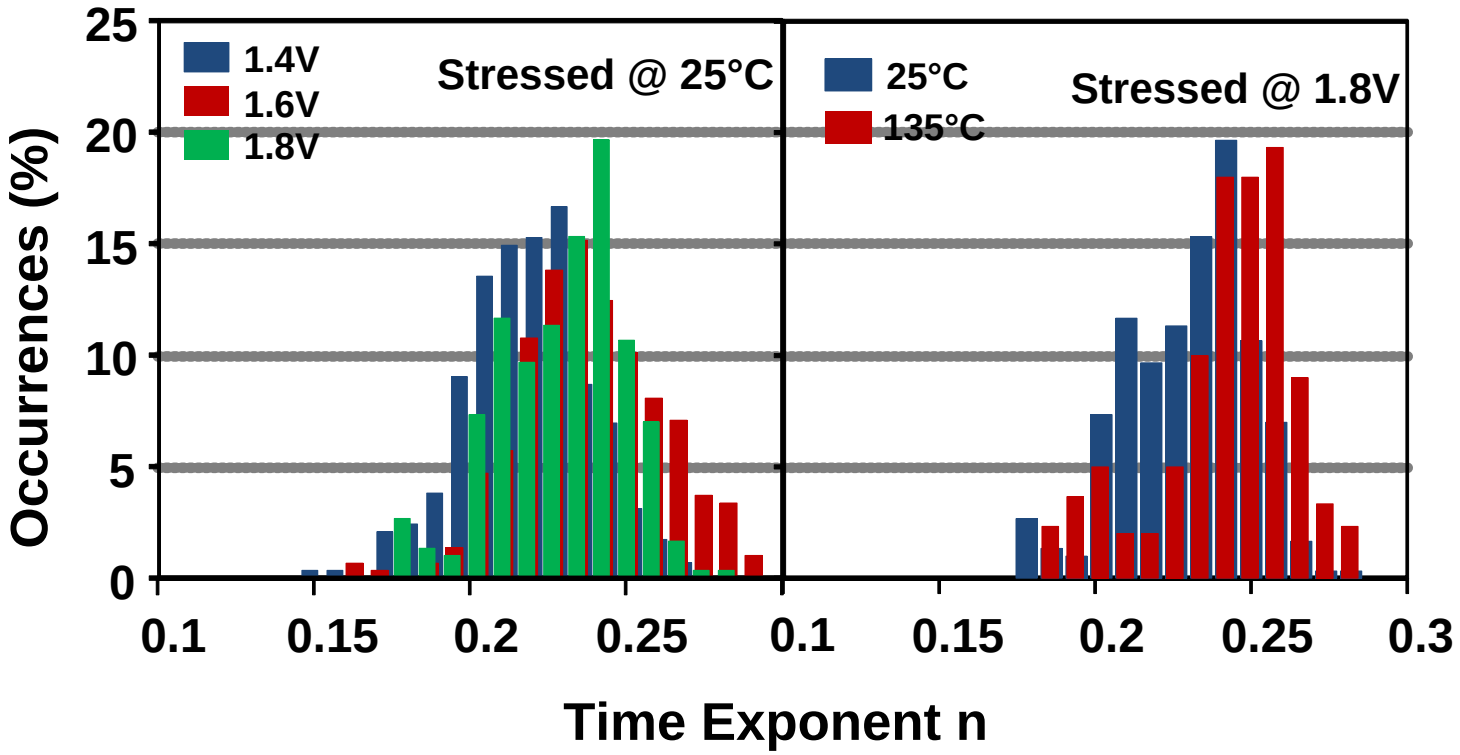
- σ of the SRAM read frequency degradation (Δf_{read}) follow power law dependence (t^n) as μ, due to discrete random charge fluctuation
- Larger degradation at higher stress voltages

Impact of Temperature on the Degradation of f_{read}



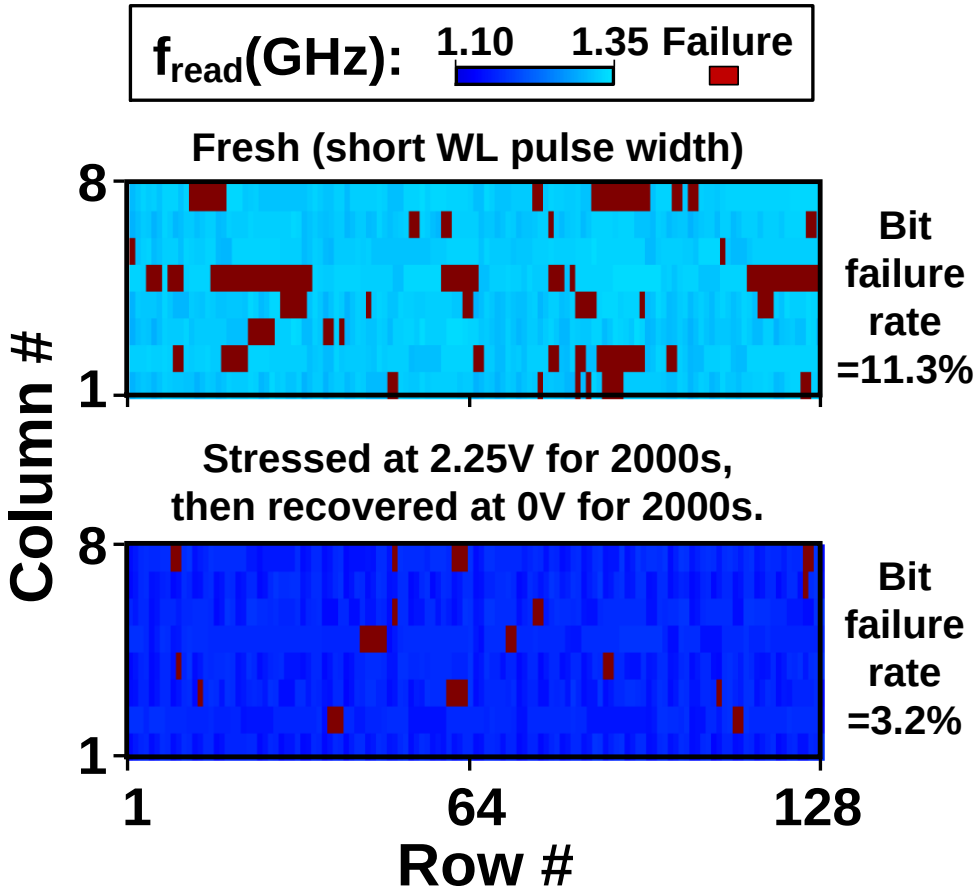
- **The magnitudes of both μ and σ of Δfread at 135°C are more than twice of those at 25°C.**

Slope distribution of f_{read} Aging



- The voltage and temperature have little impact on the BTI time slope distribution

Reduced SRAM Read Error Rate



- **Bit failure rate is reduced after stress due to the relaxed WL pulse width**

Summary

- Impact of asymmetric BTI aging on SRAM read speed studied for the first time
- An SRAM read speed odometer based on the beat-frequency detection concept was implemented in HKMG technology with ps resolution and μs measurement interruption
- SRAM read speed degrades due to the delayed SAE signal
- SRAM read failure rate decreases after stress due to the relaxed WL pulse width