SRAM Read Performance Degradation under Asymmetric NBTI and PBTI Stress: Characterization Vehicle and Statistical Aging Data

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***Abstract* — Asymmetric BTI aging in circuit paths has shown to cause a time dependent shift in the signal's duty cycle, affecting the performance of circuits such as low power SRAMs whose operation rely on both the positive and negative edges of the clock signal. In this work, we propose the first known on-chip reliability monitor to accurately characterize the impact of asymmetric BTI on SRAM read speed. Statistical data collected from test chip built in a 32nm high-k metal-gate technology shows that (i) the average SRAM read frequency decreases with stress while its variation increases with stress and (ii) both μ and σ of read frequency shift follow a power law dependence on stress time. These observations point to the impact of SRAM peripheral circuit aging on read performance, and the utility of the proposed monitor for characterizing circuit level reliability concerns.**

***Index Terms* — SRAM, read degradation, BTI, asymmetric aging, peripheral circuits.**

I. Introduction

Bias temperature instability (BTI) has become the chief reliability concern in scaled CMOS technologies [1-5]. With the advent of high-k metal-gate transistors for suppressing gate tunneling leakage, positive BTI in NFET transistors has emerged as an important design consideration in both logic and memory. Although there have been a number of researches addressing aging issues in SRAM memory, most of the work has focused on bit cell level metrics such as read margin and write margin [2,3]. In contrast, very little attention has been paid on performance degradation issues in peripheral circuits such as row decoders, sense amplifiers, column I/Os, and timing generation blocks. Recently, asymmetric BTI stress occurring in a clock path has shown to have a detrimental effect on signal duty cycle [4-5]. As illustrated in Fig. 1, DC BTI stress causes NBTI and PBTI in alternating gates of a delay chain when the circuit is idle (e.g. clock gating

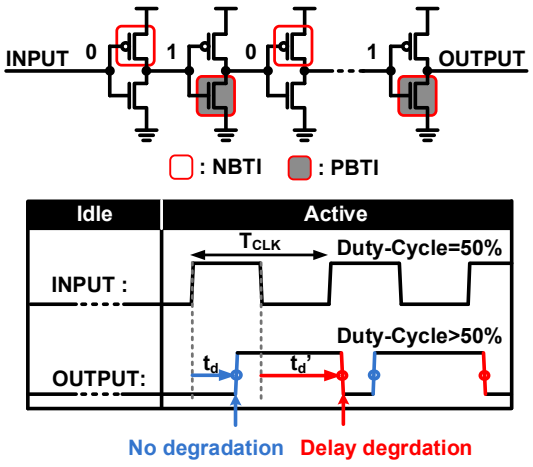


Fig. 1. (upper) Alternating NBTI/PBTI stress in a clock buffer chain in idle mode. (lower) Asymmetric delay degradation of rising and falling edges causes BTI-induced duty-cycle shifts.

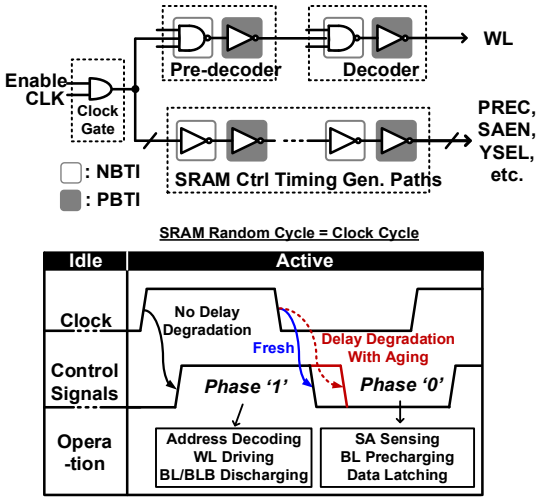


Fig. 2. Many low power SRAM designs derive internal timing signals from both rising and falling edges of the clock. Asymmetric aging described in Fig. 1 can lead to inaccurate SRAM timing.

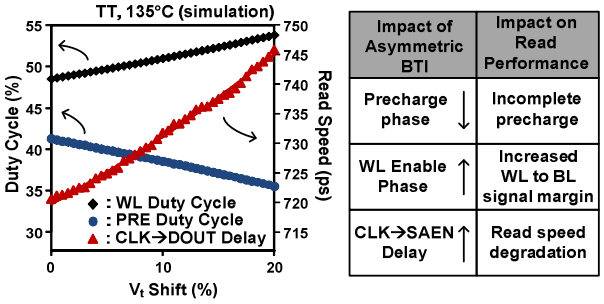


Fig. 1. SRAM read timing under asymmetric BTI aging. Duty cycle affects the SRAM timing signals resulting in a longer read cycle time.

mode). When the circuit switches from idle to active mode, the first rising edge of the input clock travels through the fresh devices on the path and hence is not affected by BTI stress. The subsequent falling edge on the other hand experiences considerable delay degradation as the signal traverses through the devices that were stressed in the preceding idle mode. The delay difference between the rising and falling edges of the clock gives rise to a time-dependent duty cycle shift called asymmetric BTI aging. This negatively affects SRAM performance as both the rising and falling edges of the input clock are used to generate various timing signals of an SRAM as shown in Fig. 2. In this example, phase '0' (i.e. address decoding, wordline driving, and bitline discharging) becomes longer, while phase '1' (i.e. sense amplifier enable, bitline precharging, and data latching) becomes shorter with BTI stress. This has two consequences: (1) the clock-to-dataout delay increases due to the delayed sense amplifier enable signal, and (2) the shorter precharge cycle leads to an incomplete bitline pre charge level which in turn increases the sensing time. This can be seen in the simulation results in Fig. 3.

In this work, we propose the first known on-chip reliability monitor to accurately characterize the impact on asymmetric BTI on SRAM read speed. Our proposed technique measures the frequency difference between a fresh and stressed SRAM arrays where the output signal is looped back to the input clock to form an oscillating circuit. We have adopted our previous beat frequency detection circuit to achieve a picosecond order measurement precision with a measurement interrupt less than a microsecond.

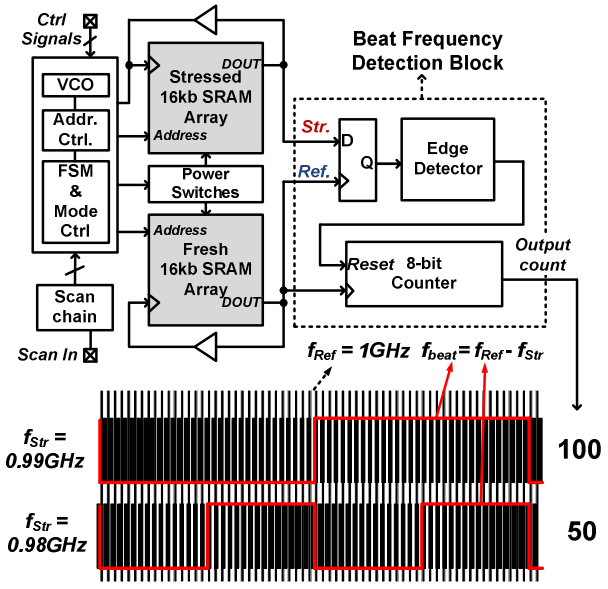


Fig. 4. Top level schematic of the proposed SRAM reliability test vehicle. The difference in read speed between a fresh and stressed SRAM array is measured using the beat frequency detection scheme which can achieve a frequency shift measurement resolution of >0.01% and a measurement time of >1µs. Unwanted BTI recovery can be prevented using this fast measurement technique. The output of the SRAM array is looped back to generate an oscillating frequency corresponding to the critical read path delay.

II. SRAM Reliability Test Vehicle

The top level diagram of the proposed SRAM reliability test macro is shown in Fig. 4, which consists of two identical 16k bit SRAM blocks, a beat frequency detection (BFD) system, global control circuits (scanchain, FSM, address control, etc.) and on-chip power gate switches. During stress mode, a high supply voltage is applied to only one of the SRAM blocks through the on-chip power switches, while the other SRAM is kept fresh by shutting off the power supply. In measurement mode, both SRAMs operate under a nominal VDD with their respective dataout signals looped back to generate two oscillating signals.

The frequency difference between the output signals of the stressed and reference SRAM arrays is then captured by the BFD block [6,7,9]. The block diagram of the BFD block is shown in Fig. 4 (upper right). Frequency difference (or beat frequency) is sensed by a D-flip-flop. A counter records the beat frequency by counting the number of reference SRAM period during one period of beat output. The output count is then periodically scanned out over the course of the stress experiment. As proven in our previous odometer designs [6,7,9], a measurement

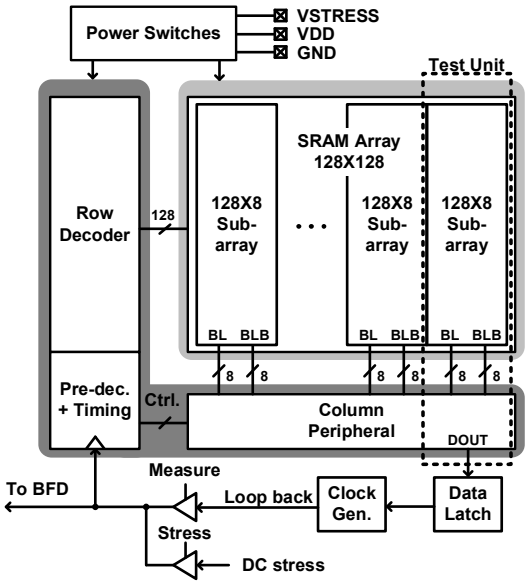


Fig. 5. Schematic of a single 128x128 SRAM array. DOUT is looped back to trigger the clock input, generating an oscillating output for read frequency measurements.

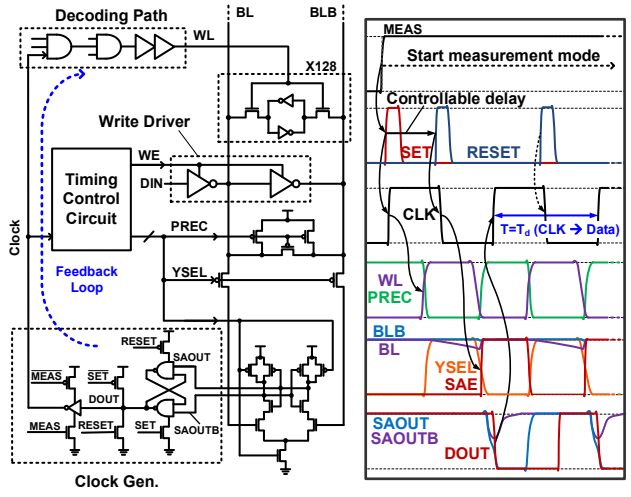


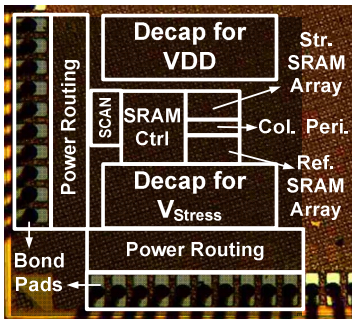
Fig. 6. Detailed schematic and timing diagram of SRAM read path with loop back configuration. At the end of the first read cycle, DOUT is fed back to trigger the next rising edge of the input clock. A reset signal is used to initialize the clock for the next cycle.

scheme that detects beat frequency rather than the absolute frequency can achieve high precision and a short measurement time to prevent unwanted BTI recovery. Furthermore, the differential sensing nature and the symmetric layout of the proposed circuit effectively rejects any common mode noise due to temperature or voltage drifts.

Each SRAM macro comprises peripheral circuits and sixteen 128x8 sub-arrays as illustrated in Fig. 5. During stress mode, the clock can be either gated off to induce asymmetric BTI aging or toggled by an on-chip VCO for AC stress. The detailed measurement sequence is described in the read path schematic and the internal control waveforms in Fig. 6. At the beginning of the measurement mode, the rising edge of the MEAS signal triggers the first SET signal, which generates a rising edge at the SRAM input clock. The clock is then switched back to 0 by an NMOS device controlled by the self-timed RESET signal. The tunable delay between SET and RESET pulses determines the pulse width of the SRAM clock, which in turn sets the duty-cycle of internal control signals. After the first read cycle is complete, the data output signal, DOUT, triggers the next clock rising edge. As this process repeats, an oscillating signal is generated with a period corresponding to the SRAM read path delay.

III. 32NM TESTCHIP RESULTS

The proposed SRAM reliability macro was implemented in a 32nm high-k metal gate process. The die photo and feature summary table are given in Fig. 7. The entire sub-array was initialized to '0' prior to applying stress to ensure the falling edge of DOUT triggers the oscillation. Subsequently, we apply voltage stress.



Process	32nm HKMG
VDD / IO Supplies	0.9V / 1.8V
Each SRAM Array Size	128X128
SRAM Cell Device Type	Floating-body device
Peripheral Device Type	Body-contact device
Area	500x455μm^2
Meas. Δf Resolution	>0.01%
Meas. Interrupt	>1μs

Fig. 7. Die microphotograph and test chip feature summary.

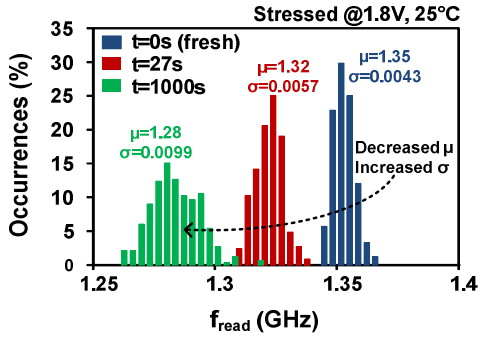


Fig. 8. SRAM read frequency (f_{read}) distribution at different stress times.

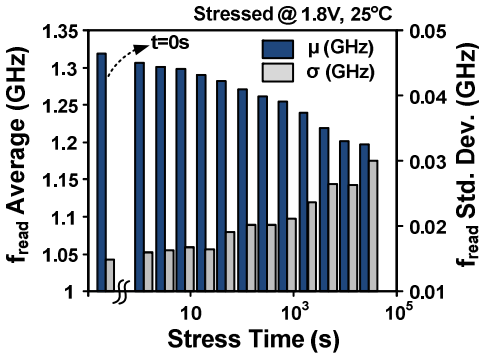


Fig. 9. μ and of f_{read} as a function of stress time.

Intermittent measurements are taken from each SRAM cell between the long stress intervals. Distributions of the fresh and stressed read frequencies (f_{read}) under a 1.8V stress are plotted in Fig. 8. The average (μ) of f_{read} decreases with stress time while its standard deviation ( ) increases. As shown in Fig. 9, after being stressed under 1.8V, 25° for 40k seconds, μ of f_{read} drops from 1.33GHz to 1.2GHz, while increases from 0.015GHz to 0.030GHz. The distribution of f_{read} after a 1500 second stress period under different stress voltages are compared in Fig. 10, showing that of f_{read} increases with a higher stress voltage. The μ and of f_{read} versus stress time are shown in Fig. 11, confirming that both μ and follow a power law dependence. The time exponent (n) of is less than that of μ, which is consistent with the modeling results

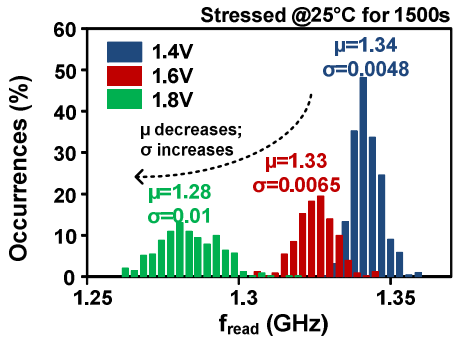


Fig. 10. f_{read} distribution after 1500 seconds of DC stress under different voltages.

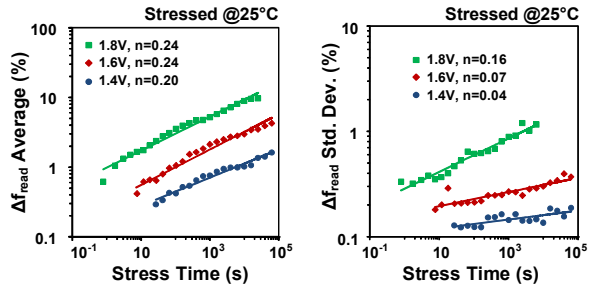


Fig. 11. μ and of f_{read} under different stress voltages. Frequency shift data follows a power law relationship with respect to stress time.

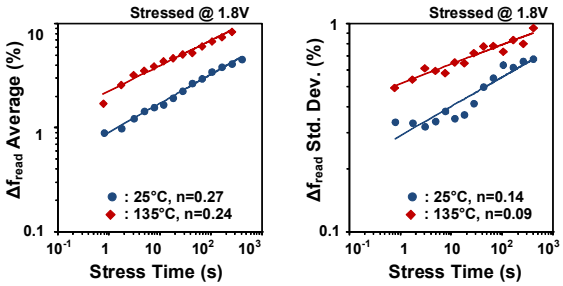


Fig. 12. μ and of f_{read} under different temperatures.

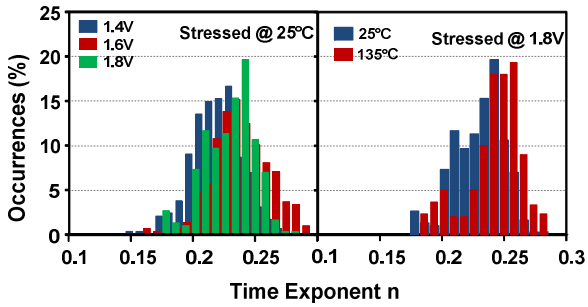


Fig. 13. Distribution of time exponent n under different stress voltages and temperatures.

based on discrete random charge fluctuation [8] as well as the statistical data collected from a ring oscillator array [9]. Stronger BTI at higher temperature induces more random defects, which in turn increases the of f_{read} as shown in Fig. 12. The magnitudes of both μ and of f_{read} at 135°C are more than twice of those at 25°C. Fig. 13 shows the distribution of time exponent n, from which we can see the voltage and temperature have little impact on the BTI time slope distribution.

IV. Conclusions

DC BTI induced asymmetric duty-cycle shift affects SRAM read operation as both rising and falling clock edges are used to generate internal timing signal. In this work, we present a SRAM reliability test vehicle to detect the asymmetric aging impact on the read performance in a 32nm SRAM. Statistical data shows that variation in read frequency increases with the stress time. Both average and standard deviation of read frequency shift (i.e. f) follow a power law dependence with respect to stress time.

V. Acknowledgement

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