A Test Circuit Based on a Ring Oscillator Array for Statistical Characterization of Plasma-Induced Damage

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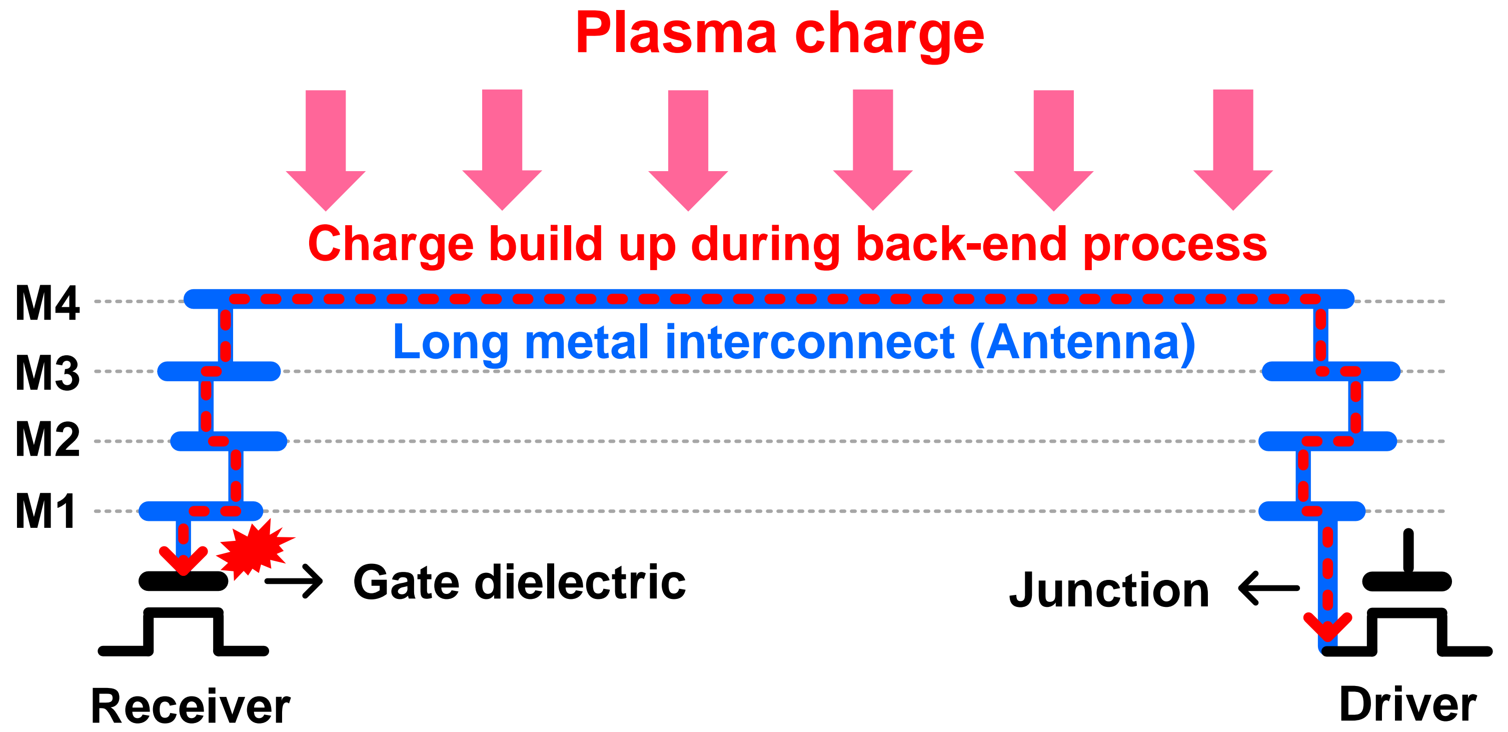
Agenda

- Plasma-Induced Damage (PID)
- Proposed PID characterization circuit Based on a Ring Oscillator Array
- Antenna Design
- Statistical Experiment Results
- Conclusions

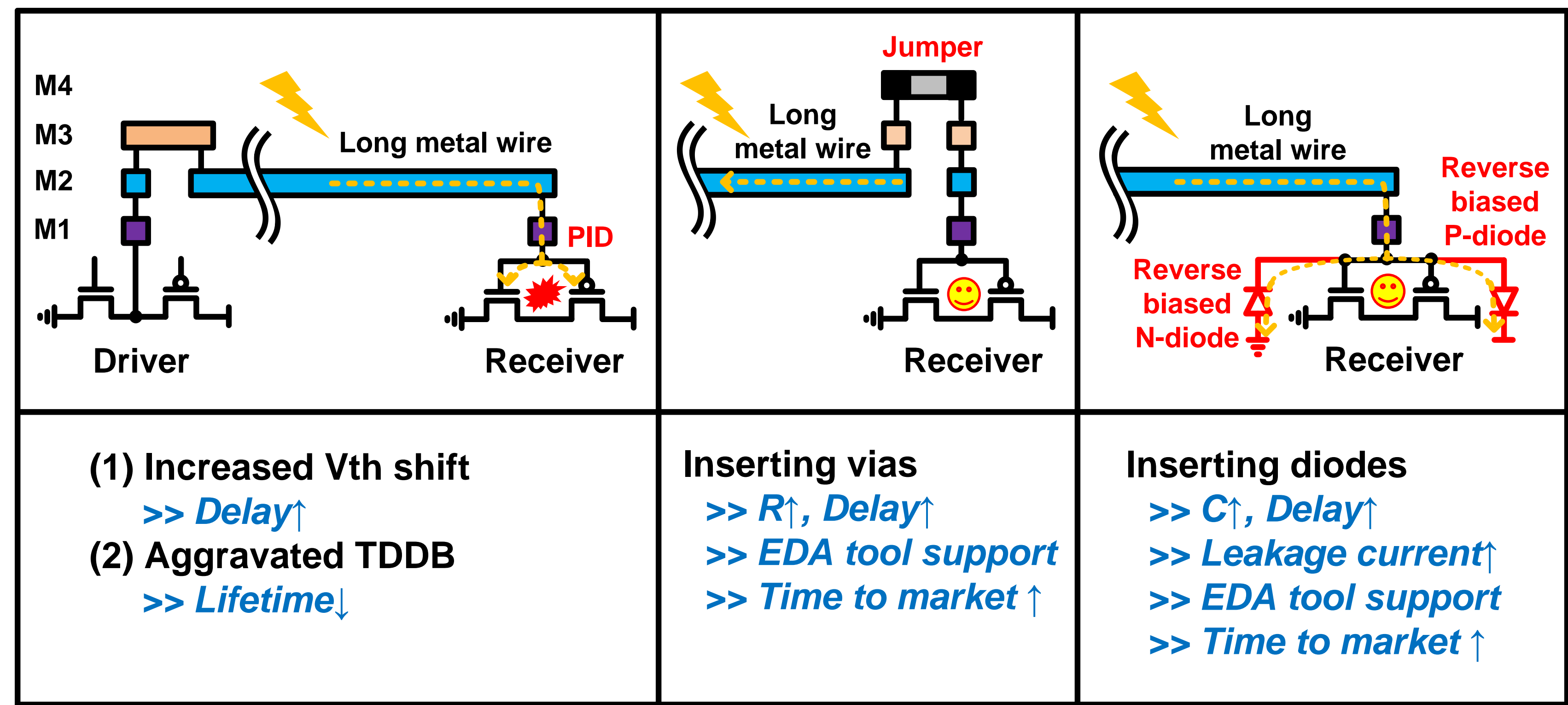
Plasma-Induced Damage (PID)



Z. Wang, *et al.*, ICICDT 2005

- **Plasma charge generated during the fabrication process leads to damage in the gate dielectric manifesting as latent device lifetime issue.**
- **The contiguous metal structure referred to as "antenna"**

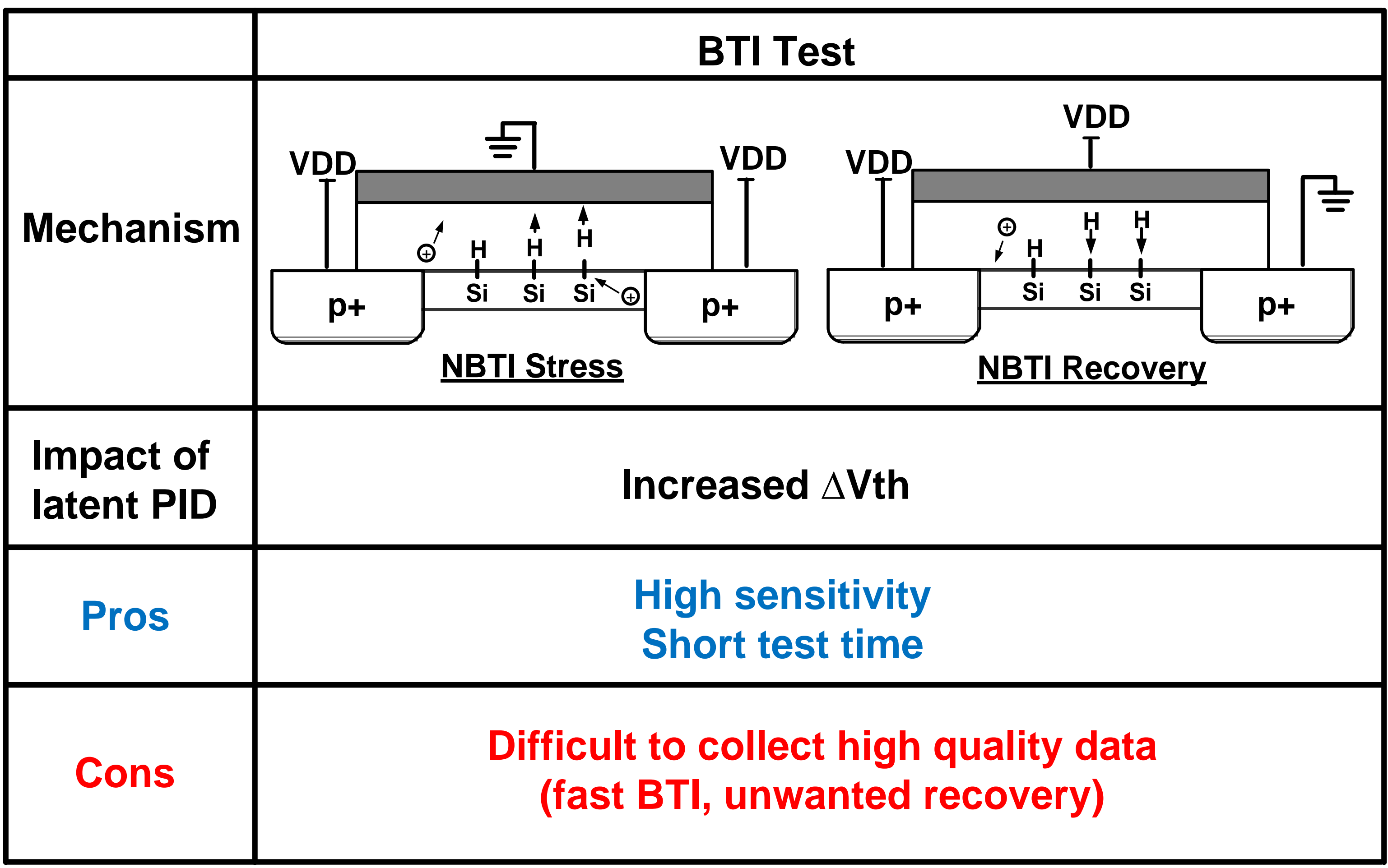
Circuit Impact and Mitigation Techniques



P. H. Chen, IEEE Circuits & Devices Magazine 2004

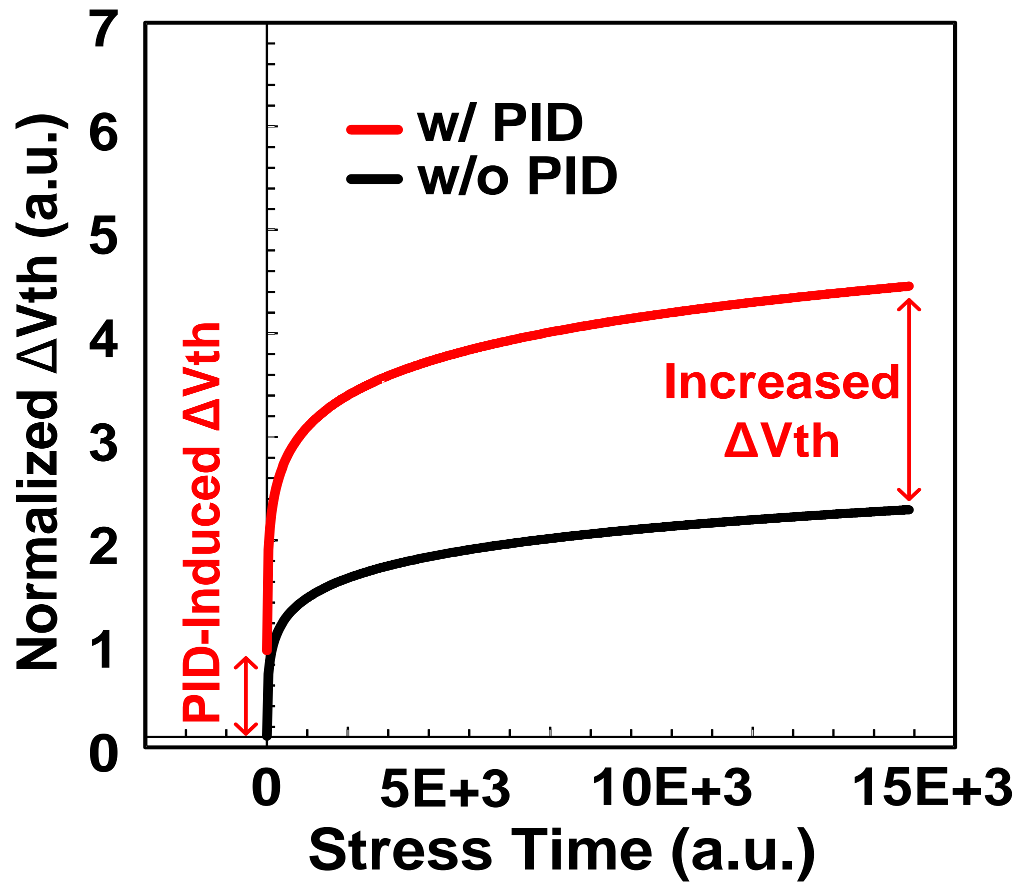
- **Mitigation techniques incur speed, power, cost, and time-to-market overhead**
- **PID impact on circuits need to be accurately assessed**

Characterizing Latent PID: BTI (Bias Temperature Instability) Test



	BTI Test
Mechanism	NBTI Stress / NBTI Recovery
Impact of latent PID	Increased ΔVth
Pros	High sensitivity Short test time
Cons	Difficult to collect high quality data (fast BTI, unwanted recovery)

Increased Vth Shift by “Latent” PID



- Initial Vth shift occurs on the device by “latent” PID
- After the device is being used, the Vth shift increases

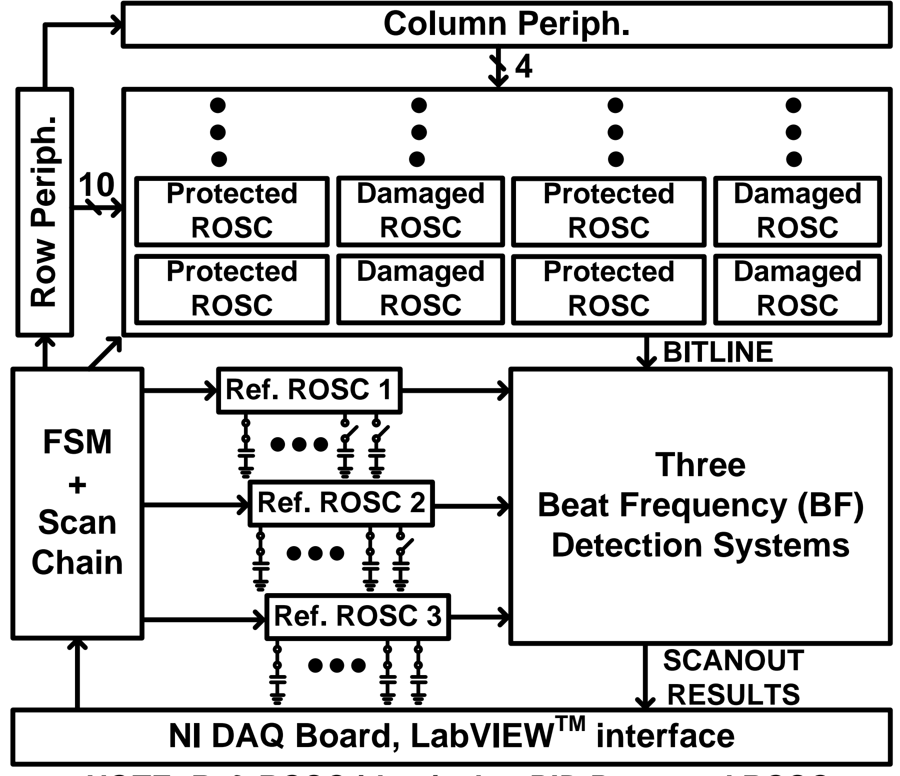
Comparison with Prior Art

	Device probing		Circuit based system	
	[1]	[2]	[3]	This work
Cell feature	Single device	1D Array	2D Array	2D Array
Schematic	Antenna, G, D, S	D, G, S, Antenna, Antenna, I_D	G, Antenna, Antenna, I_G, BL, Current-to-digital converter, Counting number	*Note: one stress cell is shown* Antenna, Antenna, Antenna, f, BL, Beat frequency system, Counting number
Parameter of interest	Increased ΔVth TDDB	Initial ΔVth	TDDB	Increased Δf
Silicon area	Large	Small	Small	Small
Measurement time	Long (Serial stress)	- (No stress purpose)	Short (Parallel stress)	Short (Parallel stress)
Measurement resolution	High	High	Limited	High
Sampling Time	Depends on tester speed (several milliseconds)	Depends on I/O BW (several milliseconds)	N/A	Short time interruption (>1μs*)

** For a 0.01% frequency shift Resolution and a ROSC period of 10ns, enable to minimize the unwanted BTI recovery*

[1] T.B. Hook, *et al.*, IRPS 2000 [2] P. Simon, *et al.*, TSM 2000 [3] W.H. Choi, *et al.*, IRPS 2013

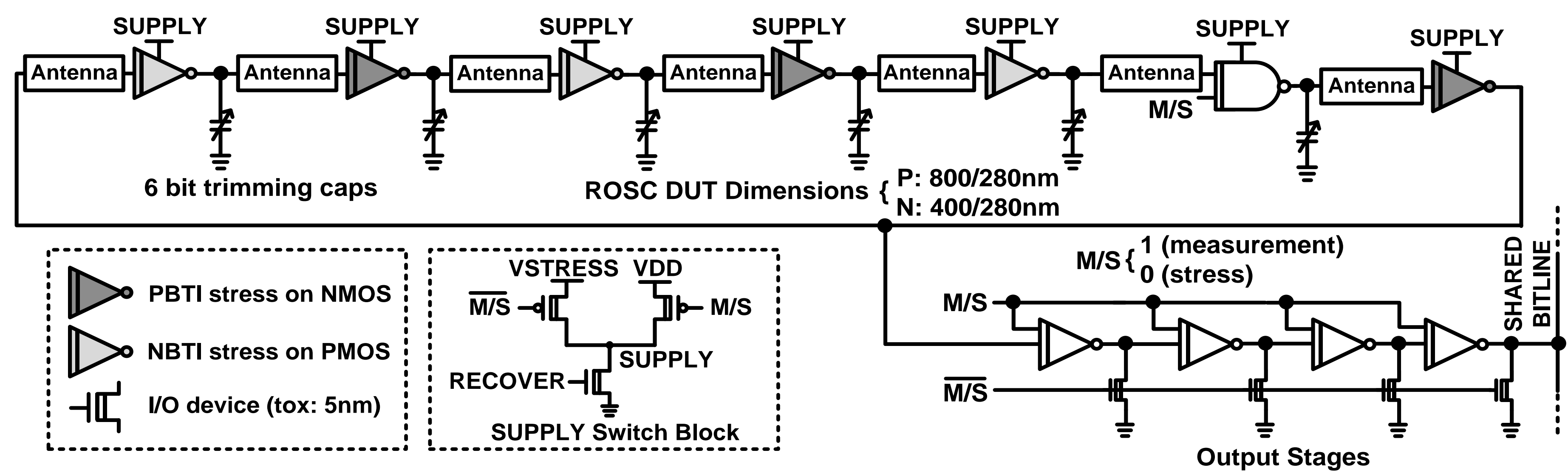
Proposed PID Characterization Circuit



NOTE: Ref. ROSC identical to PID Protected ROSC

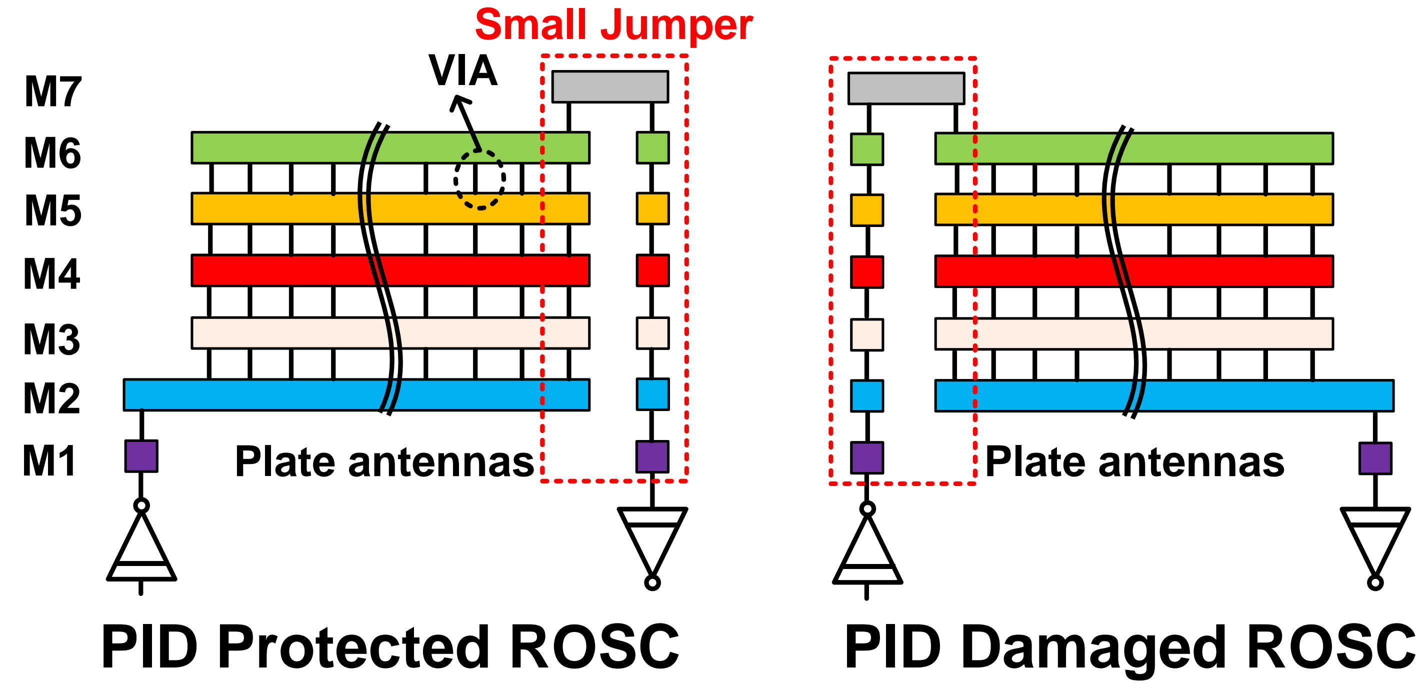
- **10x4 stress ROSC cells (two types: PID protected, damaged) array allows parallel stress/serial measurement capability**
- **3 reference ROSCs trimmed to various points in stressed ROSC frequency distribution**

PID Protected and Damaged ROSCs with Antenna Structures



- 5V DC stress, nominal 2.5V for the measurement
- The primary degradation mechanism is NBTI
- PID for 7 DUTs, NBTI degradation on PMOSs of 3 DUTs

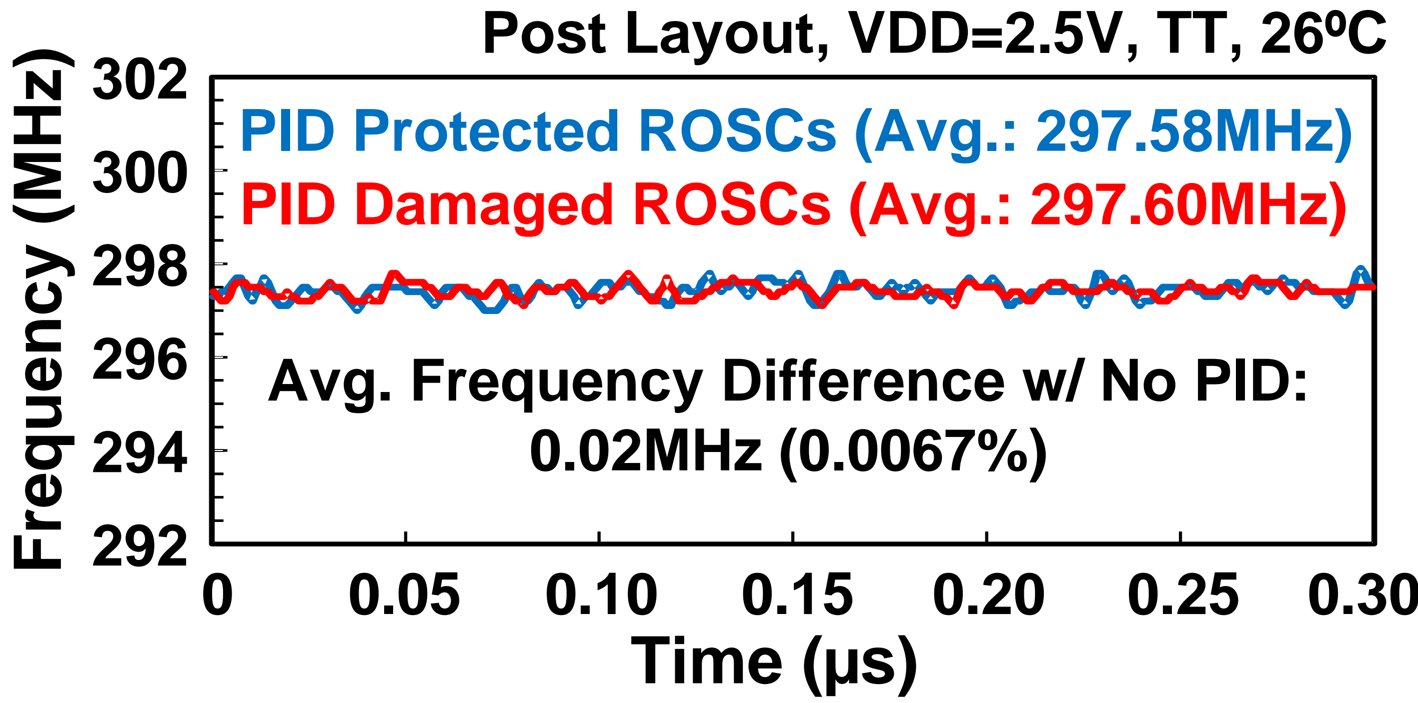
Cross-sectional View of a Single Stage



$$AR = \frac{\text{total surface area of antenna structure}}{\text{gate area}}$$

- **AR values of 4.4k (Metal) and 0.7k (VIA) were implemented in a single inverter stage**

Simulated Frequency Difference Between Two ROSC Types



- **Simulations showing negligible freq. difference between two ROSC types**

Beat Frequency Detection System

Stressed ROSC
(PID Protected or Damaged ROSC)

A

Phase Comp.

Beat Frequency Counter

B

Reference ROSC
(PID Protected ROSC)

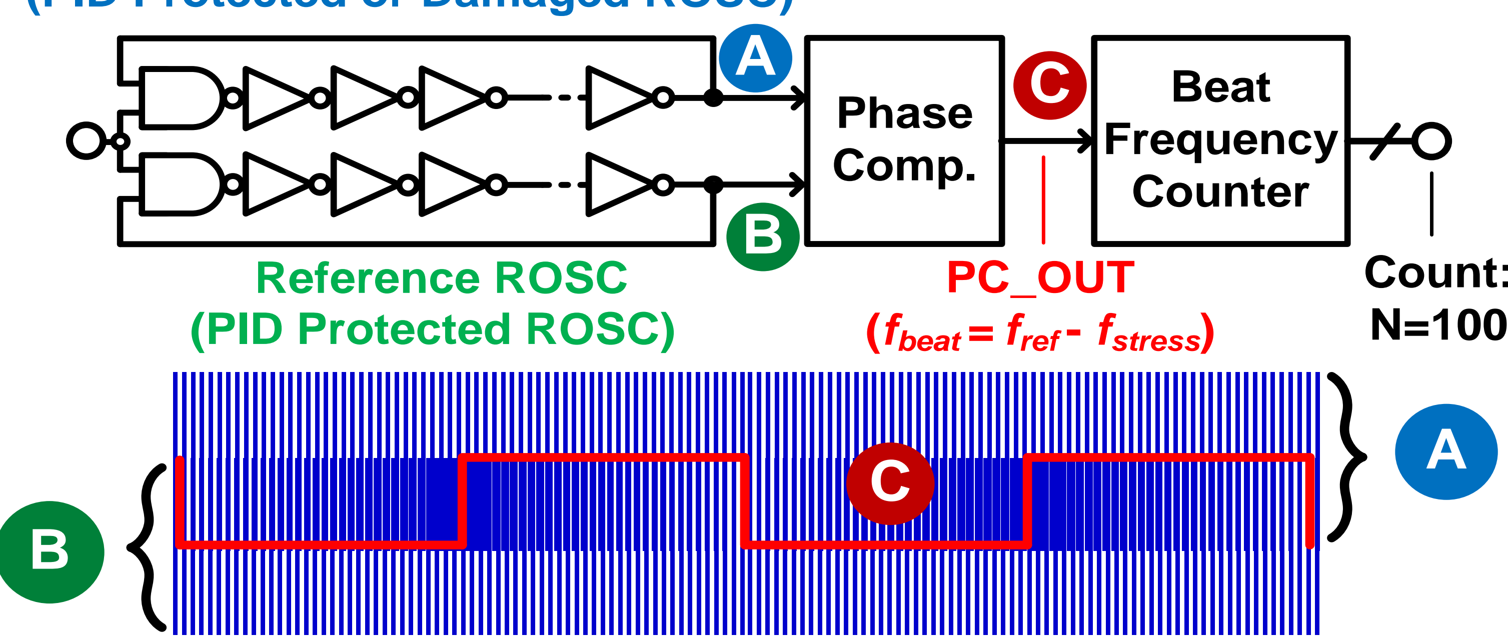
T.H. Kim, *et al.*, VLSI Circuits 2007

f_{str} : 0.99GHz — A

B — f_{ref} : 1.00GHz

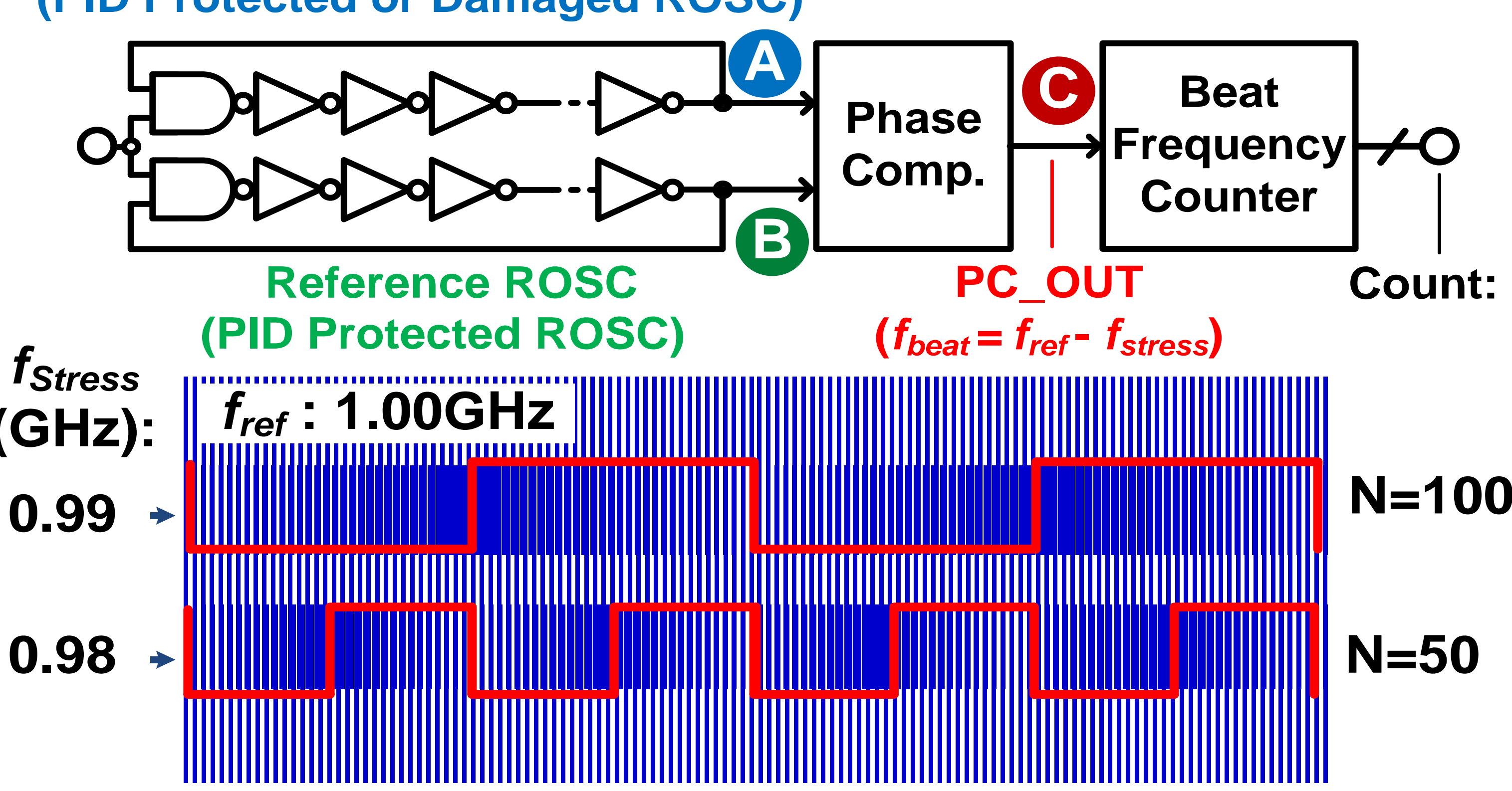
- Phase comparator is used to generate the beat frequency
- 3 benefits: high resolution (>0.01%), insensitive to common mode noise, fully-digital scan-based interface

Beat Frequency for a High Resolution



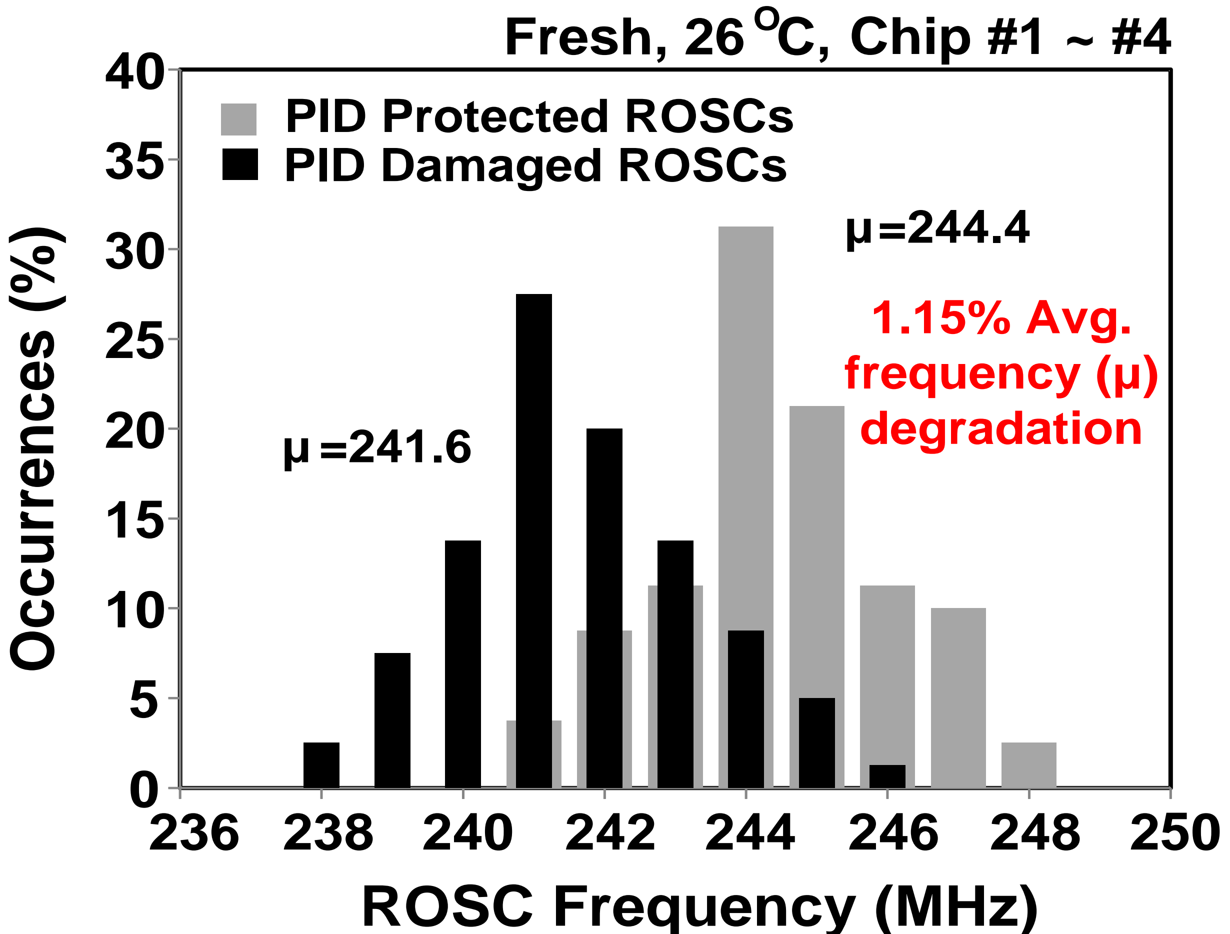
- Phase comparator output: $f_{beat}=f_{ref}-f_{stress}$
- Counter counts the number of reference cycles in one period of the beat signal

Beat Frequency for a High Resolution



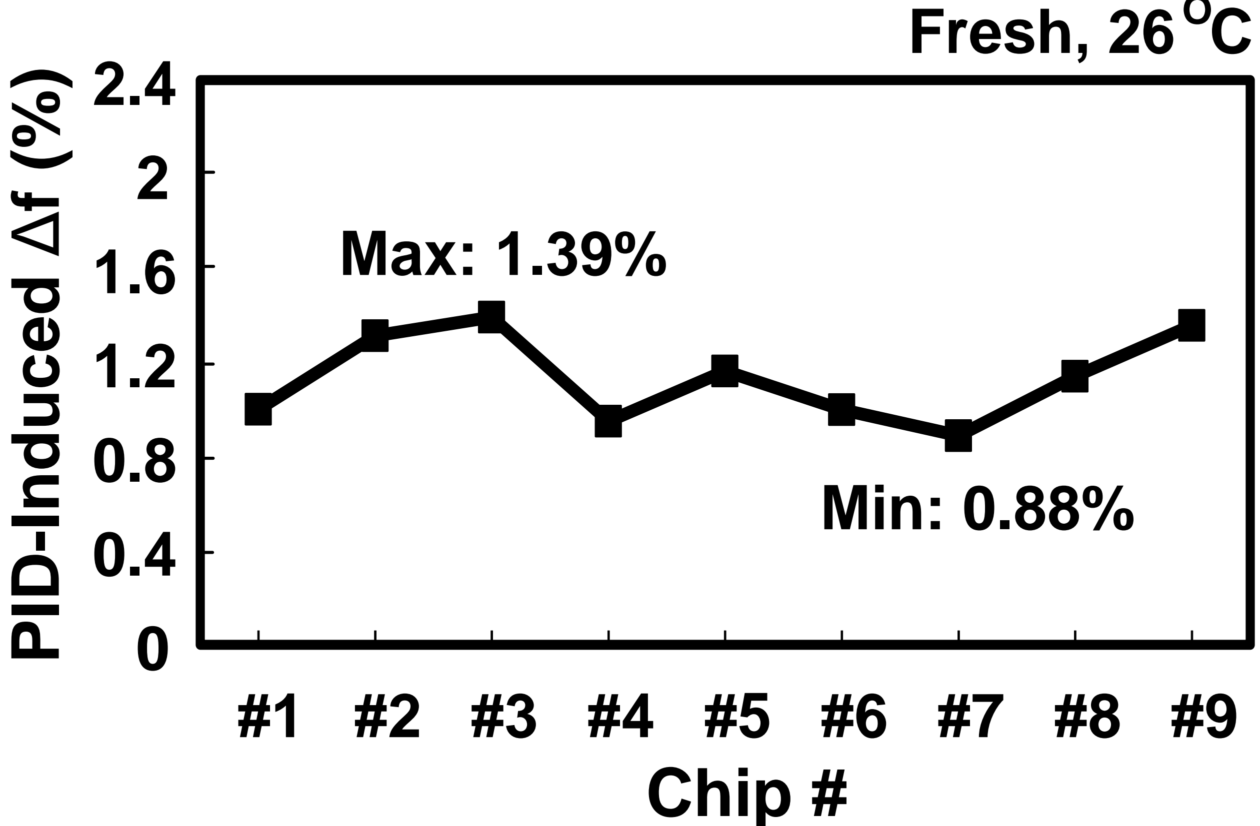
- 1% frequency difference before stress → N=100
- 2% frequency difference after stress → N=50
- Δf or ΔT sensing resolution is 0.01%

Measured Fresh Frequency Distributions



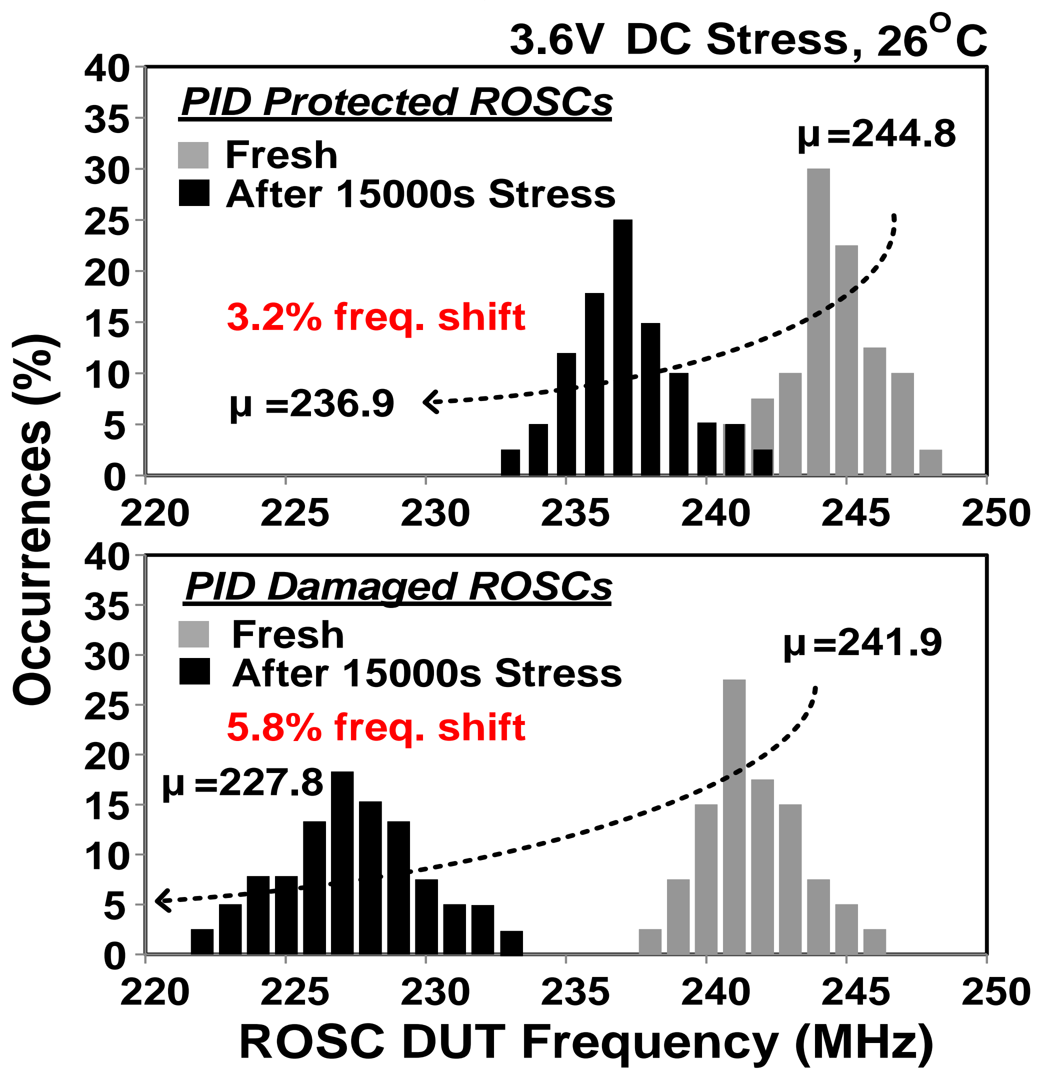
- 1.15% degradation in average frequency as a result of PID

Chip-to-Chip Variation

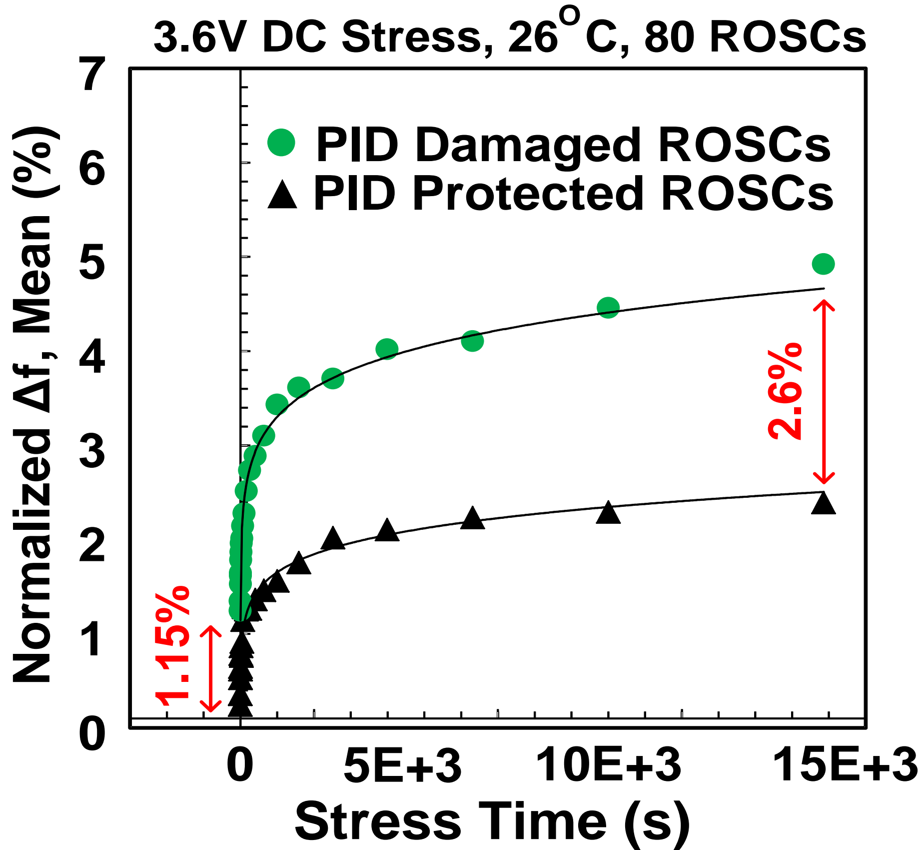


- Degradation trend in the average fresh frequency is consistent across different chips

Measured Freq. Degradation after 15000s, 3.6V DC Stress

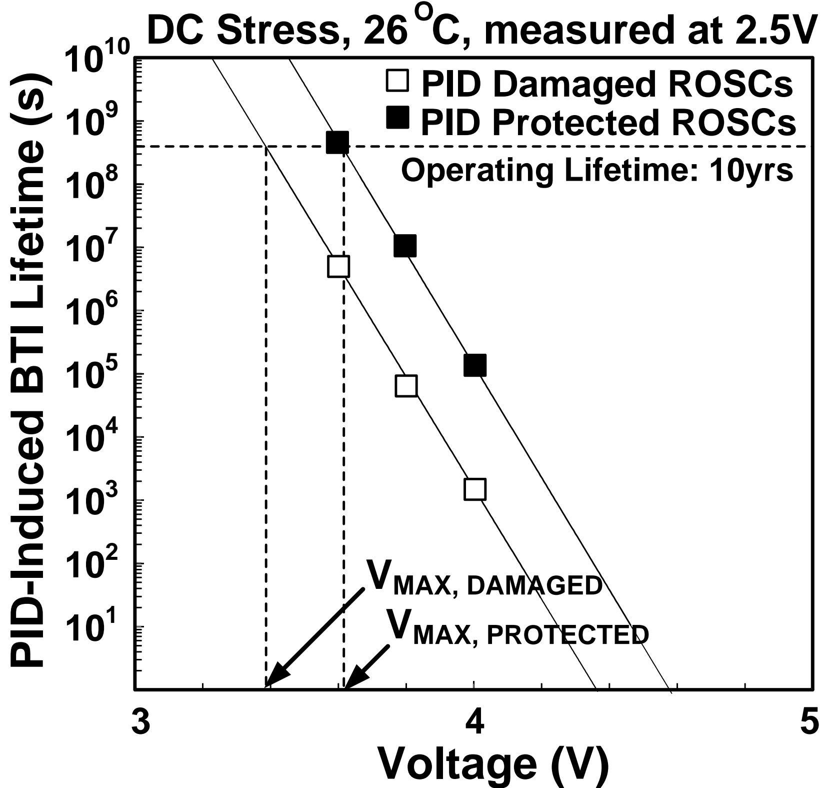


Measured BTI-Induced Frequency Shift



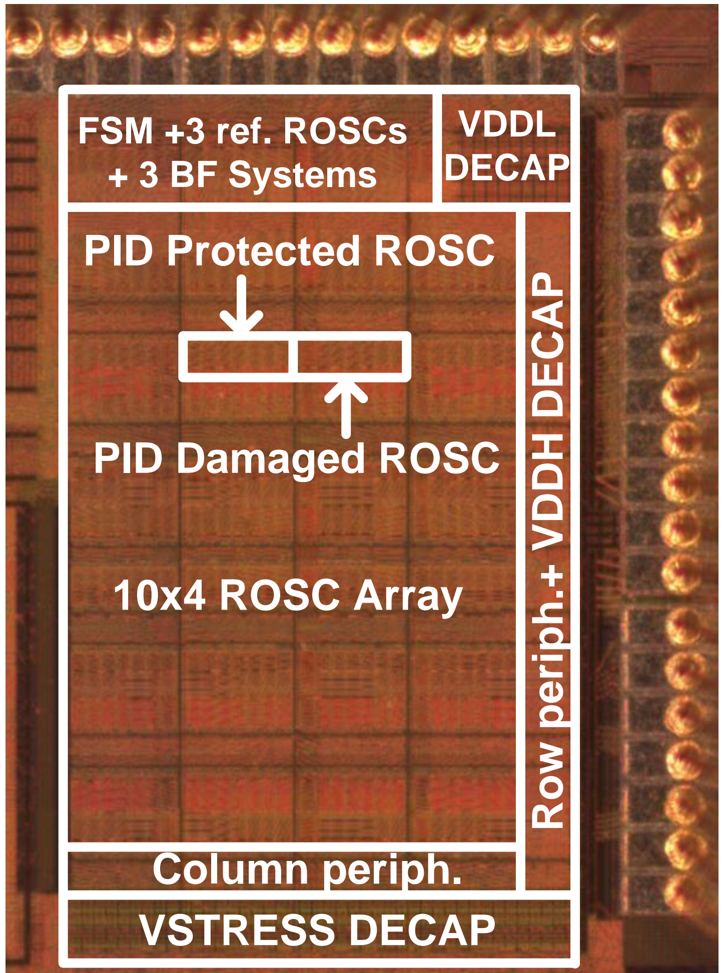
- The initial frequency shift of 1.15% between both ROSC types increases to 2.6% after 15000s, 3.6V DC stress

PID-Induced BTI Lifetime Projection from Measured Statistics



- The proposed test circuit would be equally useful in the prediction of PID-induced BTI lifetimes <u>with different ARs in any type of device with any topology of antenna structure under any fabrication process</u>

65nm Die Photo and Chip Features



Process	65nm LP CMOS, 7M
Core / IO Supplies	1.2V / 2.5V
Stress Voltage	3.6V, 3.8V, 4.0V
Measurement Voltage	2.5V
DUT Type	IO devices
ROSC DUT dimensions	P: 800/280nm N: 400/280nm
Δf Resolution	> 0.01%
Measure Interrupt	> 1μs
Total Area	496x767 μm^2

- Measured with LabVIEW & NI DAQ board

Conclusions

- **ROSC array-based PID characterization circuit with antenna structures fabricated in a 65nm process**
  - **To collect high quality massive PID-induced BTI statistics**
  - **It provides a high measurement precision (>0.01%) with a short measurement interrupt (>1μs)**
- **Measurement results confirm that circuits undergo PID-induced frequency degradation even before they are being used and therefore, the BTI lifetimes are reduced down the road.**