A Test Circuit Based on a Ring Oscillator Array for Statistical Characterization of Plasma-Induced Damage

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***Abstract*- We propose a test circuit for characterizing Plasma-Induced Damage (PID) based on a ring oscillator array for collecting high-quality BTI statistics. Two types of ring oscillators, PID protected and PID damaged, with built-in antenna structures were designed to separate PID from other effects. A beat frequency (BF) detection scheme was adopted to achieve high frequency measurement precision (>0.01%) in a short measurement time (>1μs) to prevent unwanted BTI recovery. The proposed circuit enables accurate PID-induced BTI lifetime prediction with different Antenna Ratios (ARs) in any type of device with any topology of antenna structure under any fabrication process. Measured frequency statistics from a 65nm test chip shows a 1.15% shift in the average frequency as a result of PID.**

I. Introduction

Plasma-Induced Damage (PID) has been an important concern for equipment vendors and fabs in both traditional SiO2 based and advanced high-k dielectric based processes [1-6]. Fig. 1 illustrates the PID phenomenon that occurs in a gate dielectric during the formation of a metal interconnect. The charge build-up in metal interconnects during the plasma processing steps introduces extra traps in the gate dielectric thereby worsening device reliability mechanisms such as Bias Temperature Instability (BTI) and Time Dependent Dielectric Breakdown (TDDB) [1-3, 6]. The contiguous metal structure where the charge build up occurs is commonly referred to as an "antenna."

Circuit designers rely on two methods to prevent the plasma process from imposing noticeable lifetime degradation [6]: (1) ensure that the Antenna Ratio (AR, defined as the area ratio between the antenna and the gate dielectric) does not exceed a given specification or (2) insert antenna diodes to provide other discharge paths. Unfortunately, circuit performance degradation is unavoidable even with the two methods for the following reasons: (1) previous studies have shown a noticeable difference in the PID-induced BTI lifetime for different ARs even within a given specification [3] or (2) inserted antenna diodes increase the capacitance of the metal interconnect, eventually making the circuit slower. To fully understand the impact of latent PID on device and circuit reliability, an efficient PID characterization method is needed.

Existing approaches for characterizing PID effects can be classified into four categories [6]: (1) Measuring the gate-leakage current on fresh devices is a simple and fast method, but suffers from low sensitivity [1-2]. (2) Measuring the TDDB under constant voltage stress is accurate and provides higher sensitivity, but requires a long test time of over 1000 seconds per sample [1-2]. (3) Ramped-voltage TDDB test was introduced in [1] to reduce the TDDB test time to 2 seconds per sample, but the main drawback is that the results do not match the standard TDDB results very well. (4) Measuring the remaining BTI lifetime has been generally accepted as the most effective method to detect latent PID, but only limited data have been reported so far as the unwanted BTI recovery [3] makes it difficult to collect high-quality BTI statistics.

Optimizing the plasma process and using proper operating conditions based on accurate PID-induced BTI lifetime predictions

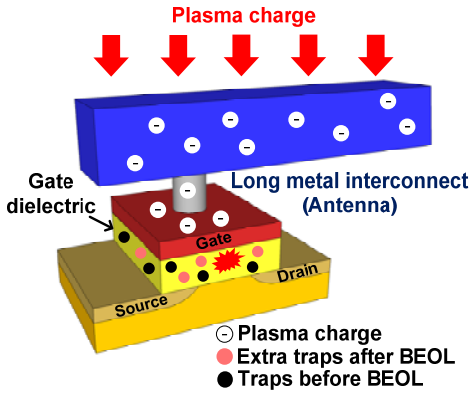


Fig. 1. Plasma-Induced Damage (PID) occurs during the back-end plasma processing resulting in BTI and TDDB issues.

under different ARs is the most practical and effective PID mitigation strategy (Fig. 2). Traditionally, characterization of PID-induced BTI degradation has involved continuously monitoring the transistor threshold voltage shift for a large population of devices using individual probing [3]. This method, however, is time-consuming and cumbersome due to serial stress. Furthermore, the test setup has to support fast measurements (e.g., within a microsecond) to suppress unwanted recovery. This requires an elaborate setup in which the device is periodically taken out of stress, measured under a nominal supply, and then switched back to a stress mode.

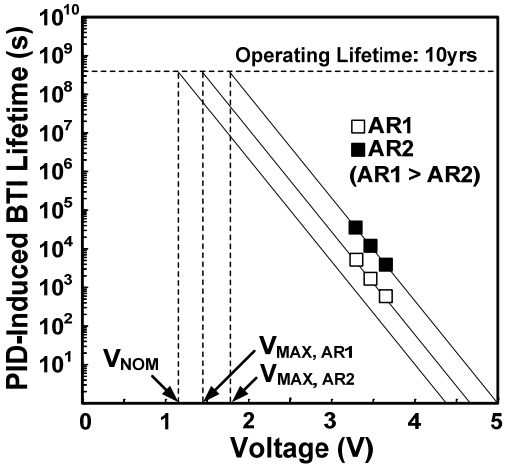


Fig. 2. PID-induced BTI lifetime projection for different Antenna Ratios (ARs) based on accelerated stress involves mass data collection.

In this work, we demonstrate for the first time a dedicated characterization circuit based on a ring oscillator (ROSC) array, capable of measuring PID-induced frequency shifts with a high precision (>0.01%) and short measurement time (>1μs). Additional benefits over traditional device probing include a reduced test silicon area, shorter test times, and simpler and more flexible test setups.

II. PROPOSED PID CHARICTERIZATION CIRCUIT DESIGN

Our proposed PID characterization circuit shown in Fig. 3 consists of an array of 40 ROSC cells, a finite state machine (FSM), a scan based interface, and three BF detection systems. Two types of ROSCs, a PID protected ROSC and a PID damaged ROSC, are designed using different antenna connections. Details of the antenna configuration are provided in the following section. The reference ROSCs are identical to the PID protected ROSCs in the test array. One ROSC is selected at a time from the large array for the frequency measurements using column and row select signals. Output of the selected ROSC toggles the shared bitline signal which is multiplexed out to the BF detection system for on-chip frequency measurements. Each ROSC has 7 delay stages with antenna structures attached to each stage as shown in Fig. 4. Both ROSC types are identical except

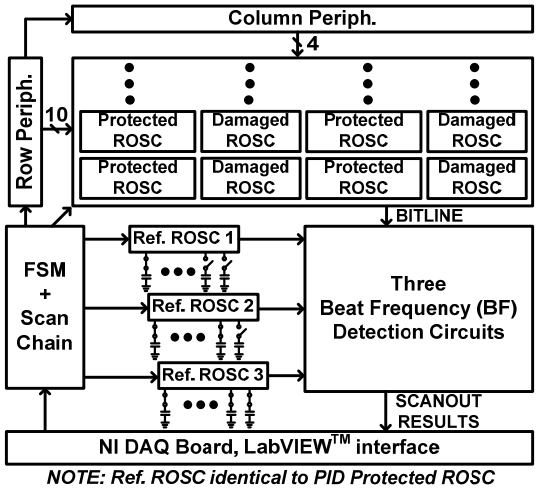


Fig. 3. Diagram of proposed array-based PID characterization circuit.

for the antenna connection. By measuring the frequency difference between the two structures, we can effectively separate out the PID effect. The inverter stages in each ROSC are implemented using standard 2.5V thick oxide I/O devices. Although both thin oxide and thick oxide devices can be considered, we chose to use the latter option as previous work indicates that devices with thicker oxides are more susceptible to PID effects [3]. Note that the proposed characterization method would be equally useful and perhaps more effective in measuring latent PID effects in thin oxide devices by building larger arrays.

The supply voltage of each ROSC can be independently switched between stressed voltage (VSTRESS), nominal supply (VDD), and 0V using the on-chip power gates depicted in Fig. 4. This allows us to collect both the fresh and stressed frequency distributions. During stress, the ROSC loops are opened so that DC stress can be applied to the ROSC devices. During the measurement mode, the supply voltage of the selected ROSC is switched to a nominal supply using the power gate while the other ROSCs are kept in the stress mode. Subsequently, the M/S signal is asserted and the selected ROSC generates a frequency output which is paired with a fresh reference. Note that the reference ROSCs are kept fresh (i.e., 0 V supply) during the long stress periods and are only activated (i.e., nominal supply) during the short measurement times. The frequency degradation is measured using the BF detection scheme shown in Fig. 5 [7]. This technique can achieve sub-picosecond frequency shift resolution by measuring the frequency difference between two free-running ROSCs [7]. The operating example in Fig. 5 shows that a 1% shift in the stressed frequency corresponds to a 50% change in the output count. To achieve high measurement precision for the entire frequency range of the test array, three reference ROSCs with slightly different frequencies were employed [8].

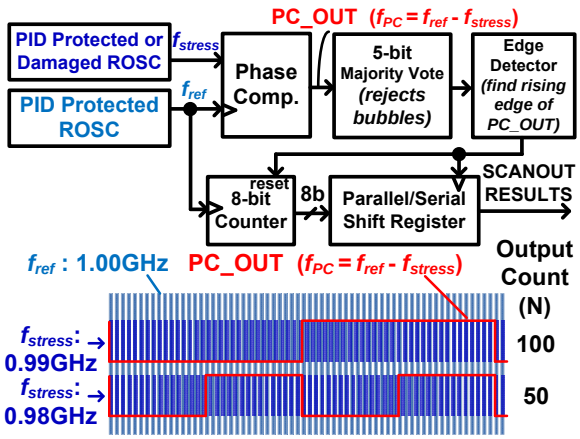


Fig. 5. Beat frequency detection system achieves a high frequency shift precision (>0.01%) and a short (>1μs) stress interrupt time for precise BTI measurements.

III. ANTENNA DESIGN

Plate type antennas were inserted in each ROSC stage as shown in Figs. 6 and 7. Since we want only the PID damaged ROSC to be affected by the plasma charge, we adopted a jumper technique in which the position of a small M7 jumper and a small wire was

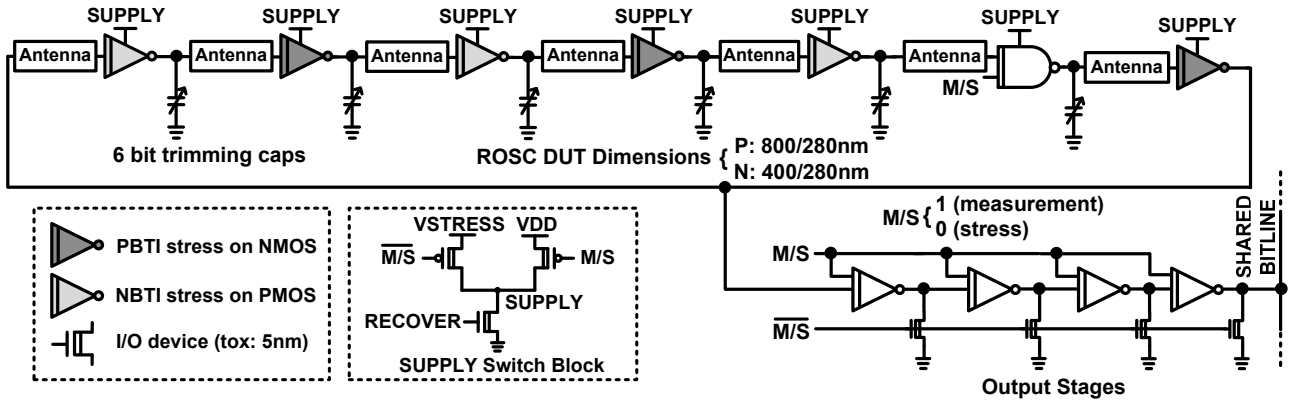


Fig. 4. Schematic of PID protected and damaged ROSCs. Aside from the antenna connection (Fig. 6), the two ROSCs are identical and thus any difference in measured frequency can be attributed to PID.

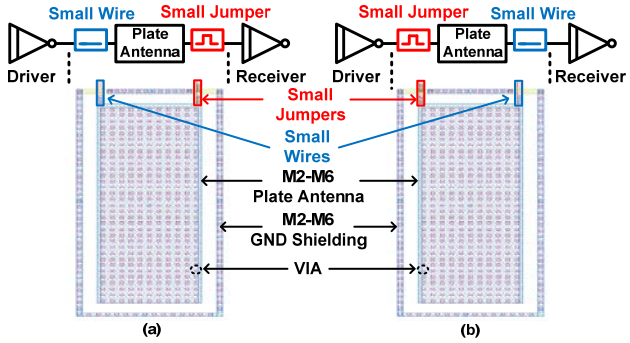


Fig. 6. Schematic and layout view of a single stage of (a) PID protected ROSC and (b) PID damaged ROSC.

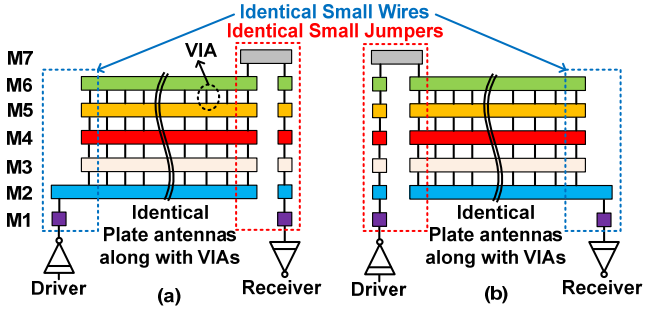


Fig. 7. Cross-sectional view of a single stage of (a) PID protected ROSC and (b) PID Damaged ROSC.

swapped in the two ROSC types. In this way, PID damage is protected in the load transistors which are connected to antennas through a jumper structure. In contrast, PID damaged ROSCs are indeed affected by PID since a plasma charge can discharge only through the gate dielectric of the load transistor. Fig. 8 shows the simulated frequencies of both types of ROSCs from the post-layout RC extracted netlist indicating a negligible frequency difference of 0.02MHz (or 0.0067%). This ensures that any frequency difference greater than this amount can be attributed to PID. The top surface areas for each metal layer along with the total antenna area are listed in Fig. 9. To maximize the amount of PID in dense chip implementation, the antenna utilizes a dense M2-M6 metal stack with numerous VIAs between the different layers. Here, M1 and part of the M2-M4 layers were used for the signal and power routing tracks. The total AR is 4464 for the metal wires and 721.79 for the VIAs.

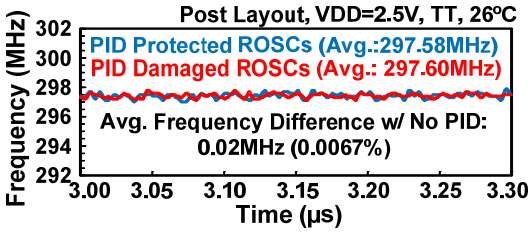


Fig. 8. Simulations showing negligible freq. difference between the two ROSC types.

	Metal	VIA
M5, M6	300µm^2	43.15µm^2
M2, M3, M4	300µm^2	52.07µm^2
Total antenna area of each DUT	1500µm^2	242.52µm^2
AR (Antenna Ratio)	4464	721.79

$$AR = \frac{\text{total surface area of antenna structure}}{\text{gate area}}$$

Fig. 9. Antenna area of each metal layer and total AR.

IV. Statistical Frequency Measurements

A test chip was fabricated in a 65nm CMOS process and measurements were fully automated through a data acquisition board controlled by LabVIEWTM software. Fig. 10 shows the measured fresh frequency distributions for both types of ROSCs. The average fresh frequency of PID damaged ROSCs is 1.15% lower than that of the PID protected ROSCs. A consistent trend is measured across different chips (Fig. 11). Figs. 12 and 13 show the measured frequency distributions after a 1000-second DC stress along with the fresh distributions under 3.6V and 4.0V stress voltages. The degradation of the average frequency for the PID protected ROSCs and PID damaged ROSCs are 2.5% and 4.4%, respectively, for 3.6V stress voltage. Similar trends is measured for stress voltage of 4.0V. Our experiment results confirm that circuits undergo PID-induced BTI degradation even before they are functional. Fig. 14 shows the measured mean and standard deviation of the frequency shifts (i.e., Δf) at 3.6V and 4.0V stress voltages. The mean and standard deviation of the frequency shift for both ROSC types follow power law dependency. The time slope of the mean is measured to be roughly twice that of the standard deviation.

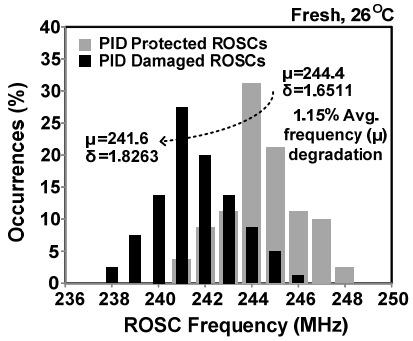


Fig. 10. Measured fresh frequency distributions show a 1.15% degradation in average frequency as a result of PID.

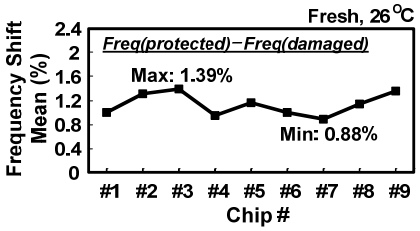


Fig. 11. Degradation in the average fresh frequency measured from different chips shows a consistent trend.

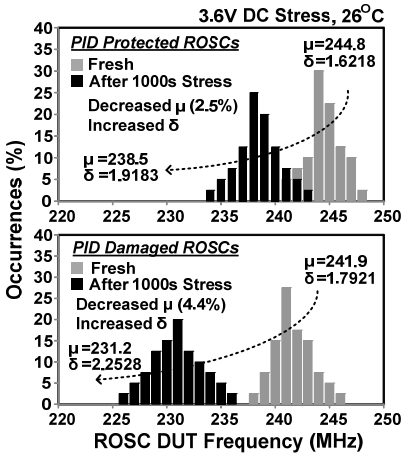


Fig. 12. Frequency distribution before and after a 1000 sec, 3.6V DC stress for PID protected and PID damaged ROSCs.

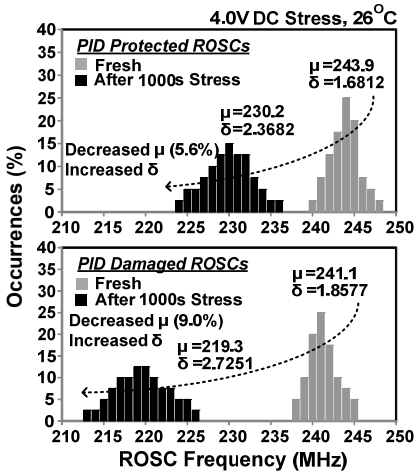


Fig. 13. Frequency distribution before and after a 1000 sec, 4.0V DC stress for PID protected and PID damaged ROSCs.

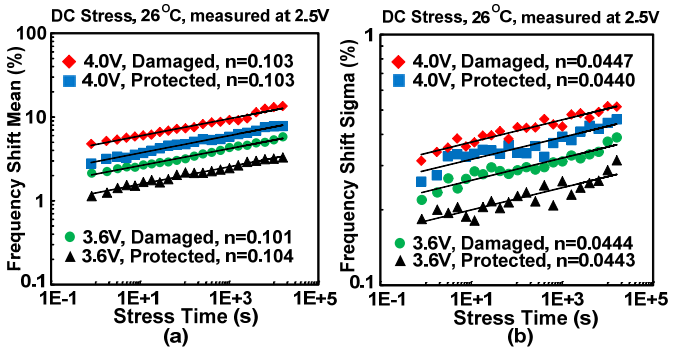


Fig. 14. Measured (a) mean and (b) standard deviation of BTI induced frequency shift for the two ROSC types.

V. PID-INDUCED BTI LIFETIME PREDICTION

Fig. 15 compares PID-induced BTI lifetime for PID protected and PID damaged ROSCs. We observe that the projected V_{MAX} of PID damaged ROSC is smaller than that of PID protected ROSC. Note that the proposed test circuit would be equally useful in the prediction of PID-induced BTI lifetimes with different ARs in any type of device with any topology of antenna structure under any fabrication process. A 65nm test chip die photo with the chip summary is shown in Fig. 16.

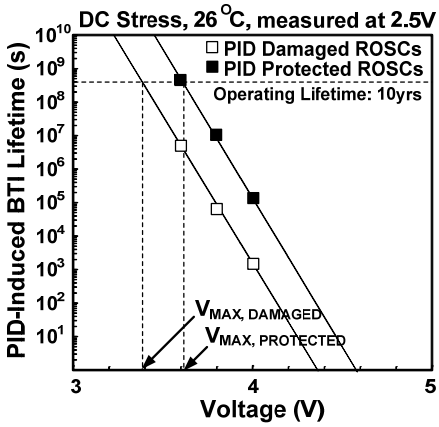
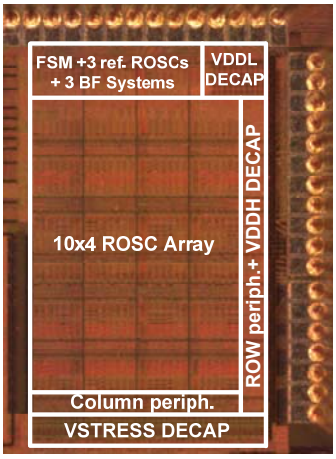


Fig. 15. Comparison of projected PID-induced BTI lifetimes for PID protected and PID damaged ROSCs are performed from measured statistical data.



Process	65nm LP CMOS, 7M
Core / IO Supplies	1.2V / 2.5V
Stress Voltage	3.6V, 4.0V
Measurement Voltage	2.5V
DUT Type	IO devices
ROSC DUT dimensions	P: 800/280nm N: 400/280nm
Δf Resolution	> 0.01%
Measure Interrupt	≥ 1μs
Total Area	496x767 μm²

Fig. 16. 65nm test chip die photo with chip summary.

VI. CONCLUSION

Optimizing the plasma process and using proper operating conditions based on accurate PID-induced BTI lifetime predictions under different ARs is the most practical and effective PID mitigation strategy. However, the main challenge with this approach is collecting the massive PID-induced BTI statistical data from accelerated tests in a short measurement time to prevent unwanted BTI recovery. In this work, we propose a test circuit for the statistical characterization of PID based on a ring oscillator array for collecting high quality BTI statistics. Two types of ring oscillators with built-in antenna structures, namely the PID protected and PID damaged ROSCs, were designed in the test circuit to separate PID from other effects. The adopted beat frequency (BF) detection scheme achieves high frequency measurement precision (>0.01%) in a short measurement time (>1μs) to prevent unwanted BTI recovery. Measured frequency statistics from a 65nm test chip shows a clear shift in average frequency as a result of PID. Our experiment results confirm that circuits undergo PID-induced BTI degradation even before they are functional.

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