A VCO-Based ADC Employing a Multi-Phase Noise-Shaping Beat Frequency Quantizer for Direct Sampling of Sub-1mV Input Signals

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***Abstract*- A VCO-based ADC featuring a multi-phase beat frequency based quantization scheme with first order noise shaping is demonstrated in a 65nm CMOS process. The proposed ADC is unique in that it can achieve high resolution (e.g. 6-7 ENOB) for signals with extremely small amplitudes (e.g. <1mV). This allows us to remove or simplify the pre-conditioning amplifiers, reducing power consumption as well as the overall system complexity. The proposed ADC achieves 43dB SNDR for a 1mV input signal while achieving a 10kHz bandwidth and 300kHz sample rate, and consumes 36µW at a 1.2V supply.**

I. Introduction

Analog-to-Digital Converter (ADC) is a critical building block for ultra-low power applications such as wireless sensor nodes and bio-potential (e.g. ECG, EEG, neural recording) monitoring systems. Significant progress has been made recently in the area of energy-efficient ADC design including SAR-ADCs for sensor and medical applications boasting microwatt level power consumption by adaptively changing the sampling rate and resolution based on the system level specifications [1, 2]. Despite these advances, the actual performance improvement experienced by the end-user may be rather limited due to the power and area overhead of auxiliary circuits such as the multiple stage amplifiers required for signal pre-conditioning (Fig. 1, upper). Most ADC papers ignore the design complexity and power overhead of various amplifiers by assuming an ideal rail-to-rail input signal. Not only does this situation obscure the true benefits at the system level, the device noise in the amplifiers is neglected resulting in an overly optimistic performance estimate. Recently, a Beat Frequency based ADC (BF-ADC) scheme has been proposed for direct analog-to-digital conversion of small input signals which can eliminate amplifier circuits all together from the system [3]. In this paper, we present details of a new BF-ADC with an improved SNDR and a higher sampling rate by using a multi-phase noise-shaping BF quantizer. Experimental data from a 65nm test chip shows a 43dB SNDR when directly sampling a 1mV input signal. The measured SFDR was 57dB.

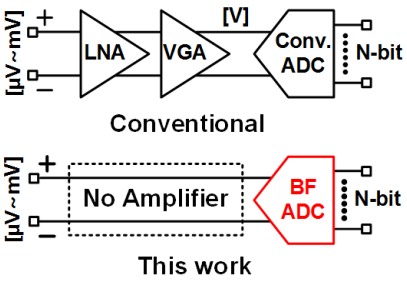

Fig. 1. The focus of this work is on direct analog-to-digital conversion of small (e.g. <1mV) input signals which could allow us to get rid of the power hungry pre-conditioning amplifiers.

II. Basic Concept of Beat Frequency Based Quantizer

The proposed BF based quantization scheme is compared with the conventional VCO based ADC scheme in Fig. 2. The conventional quantizer (Fig. 2, upper) counts the number of VCO clock periods (CK_{IN}) in each sampling clock period (CK_S), thereby generating a count output corresponding to the input voltage. For good linearity and high gain, the raw analog input of the conventional scheme must be adequately amplified and level shifted before it can be used as a VCO bias. The proposed BF based quantizer (Fig. 2, lower) on the other hand, measures the beat frequency (BF) between two similar frequencies (i.e. $f_{BF}=f_{REF}-f_{IN}$) to amplify small changes in the input frequency into a large measurable count output (i.e. D_{OUT}). This allows us to eliminate the frontend amplifiers (e.g. LNA and VGA) from the system, reducing the power and area overhead and simplifying the overall design complexity [3]. To illustrate this point better, let's consider an example in which the initial frequency difference between CK_{REF} and CK_{IN} is 1%. This gives a count output of 100 as it takes 100 clock cycles for the fast clock to pass, catch up, and overtake the slow clock. Now, suppose the frequency difference becomes 1.01% due to a miniscule change in the input signal. This translates into an output count of 99 since it takes one less cycle for the fast clock to catch up with the slow one. In contrast, to obtain the same count change of 100 to 99, the conventional VCO-based quantizer in Fig. 2 (upper) would have required a much larger change in frequency (1% rather

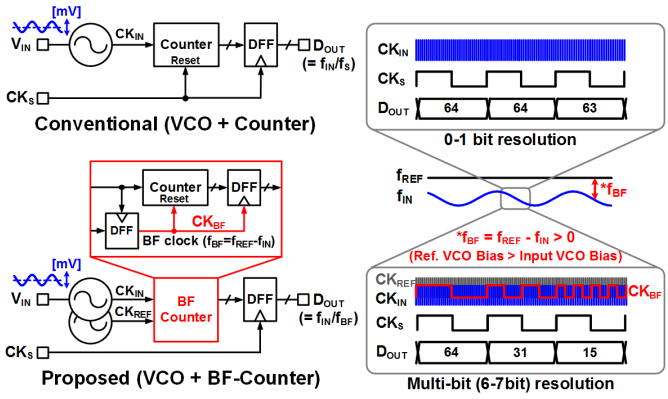

Fig. 2. Comparison between conventional and proposed VCO-based quantizers. The proposed circuit achieves a high resolution (e.g.6-7bit) for a small input signal (e.g. <1mV) by incorporating a BF counter which can detect an input voltage difference as small as 0.01mV. A single-ended input example is shown here, though differential sensing is also possible.

than 0.01%) which translates into a 100x lower sensitivity. Note that the CK_{REF} frequency in the BF quantizer must be configured to be close to the CK_{IN} frequency (typically within 1-5%) for sufficiently high resolution. This can be readily achieved using an identical VCO with a common mode reference bias.

III. Noise-Shaping and Multi-Phase BF Quantization

In addition to exploiting the BF quantizer's inherently high sensing resolution, the proposed work further improves the ADC performance by oversampling the input voltage with a noise-shaping BF quantizer described in Fig. 3. The previous design in [3] resets the VCO after each BF clock period and as a result, the quantization error at the end of each BF cycle is lost (Fig. 3, left). By contrast, the proposed quantizer measures each BF clock cycle without resetting the VCO. By doing so, the quantization error is passed on to the next cycle and hence accounted for (Fig. 3, right). In addition to accomplishing first-order noise-shaping, the sampling rate is maximized since there is no dead period between samples.

Another technique we employed to improve the ADC resolution is a multi-phase VCO for measuring multiple BF periods from a single VCO. Fig. 4 shows the basic idea using a simplified 7-phase ring oscillator as an example circuit. Here, the output of each delay stage is utilized for reducing the phase offset and thus achieves a finer timing resolution. The previous design used a single-phase clock which limits the timing resolution to one oscillation period of the VCO. By using a 31-phase ring oscillator, the SNDR is improved by 10dB compared to its single-phase counterpart.

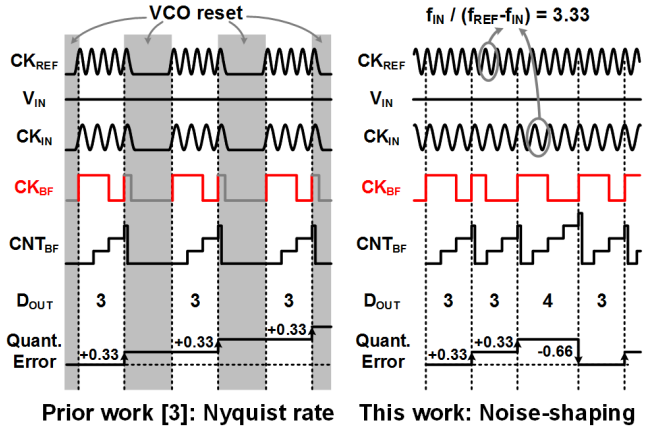

Fig. 3. First-order noise-shaping is achieved by counting the number of CK_{IN} periods in each BF cycle without any interruption. The simplified example shown here is for a small BF count number of 3 or 4.

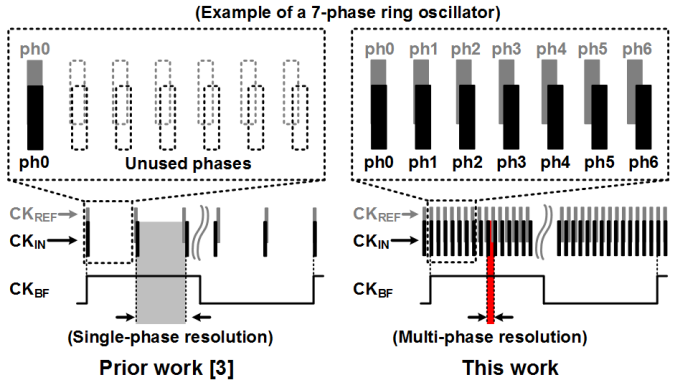

Fig. 4. Multi-phase BF quantization improves the timing resolution by a factor of N where N is the number of phases in the ring oscillator.

IV. Conversion of BF Code to Linear Code

Fig. 5 show how the beat frequency code is utilized in the previous and new BF-ADC designs. The previous single-phase implementation requires a decoder (denoted as BF DEC

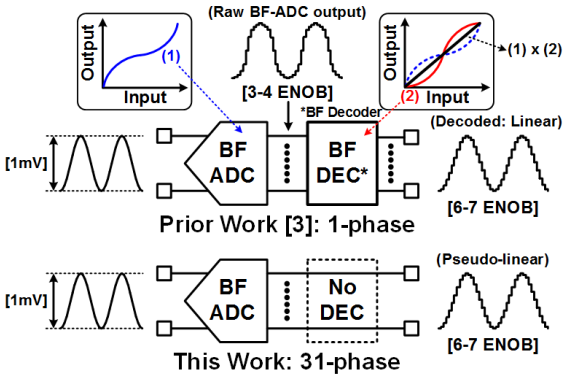

Fig. 5. Converting non-linear BF output code to a linear code. The proposed multi-phase design does not require BF decoding by incorporating a multi-phase BF quantization scheme which could result in a high resolution (6-7 ENOB) for a narrow (i.e. pseudo-linear) BF output code range.

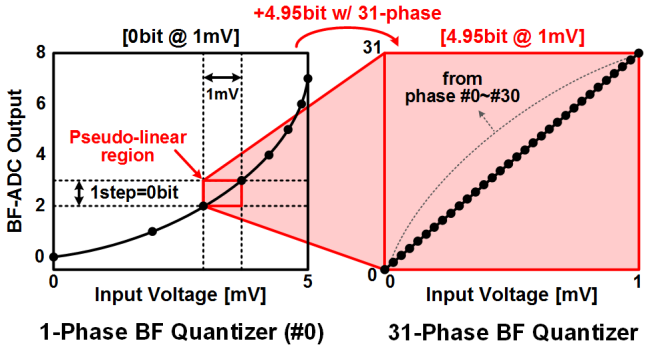

Fig. 6. Input voltage versus BF output code showing that a 31-phase design can improve the ADC resolution by 4.95 bits compared to a single-phase design. For illustration purpose, a single-ended (i.e. not differential) BF-ADC is assumed here.

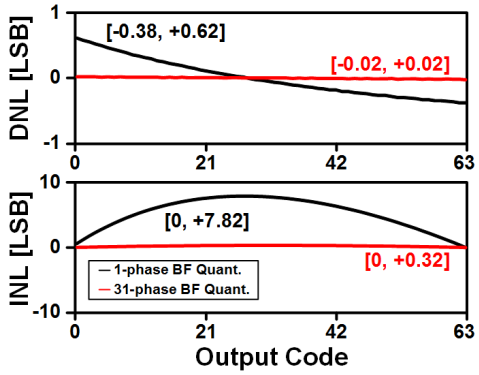

Fig. 7. DNL/INL for a 6 bit BF quantizer output before any BF decoding is applied. Output BF code for a single-phase VCO ranges from 100 to 163, while the 31-phase VCO has a wider output range of 3100~3163. Output code range shown here is from the minimum code (i.e. 100 or 3100) to the maximum code (i.e. 163 or 3163) depending on the number of phases.

in Fig. 5) for converting the non-linear BF-ADC output code to a linear code. In contrast, the output code of the new multi-phase design can be directly used by the subsequent blocks due to the higher resolution and superior linearity. This is possible due to the fact that the proposed multi-phase design increases the number of conversion steps by a factor of N where N is the number of phase outputs available. This can be seen in Fig. 6, where a single conversion step in the previous single-phase BF-ADC is further divided into 31 levels, offering a 4.95-bit resolution for each conversion step of the single-phase BF-ADC. Fig. 7 shows the simulated ADC linearity results before any decoding is applied for a 6-bit BF-ADC. For producing the same 6 bit outputs, we assumed the output range is [100, 163] for the single-phase design and [3100, 3163] for the 31-phase design. As a result, BF quantization with 31 additional levels shows a significantly lower DNL and INL (i.e. [-0.02, 0.02], [0, +0.32]) as compared to the values from its single-phase counterpart (i.e. [-0.38, +0.62], [0, +7.82]).

When dealing with circuit elements such as flip-flops or voltage comparators used to discern small differences in signal timing or voltage levels, metastability becomes a common concern. Although rare, metastability could cause logic failures and negatively impact the ADC linearity. The topic of metastability in VCO-based quantizers deserves a separate in-depth treatment. However, previous work on VCO-based

	Conventional VCO-based	Previous BF-ADC [3]	This work
Quantization Scheme	Linear Counting	Beat Freq. Counting	Beat Freq. Counting
Freq. Detection Sensitivity* (@ 100 counts)	Low (1%)	High (0.01%)	High (0.01%)
Noise-Shaping	Yes	No	Yes
Multi-Phase	Yes	No	Yes
BF Code Utilization	-	Wide (Nonlinear)	Narrow (Pseudo-linear)
BF Decoding	-	Required	Not Required

*Freq. step required for a count change of one

Fig. 8. Comparison between conventional VCO-based, prior BF-ADC [3] and this work.

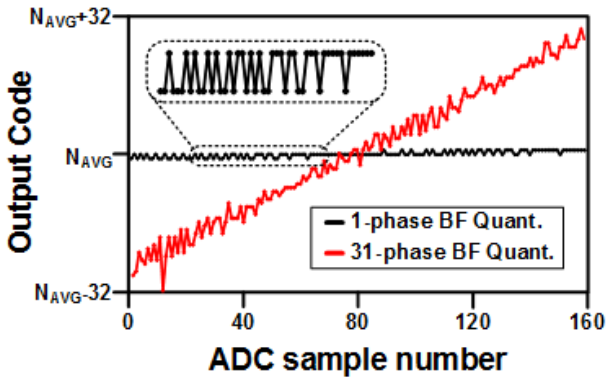

Fig. 10. Measured ADC output code for a ramp input. The sum of 31 BF counts clearly follows a ramp waveform (includes noise-shaping characteristics) ascending from -32 to +32, while the BF count from a single stage only increases from -1 to +1.

ADCs have shown that this new class of ADC has a lower probability of a metastable event compared to conventional voltage comparator-based quantizers [4]. Fig. 8 provides a comparison between various VCO-based ADCs including the proposed BF-ADC.

V. Circuit Implementation

Fig. 9 shows the implementation details of the proposed VCO-based ADC. Differential input signals V_{IN+} and V_{IN-} individually control the frequencies of the two 31-stage ring-oscillators. Each delay stage output is connected to a dedicated BF quantizer block. Each quantizer contains a positive and negative BF circuit for measuring frequencies ($f_{REF} - f_{IN+}$) and ($f_{REF} - f_{IN-}$), respectively. A separate 31-phase VCO is used to generate the reference clocks for the positive and negative BF quantizers. After the BF signal has been detected, sample/reset pulses are automatically generated by the self-timed short pulse generator block in Fig. 9. These pulses are then used to sample the current BF count and reset the counter for the next cycle. To ensure uninterrupted noise-shaping operation without missing a count, the pulse width is kept short enough to fit within a single input clock cycle. Finally, the digital output codes from all 31 BF quantizers are summed up and

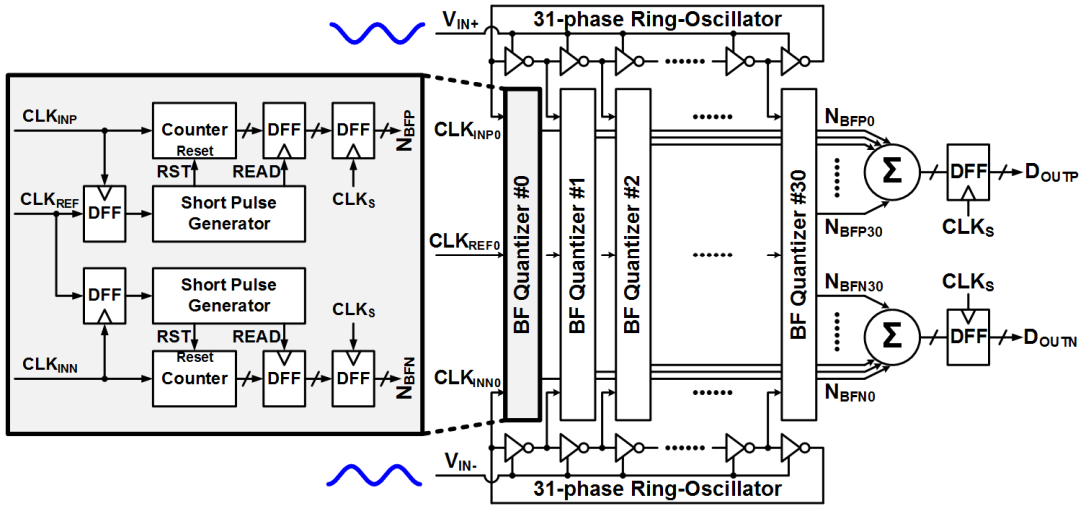

Fig. 9. Proposed multi-phase VCO-based ADC including a bank of noise-shaping BF quantizers.

sampled by the system clock (i.e. CLK_S) to produce the final ADC output. By summing up the BF quantizer outputs from each VCO stage, the number of conversion steps we can obtain increases by 31x resulting in a higher ADC resolution. Alternatively, we can read out the individual BF counts of each stage without summing them up, in which case we can achieve a higher sampling rate while maintaining the same resolution.

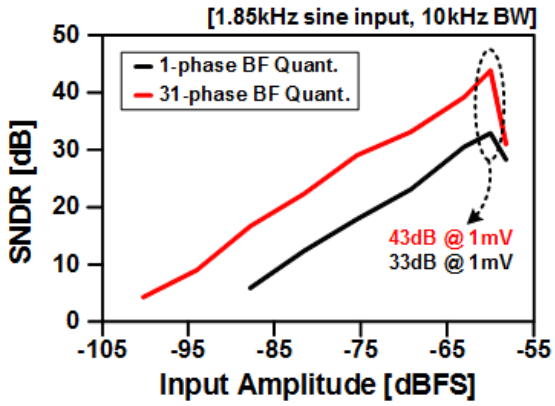

Fig. 11. Measured SNDR vs. ADC input amplitude for a 10kHz signal bandwidth. Here, the full-scale is assumed to be 1V, although the input range of interest is 1mV (i.e. -60dBFS).

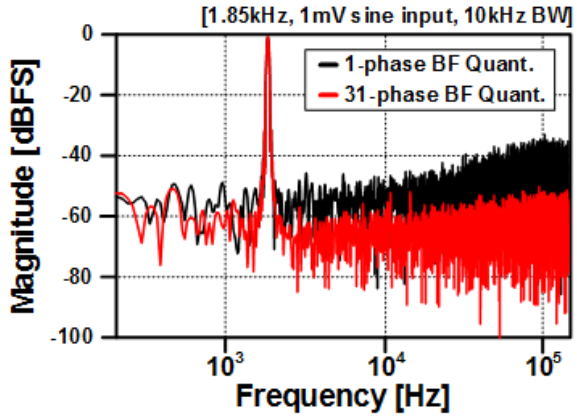

Fig. 12. Measured FFT for a 1.85kHz, 1mV sinusoidal input using bandwidth of 10kHz and a sampling rate of 300kS/s. SNDR is 43dB (i.e. ENOB = 6.85) and SFDR is 56.7dB for the 31-phase BF-ADC.

VI. Test Chip Measurements

A test chip was fabricated in a 65nm LP CMOS process to demonstrate the proposed BF-ADC circuit concepts. Fig. 10 shows the noise-shaping behavior of the proposed ADC when a small ramp input is provided. Note that the proposed multi-phase BF quantizer based ADC has a linear input-output relationship and a 31x wider output range compared to the single-phase implementation under the same test condition. Fig. 11 depicts the measured SNDR as a function of input amplitude for a 1.85kHz sinusoidal input sampled at 300kHz per BF count, assuming a bandwidth of 10kHz. The results show a 43dB SNDR at -60dBFS (i.e. 1mV) for the multi-phase design which is 10dB higher than its single-phase counterpart. Fig. 12 shows the measured ADC output spectrum for a 1.85kHz 1mV sinusoidal input signal using a 65536-point FFT. Fig. 13 compares the proposed ADC with previous VCO-based ADCs [3, 4, 5] in terms of various performance metrics. The die photo of the test chip is shown in Fig. 14 indicating an active area of 0.258mm^2.

	[4] VLSI'07	[5] VLSI'11	[3] CICC'13	This work
Process	0.13µm	90nm	65nm	65nm
Supply	1.2V	N/A	1.2V	1.2V
Sample Rate	950MHz	640MHz	4.17kHz	300kHz
Input BW	20MHz	8MHz	2kHz	10kHz
$SNDR_{1mV}$*	12dB	3dB	35dB	43dB
$ENOB_{1mV}$*	1.70	0.21	5.52	6.85
SFDR[dB]	N/A	71.4	41.9	56.7
IN_{0dB}[dBFS]**	-70	-63	-89	-105
Power	38mW	4.3mW	0.92µW	36µW
Area[mm^2]	0.185	0.10	0.013	0.258

* Peak SNDR/ENOB for a 1mV input amplitude.
** Input amplitude at SNDR = 0dB (dBFS @ full-scale = 1V)

Fig. 13. Performance comparison table.

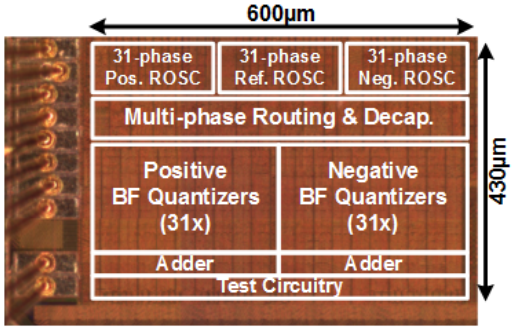

Fig. 14. 65nm test-chip die photo.

VII. CONCLUSION

In this paper, we present the operating principle, circuit design, and experimental data of a VCO-based ADC featuring a noise-shaping multi-phase BF quantization scheme. Measured data from a 65nm test chip shows a 43dB SNDR (or 6.85 ENOB) for a 1mV input signal when sampled at a frequency of 300kHz. The ADC consumes 36µW when operating under a 1.2V supply and occupies an active area of 0.258mm^2.

REFERENCES

[1] P. Harpe, Y. Zhang, G. Dolmans, K. Philips, H. D. Groot, "A 7-to-10b 0-to-40MS/s Flexible SAR ADC with 6.5-to-16fJ/conversion-step," in *Proc. Int. Solid-State Circuits Conf.*, pp. 472-473, February 2012.

[2] M. Yip, A. Chandrakasan, "A Resolution-Reconfigurable 5-to-10b 0.4-to-1V Power Scalable SAR ADC," *in Proc. Int. Solid-State Circuits Conf.*, pp. 190-191, February 2011.

[3] B. Kim, W. Xu, C. H. Kim, "A Fully-Digital Beat-Frequency Based ADC Achieving 39dB SNDR for a 1.6mVpp Input Signal," in *IEEE Custom Integrated Circuits Conf.(CICC)*, September 2013.

[4] M. Straayer, M. Perrot, "A 12-bit, 10-MHz Bandwidth, Continuous-Time ΣΔ ADC With a 5-bit, 950-MS/s VCO-based Quantizer," *in IEEE Journal of Solid-State Circuits (JSSC),* pp. 805-814, Apr. 2008.

[5] S. Lao, B. Young, A. Elshazly, W. Yin, N. Sasidhar, P. Hanumolu, "A 71dB SFDR Open Loop VCO-Based ADC Using 2-Level PWM Modulation," *in Proc. IEEE Symp. VLSI Circuits*, pp. 270-271, June 2011.