RTN Induced Frequency Shift Measurements Using a Ring Oscillator Based Circuit

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Abstract

The impact of random telegraph noise on ring oscillator (ROSC) frequency was measured for the first time using an on-chip beat frequency detection system. The proposed differential sensing scheme achieves a high frequency measurement resolution (>0.01%) at a short sampling time (>1μs) allowing efficient collection of RTN induced frequency shifts. Experimental data from a ROSC array fabricated in a 65nm LP process display both single trap and multi-trap RTN behavior. The voltage dependencies of the frequency shift and capture/emission times were measured and analyzed.

Introduction

Parametric shifts caused by temporal random trapping and de-trapping of carriers in the channel, also known as Random Telegraph Noise (RTN), have become a growing concern in extremely scaled CMOS. RTN coupled with Random Dopant Fluctuation (RDF) is predicted to have a detrimental effect on SRAM cell stability beyond 15nm. This situation has spurred a number of studies focusing on the characterization and mitigation of RTN effects in large-scale SRAM arrays [1,2]. As for logic circuits, only few attempts have been made to assess the true RTN impact. This, we believe, is primarily due to the difficulty of taking high precision measurements in a short measurement time from realistic circuits such as Ring OSCillators (ROSCs). Traditionally, characterization of RTN involved continuously monitoring the transistor drain current for a large population of devices using individual probing [3,4]. This method, however, is time-consuming, cumbersome, and provides little insight into the circuit level implications of RTN. Furthermore, due to the limited sensitivity of prior circuit based approaches, accelerated stress had to be applied in many experiments to amplify the RTN signal. This practice significantly undermines the confidence and applicability of the test results. In this work, we demonstrate for the first time, an on-chip beat frequency based monitor circuit capable of measuring RTN induced frequency shifts with a high precision (>0.01%) and short sampling time (>1μs). Additional benefits over traditional device probing include reduced test silicon area, shorter test times, and simpler and flexible test setups.

Beat Frequency Technique for RTN Monitoring

The basic concept of the beat frequency detection odometer technique for measuring the frequency difference between two ROSCs is illustrated in Fig. 1 [5]. The odometer samples the output of one oscillator using a D flip-flop at intervals set by the output of the other. The faster signal A catches up and then overtakes the slower signal B, and as this process repeats, the time between the overlapping points is the period of the beat frequency. This time is measured by counting the number of reference ROSC periods during a single beat period. This information is then read out through a scan based interface. The details on how to calculate the actual % frequency shift based on the scanned data can be found in the previous publication [5]. The beat frequency approach enables us to measure changes in transistor switching times as small as one part in 10,000 in less than a microsecond, making it ideally suited for characterizing RTN effects in logic paths.

The top level diagram of the 65nm test vehicle is shown in Fig. 2. It consists of a 10x8 ROSC array, a reference ROSC, and a beat frequency detection unit. Each ROSC has only 11 inverter stages to ensure high RTN sensitivity by minimizing the averaging effect. Prior to the testing, the initial frequency difference between the DUT and reference ROSCs is set to be around 1% (i.e. output count = 100) using on-chip trimming capacitors. This initial setting was found to provide a sufficiently high measurement resolution (= 0.01%) with minimal noise effects. One DUT ROSC is selected at a time for the frequency measurements using column and row select signals. Output signal of the selected DUT ROSC drives the bitline signal which is multiplexed out and fed to the D flip-flop inside the beat frequency detection unit.

For a better understanding, Fig. 3 compares three ROSC based RTN measurement structures including the proposed technique. A ROSC with a frequency divider can be considered, however, this single-ended configuration suffers from large measurement noise in the presence of voltage fluctuations and temperature drifts. To the best of our knowledge, there haven't been any reports showing RTN data based on this simple approach. Another method for measuring RTN is illustrated in Fig. 3 where a frequency divider in a metastable state is used [6]. The divider's output frequency switches between f/2 and f/3 according to the RTN capture and emission times. Here, f is the input frequency. The main drawback of this approach is that it is hard to infer physical parameters such as frequency or V_t based on the erratic divider output. The beat frequency scheme, on the other hand, can measure the exact frequency shift due to single or multiple RTN traps with high precision and short measurement time, making it an effective characterization method for RTN effects in logic circuits.

RTN Induced Frequency Shift Measurements

The frequency shift waveforms in Fig. 4 are from three different ROSCs in the test array. RTN's signature trapping/de-trapping behavior can be clearly observed. Independent of the time constant values, the frequency shift caused by a single RTN trap was approximately 0.4% for the 11 stage ROSC operating at 0.8V and 25°C. Our repeated experiments revealed no RTN in the reference ROSC, although this is purely a statistical occurrence. Due to the identical layout and physical proximity, there is no reason to believe that the chances of having an RTN trap in the reference and DUT ROSCs will different. The emission and capture time constants (i.e. τ_e and τ_c) ranges from 2.50ms to 405ms depending on the supply voltage and ROSC instance. Fig. 5 (upper) shows frequency traces of two ROSCs having a single trap and two traps, respectively. The capturing and emission transitions can be better visualized using the time lag plot [3] shown in Fig. 5 (lower).

RTN parameters are shown to have a strong voltage dependence which was experimentally verified from the test chip (Fig. 6). As the supply voltage is increased from 0.8V to 1.1V, the RTN induced frequency shift decreases from 0.48% to 0.14%. Eventually, RTN becomes indistinctive at 1.2V, the nominal operating voltage of this process. These results are in line with previous studies that have reported a stronger RTN signal at lower supply voltages [3]. Fig. 7 shows the distribution of the capture and emission times at 0.8V and 1.0V. The exponential model agrees well with the measured data. The time constants τ_c and τ_e extracted from the distributions display opposite dependencies on supply voltage as shown in Fig. 8. The Power Spectrum Density (PSD) of a DUT ROSC with a single trap is shown in Fig. 9. The spectrum follows a Lorenzian with the typical $1/f^2$ frequency dependence. Histogram of the numbers of RTN traps per ROSC is shown in Fig. 9. 66% of the ROSCs did not show any signs of RTN while no ROSC had more than 2 traps. The relatively low number of traps in each ROSC can be attributed to the mature process technology used for the test chip fabrication. The transistor V_t shift caused by a single RTN trap was estimated to be 1.2% (Fig. 11). For this, we simulated an 11 stage ROSC and translated the measured frequency data back to the device V_t using the mapping curve in Fig. 12. Finally, the die photograph of the 65nm RTN test chip is shown in Fig. 13.

Reference: [1] S.Toh, IEDM, 2009. [2] K. Takeuchi, VLSI Tech. Symp., 2011 [3] T. Nagumo, IEDM, 2009. [4] S. Realov, IEDM, 2010. [5] J. Keane, IEDM, 2010. [6] K. Ito, IRPS, 2011.

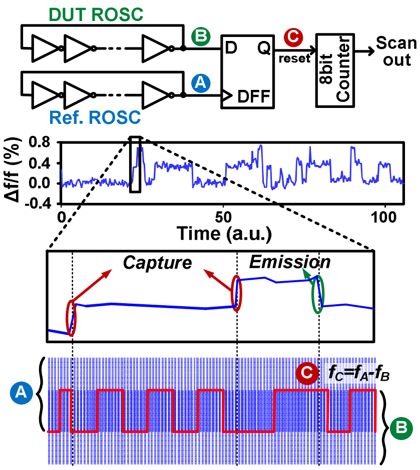


Fig. 1. Beat frequency technique proposed for RTN measurements. A high frequency shift resolution (>0.01%) and a short (>1μs) measurement time can be achieved.

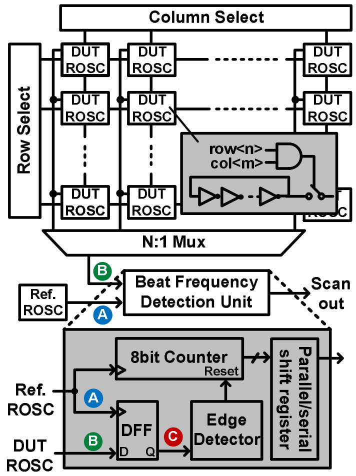
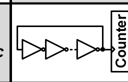
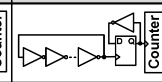
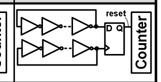


Fig. 2. ROSC array test chip for RTN measurements comprising an on-chip beat frequency detection circuit.

	Single ROSC	*DFF Sensor [5]*	*This Work*
Circuit Schematic			
Description	Simple ROSC with frequency divider	D flip-flop driven by a simple ROSC to metastable state	Differential ROSC structure, beat frequency detection
Freq. Meas. Resolution	Low resolution, sensitive to V, T drifts	Pass/fail information only	High resolution, immune to V, T drifts
*Sampling Time**	~ 100μs	N/A	> 1μs**
Capable of Measuring	N/A (no reported RTN data using this method)	Single trap only	Multiple traps
Source(s) of RTN		ROSC and DFF	ROSCs
Output	Actual ROSC freq. shift	Input frequency divided by 2 or 3	Actual ROSC freq. shift

** For a 0.01% frequency shift resolution and a ROSC period of 10ns*
*** Emission and capture times down to several microseconds can be measured*

Fig. 3. Comparison of three ROSC based RTN measurement techniques.

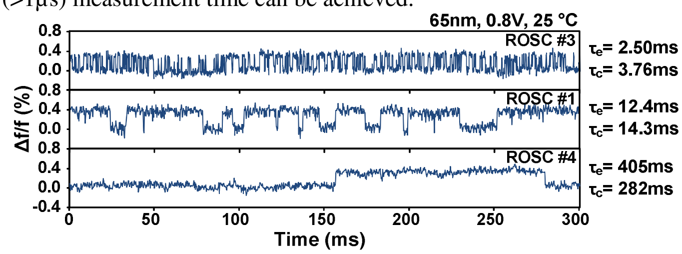


Fig. 4. Single trap RTN waveforms measured from different ROSCs.

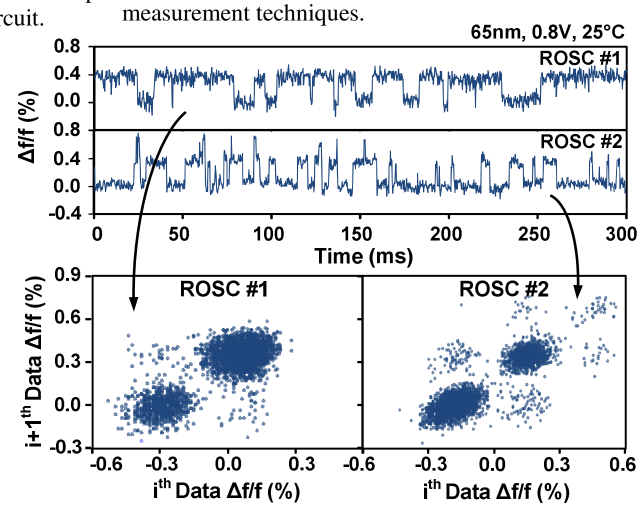


Fig. 5. (Upper) Single and multi trap RTN waveform from two different ROSCs. (Lower) Time Lag Plot (TLP) of the two traces.

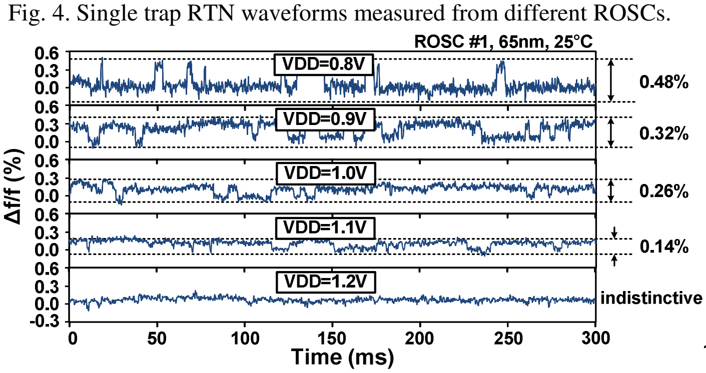


Fig. 6. RTN traces from same ROSC at different supply voltages.

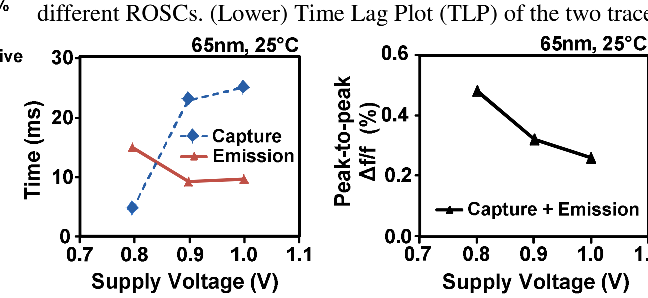


Fig. 8. Time constant and frequency shift versus supply voltage.

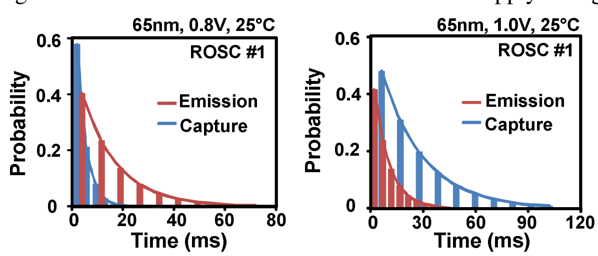


Fig. 7. Capture and emission time distributions and exponential fit results for VDD=0.8V (left) and VDD=1.0V (right).

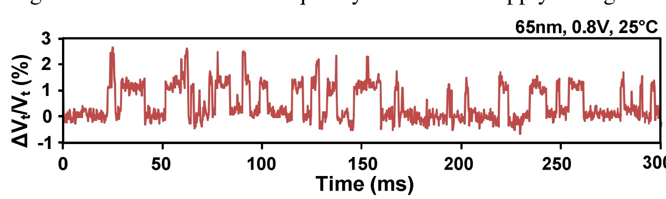


Fig. 11. Single device V_t shift estimated from ROSC frequency data.

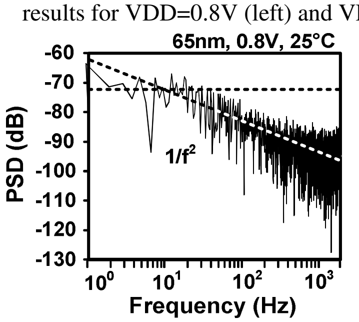


Fig. 9. Power Spectrum Density (PSD) of the frequency shift data.

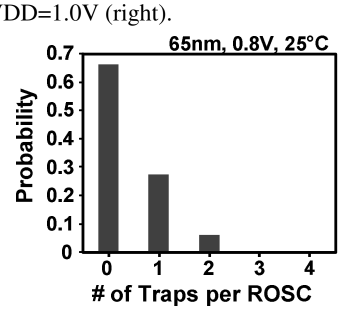


Fig. 10. Histogram of the number of traps per ROSC.

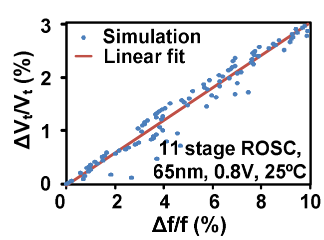


Fig.12. Frequency to V_t mapping.

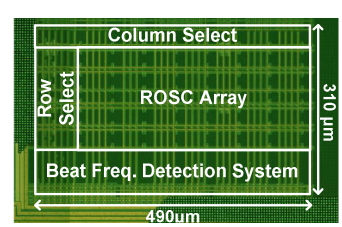


Fig.13. Test chip die photo.