A 32nm, 0.9V Supply-Noise Sensitivity Tracking PLL for Improved Clock Data Compensation Featuring a Deep Trench Capacitor Based Loop Filter

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Abstract

An adaptive PLL implemented in a 0.9V 32nm process achieves optimal clock data compensation across a wide range of PVT and operating conditions. This is accomplished by an automated supply-noise sensitivity tracking loop which constantly monitors the BER of a tunable critical path circuit. The proposed PLL achieves a 14.5% to 15.6% improvement in processor Fmax over a conventional design for a 90mV supply noise and has a 92.1% smaller area by employing ultra-high density deep trench capacitors in the loop filter.

Introduction

Power supply noise caused by the resonance between the package inductance and on-die capacitance has become a major design consideration in modern high performance systems. Recently, researchers have revealed an intrinsic timing compensation phenomenon between the clock and the data signals which could partially mitigate the impact of resonant supply noise on processor speed [1-3]. One promising approach to enhance the beneficial Clock Data Compensation (CDC) effect is to systematically couple the supply noise into the PLL output clock using programmable resistor [2] or capacitor banks [3]. Previous adaptive PLLs rely on exhaustive search for finding optimal CDC parameters which involves a cumbersome and time-consuming calibration process. Moreover, once programmed, these parameters cannot be changed making the design susceptible to operating condition changes and other PVT effects. In addition, the extra passive devices and analog circuitry in the CDC modulator (see Fig. 4) increases the PLL area and worsens the loop stability. In this paper, we propose an Automatic Supply-noise Sensitivity Tracking (ASST) PLL that addresses all the above-mentioned issues. The proposed PLL aligns the local clock edge with the datapath signal using an on-the-fly supply sensitivity tracking loop based on a tunable critical path Bit Error Rate (BER) monitor circuit. The PLL utilizes, for the first time, an ultra-dense deep trench capacitor to reduce the circuit area.

Automatic Supply-Noise Sensitivity Tracking Loop

Fig. 1 illustrates the concept of an adaptive PLL [2-3] for enhancing the beneficial CDC effect. By modulating the PLL output clock period using the resonant supply noise while carefully accounting for the clock period modulation in the clockpath, timing failures in the datapath can be avoided. This leads to either a lower power consumption under iso-operating frequency or a higher operating frequency under iso-power consumption. An exhaustive search method was used in a prior adaptive PLL for determining key CDC parameters such as phase shift and sensitivity [3]. However, a timing model based analysis reveals that adjusting the supply sensitivity parameter is sufficient for achieving the desired CDC compensation effect. The clockpath and datapath timing models used in the analysis are shown in Fig. 2. The PLL output clock (CLKi) enters the clockpath which has a time-varying delay of D(t) under resonant supply noise. As the clock edge traverses through the clock path, its period gets modulated by the supply noise. For example, the maximum (or minimum) CLKi period occurs when the supply has the steepest negative (or positive) slope, i.e. when the time-derivative of delay D(t) is maximum (or minimum). The local clock (CLKo) period is the sum of the delayed CLKi's period and the integration of the time-derivative of D(t) from time t-D(t) to t. The timing models confirm that in the presence of resonant noise, the CLKo period is aligned with the datapath delay by setting the supply sensitivity of CLKi to be equal to that of the clockpath delay (=D(t)).

A key benefit of a single parameter control over a multi-parameter one [3] is that it is simpler to build a closed-loop system for tracking the optimal CDC configuration. Measured results in Fig. 3 (right) show a 7.8% higher processor Fmax for the proposed ASST PLL compared to its fixed sensitivity counterpart.

ASST PLL Circuit Implementation

A test chip was fabricated in a 0.9V, 32nm SOI process to verify the ASST PLL operation (Fig. 4). To AC-couple the resonant noise to the PLL control voltage with constant sensitivity steps, a CDC modulator consisting of two capacitor banks (C_u, C_d) with each having 63 unit capacitors was implemented. Prior to the tracking operation, a target critical path delay was set using tunable delay stages. The tracking operation starts by enabling the tracking loop in Fig. 4 after the PLL is locked. A BER monitor generates bit errors whenever a timing violation occurs in the critical path circuit. We have the flexibility to choose between a single error event (=fast but potentially unstable tracking response) or until a certain number of errors has been reached (=slow but smooth tracking response) for updating the supply noise sensitivity. An up/down counter with a binary-to-thermometer code decoder is used to convert bit errors into a sensitivity code. Once the tracking loop is locked, the digital filter determines the up/down counting direction according to the current BER information. Response time of the entire tracking loop from the noise coupling to the sensitivity update is negligible compared to a typical resonant noise period (e.g. 10ns).

Deep Trench Capacitor Based Loop Filter

The proposed ASST PLL effectively utilizes deep trench capacitor technology, originally developed for embedded DRAM cells [5]. The capacitance density is approximately two orders of magnitude higher compared to that of a thick oxide MOS capacitor (i.e. a popular option for traditional PLL designs) while the tunneling leakage is negligible due to the thick dielectric. Note that only the area-dominating integrating capacitor (C_i in Fig. 5) was implemented using a deep trench capacitor because the relatively high series resistance of trench capacitors limits their ripple rejection capability when used as a third-pole capacitor (C_p in Fig. 5). This was confirmed through AC and transient simulations in Fig. 6. Measured results show no noticeable difference in PLL performance between a deep trench C_i and a thick oxide C_i based loop filter while the former provides a significant reduction in PLL area as shown in Fig. 10.

Test Chip Results

Several ASST waveforms along with the measured PLL control voltage are shown in Fig. 8 for a typical tracking operation. The ASST PLL starts an initial BER tracking with a monotonically increasing counter output while bit errors are being generated on-the-fly. After the initial locking, the tracking loop responds to any changes in the clockpath sensitivity due to voltage/temperature shifts by modifying the sensitivity code (i.e. EN[62:0] in Fig. 4). To compare the performance between conventional and ASST PLLs, Fmax was extracted from the measured BER vs. frequency data [3]. PLL phase noise along with the actual datapath delay fluctuation under supply noise is accounted for in the BER measurements. As shown in Fig. 9, the proposed ASST PLL achieves 14.5% to 15.6% higher processor Fmax compared to a conventional PLL with a constant output clock period under a 90 mV supply noise amplitude. PLL performance at different noise amplitudes, noise frequencies and clockpath designs has been measured to verify the effectiveness under a wide range of usage scenarios. Finally, the chip micrograph and summary table are shown in Fig. 10.

References

[1] K. Wong, JSSC, pp.749-758, Apr. 2006. [2] N. Kurd, JSSC, pp.1121-1129, Apr. 2009. [3] D. Jiao, ISSCC, pp.272-274, 2011. [4] J. Xu, ISSCC, pp. 286-287, Feb. 2007. [5] N. Butt, IEDM, pp. 27.5.1-4, 2010. [6] J. Craninckx, JSSC, pp. 2054-2065, Dec. 1998.

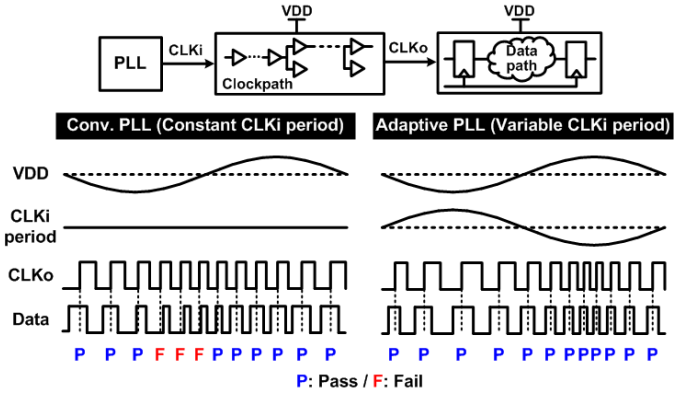


Fig. 1. Adaptive PLL for enhancing Clock Data Compensation (CDC).

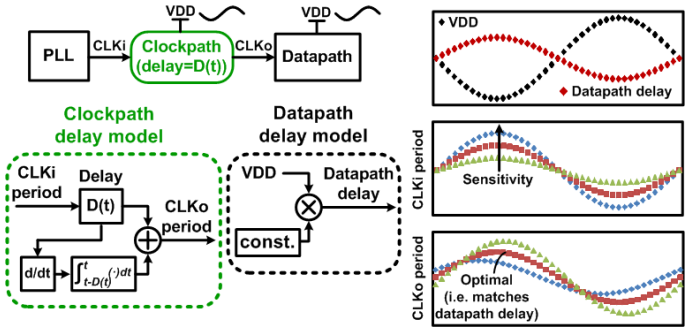
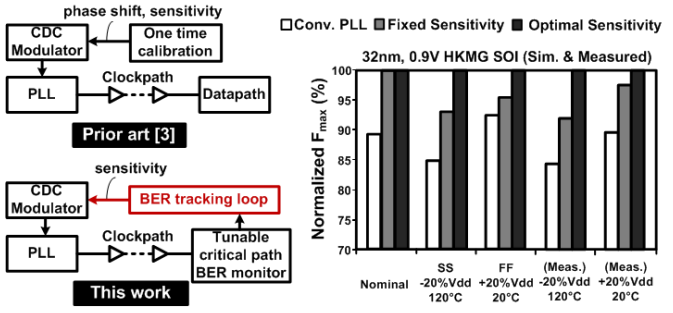


Fig. 2. Optimal CDC can be achieved by tuning the PLL's supply noise sensitivity as demonstrated using timing models.



	# of control parameters	Parameter setting	Passive area
Conv.	None	None	Large
[2]	One (sensitivity)	1D sweep, one time	Large
[3]	Two (phase, sensitivity)	2D sweep, one time	Large
This work	*One (sensitivity)	Closed-loop tracking	Small (C_{trench})

*Key requirement for stable closed-loop tracking

Fig. 3. Concept of BER based PLL sensitivity tracking loop (left). The proposed scheme (black bars) can achieve up to a 7.8% higher processor Fmax compared to a previous one-time calibration scheme (gray bars) under extreme PVT conditions (right). Comparison with prior art (bottom table).

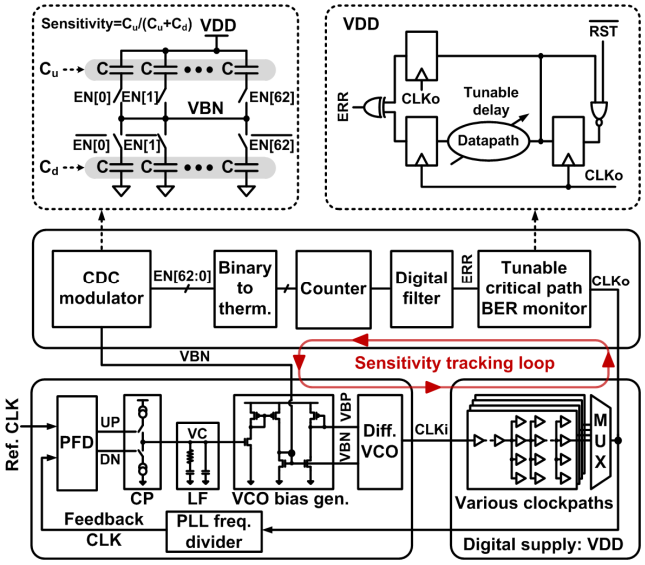
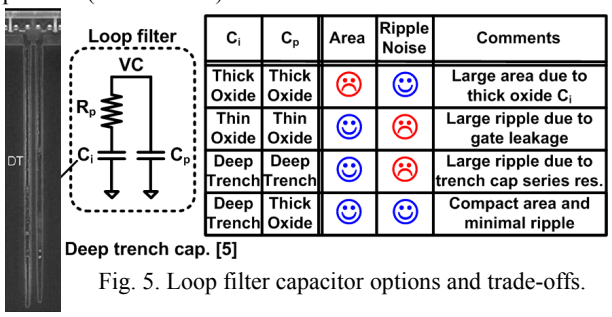


Fig. 4. Overall diagram of ASST PLL test chip.



C_i	C_p	Area	Ripple Noise	Comments
Thick Oxide	Thick Oxide	☹	☺	Large area due to thick oxide C_i
Thin Oxide	Thin Oxide	☺	☹	Large ripple due to gate leakage
Deep Trench	Deep Trench	☺	☹	Large ripple due to trench cap series res.
Deep Trench	Thick Oxide	☺	☺	Compact area and minimal ripple

Fig. 5. Loop filter capacitor options and trade-offs.

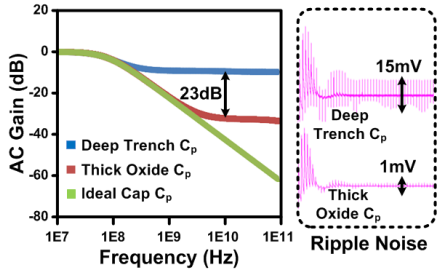


Fig. 6. Simulated PLL third-pole AC response and transient ripple noise with different C_p.

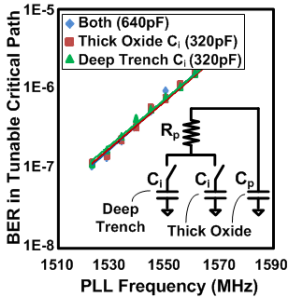


Fig. 7. Measured PLL performance for deep trench C_i and thick oxide C_i

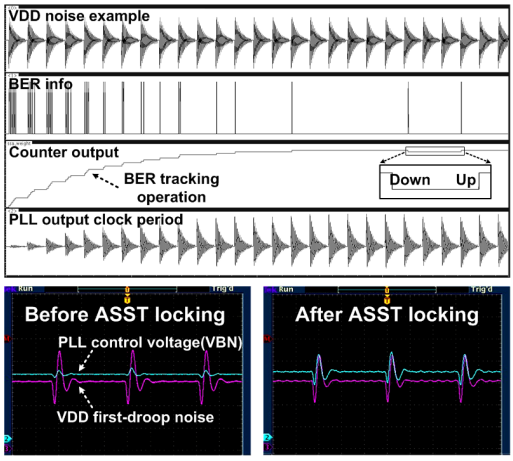


Fig. 8. Simulated waveforms (above) and measured VDD and PLL control voltage VBN (below) of the proposed ASST PLL.

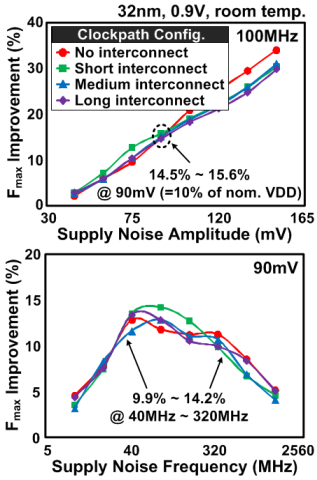
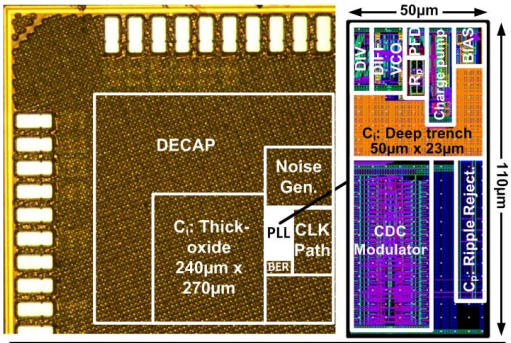


Fig. 9. Measured F_{max} vs. noise amplitude and frequency.



Process	32nm HKMG SOI	Deep trench PLL area	0.0055mm²
Supply voltage	0.9V	Conv. PLL area	0.0692mm²
F_{max} improvement (w/ 90mV noise)	14.5%~15.6%	PLL area reduction	*-92.1% **-43.6%

Compared to *single-path PLL and **dual-path PLL with 12:1 ratio [6]

Fig. 10. Die photo and feature summary table.