Subnanowatt Carbon Nanotube Complementary Logic Enabled by Threshold Voltage Control

Michael L. Geier,† Pradyumna L. Prabhumirashi,† Julian J. McMorrow,† Weichao Xu,§ Jung-Woo T. Seo,† Ken Everaerts,‡ Chris H. Kim,§ Tobin J. Marks,†,§ and Mark C. Hersam*†,§

†Department of Materials Science and Engineering and ‡Department of Chemistry, Northwestern University, Evanston, Illinois 60208, United States
§Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, Minnesota 55455, United States

ABSTRACT: In this Letter, we demonstrate thin-film single-walled carbon nanotube (SWCNT) complementary metal-oxide-semiconductor (CMOS) logic devices with subnanowatt static power consumption and full rail-to-rail voltage transfer characteristics as is required for logic gate cascading. These results are enabled by a local metal gate structure that achieves enhancement-mode p-type and n-type SWCNT thin-film transistors (TFTs) with widely separated and symmetric threshold voltages. These complementary SWCNT TFTs are integrated to demonstrate CMOS inverter, NAND, and NOR logic gates at supply voltages as low as 0.8 V with ideal rail-to-rail operation, subnanowatt static power consumption, high gain, and excellent noise immunity. This work provides a direct pathway for solution processable, large area, power efficient SWCNT advanced logic circuits and systems.

KEYWORDS: SWCNT, transistor, CMOS, inverter, NAND, NOR

Single-walled carbon nanotubes (SWCNTs) possess exceptional electronic characteristics and have been explored for applications in solution processable, flexible, high-performance electronics.1-3 In particular, advances in semiconducting SWCNT sorting4-10 and integration techniques11-13 have enabled the fabrication of random network unipolar14-20 and ambipolar21-23 logic devices ranging from transistors to 4-bit row decoders.24 However, as SWCNT electronics move from individual device demonstrations to highly integrated circuits, unipolar/ambipolar transistors present significant issues, most notably high power consumption. Although there have been demonstrations25-27 of random network SWCNT-based complementary metal-oxide-semiconductor (CMOS) circuits, this early work did not realize the principal advantage of CMOS logic, namely low power consumption, due to suboptimal threshold voltage control. Here, we demonstrate SWCNT-based CMOS logic circuits with subnanowatt static power consumption via threshold voltage tuning of the constituent p-type and n-type SWCNT transistors. The resulting ultralow power SWCNT CMOS logic circuits possess symmetric voltage transfer curves, high gain, and wide noise margins that are suitable for logic gate cascading and large-scale integration.

The development of solution-processed semiconducting SWCNTs has allowed large-area deposition of random network SWCNT films, leading to extensive studies of SWCNT thin-film transistors (TFTs) in a variety of device structures.15,16,21 Because of adventitious atmospheric doping of SWCNT TFTs under ambient conditions, p-type unipolar devices have dominated prior efforts that have primarily focused on optimizing the trade-off between mobility and current on/off ratio (I_{ON}/I_{OFF}).13,14,17 However, when implemented in logic circuits, unipolar devices sustain high steady-state currents, which lead to significant steady-state power consumption during operation. In contrast, CMOS logic is the backbone of modern microelectronics since either the constituent p-type or n-type transistor is turned off in each logic gate, resulting in intrinsically low power consumption and thus the ability to be implemented in efficient large-scale integrated circuits.28 Moreover, CMOS logic offers wide noise margins, which allows robust and reliable operation in highly complex circuitry that inevitably encounters large parametric shifts. These enabling advantages of CMOS technology not only require the realization and integration of p-type and n-type transistors but also precisely tuned, well-separated threshold voltages to ensure that the complementary devices are not concurrently passing current and thus not dissipating steady-state power. This critical issue has not been addressed in previous SWCNT TFT studies,14-23 and thus stands as the key challenge limiting the realization of highly integrated SWCNT-based CMOS electronics.

In this Letter, we demonstrate threshold voltage control for both p-type and n-type SWCNT TFTs via a local Ni gate structure, which enables ultralow power complementary device operation. A high-performance SWCNT CMOS inverter (NOT gate) is provided as an initial illustration of this device
A schematic of the inverter structure is shown in Figure 1a and consists of an unencapsulated SWCNT p-type TFT and a SWCNT n-type TFT that is chemically doped with benzyl viologen (Supporting Information Figure S1). The p-type and n-type TFTs share a common input voltage ($V_{IN}$) at their gates and a common output voltage ($V_{OUT}$) at their drains. In addition, the p-type TFT source is connected to the power supply ($V_{DD}$), and the n-type TFT source is connected to ground (GND). Figure 1b is a schematic cross-section that shows further details of the SWCNT TFT structure. Additionally, the atomic force microscope (AFM) image shown in Figure 1c illustrates the uniformity of the SWCNT network in the TFT channel region.

![Figure 1. SWCNT CMOS device structure. (a) Schematic of the SWCNT CMOS inverter including the unencapsulated p-type TFT and benzyl viologen doped n-type TFT. (b) Schematic cross-section of an individual SWCNT TFT consisting of a 300 nm SiO$_2$ on Si substrate, a local Ni (25 nm thick) gate patterned by photolithography, a conformal 10 nm Al$_2$O$_3$ layer deposited via atomic layer deposition (ALD), >99% semiconducting purity SWCNTs deposited by vacuum filtration film transfer, and Cr/Au (2 nm/50 nm) source/drain contacts. (c) Atomic force microscopy image of the SWCNT film morphology in the TFT channel region.](image1)

![Figure 2. SWCNT TFT electrical characteristics. (a) Log–linear transfer characteristics ($I_{DS}$ vs $V_{GS}$) of a p-type TFT (blue) at $V_{DS} = -1$ V and n-type TFT (green) at $V_{DS} = 1$ V. (b) Output characteristics ($I_{DS}$ vs $V_{DS}$) of a p-type TFT (left axis) from $V_{GS} = -1$ to 0 V in 0.25 V steps and n-type TFT (right axis) from $V_{GS} = 1$ to 0 V in 0.25 V steps. (c) Linear-linear transfer characteristics for PMOS (blue) at $V_{DS} = -1$ V and for NMOS (green) at $V_{DS} = 1$ V with the linear region fit shown for $V_T$ extraction. (d) Statistical distribution of $V_T$ for 30 p-type TFTs (blue) and 30 n-type TFTs (green).](image2)
the TFT channel region with a linear tube density of ∼18 nanotubes/μm (~99% semiconducting purity SWCNTs; see Supporting Information Figure S2 for more information).

Figure 2a shows the log–linear transfer characteristics of the constituent p-type and n-type TFTs with channel lengths of 20 μm and widths of 100 μm. The individual transistors have $I_{ON}/I_{OFF}$ of ∼10$^6$ and subthreshold slopes of ∼125 mV/decade (p-type) and ∼175 mV/decade (n-type) over the CMOS operating voltage range of each device, namely $V_{GS}$ of the p-type TFT is between $-V_{DD}$ and GND, and $V_{GS}$ of the n-type TFT is between GND and $V_{DD}$. The gate dielectric (10 nm Al$_2$O$_3$) has a leakage current of less than 100 pA (Supporting Information Figure S3) in the operational voltage window (∼1 to 1 V) and a capacitance of ∼850 nF/cm$^2$ (Supporting Information Figure S4). Figure 2b shows well-balanced output characteristics for the p-type TFT ($V_{GS}$ varied from 0 V to ∼1 V in 0.25 V steps) and n-type TFT ($V_{GS}$ varied from 0 to 1 V in 0.25 V steps). $V_T$ for both the p-type and n-type TFTs is determined by extrapolation from the linear transfer characteristics as shown in Figure 2c. The use of the local metallic (Ni) gate structure is critical to obtaining a negative $V_T$ for p-type SWCNT TFTs as demonstrated previously. Upon conversion of the p-type TFTs to n-type TFTs via benzyl viologen doping, the $V_T$ for the n-type TFT becomes analogously positive, thus achieving the symmetric $V_T$ separation required for ultralow power CMOS. In particular, Figure 2d shows a histogram of extracted $V_T$ for the p-type and n-type TFTs, demonstrating clearly separated and symmetric $V_T$ with negative $V_T$ for the p-type TFTs and positive $V_T$ for the n-type TFTs.

The CMOS inverter performance is investigated using the device geometry shown in Figure 1a. The inset of Figure 3a displays the circuit diagram for the CMOS inverter, which is composed of one p-type TFT and one n-type TFT connected in series. Figure 3a shows the inverter voltage transfer characteristics for different supply voltages ($V_{DD}$ = 0.8, 1.0, and 1.25 V). At low input voltage ($V_{IN} = GND$), equivalent to logic “0”, $V_{OUT}$ is pulled up to $V_{DD}$ equivalent to logic “1”. Similarly at high input voltage ($V_{IN} = V_{DD}$), equivalent to logic “1”, $V_{OUT}$ is pulled down to GND, equivalent to logic “0”. Thus, the SWCNT CMOS inverter demonstrates a full rail-to-rail ($V_{DD}$ to GND) transfer curve in a symmetric operating voltage window. The noise margins (NM) for this device are NM$_{LOW} = 0.32$ $V_{DD}$ and NM$_{HIGH} = 0.54$ $V_{DD}$ for all $V_{DD}$, thereby providing excellent tolerance against incoming signal variation and suitability for inverter cascading as well as further device integration.

Figure 3b shows the power consumption ($P = V_{DD} \times I_{GND}$) of the CMOS inverter during transfer at different supply voltages. The power consumption is less than 0.1 nW in the static states of $V_{IN} = V_{DD}$ and $V_{IN} = GND$. The peak power consumption is less than 10 nW (for all $V_{DD}$) and occurs approximately at the midpoint of the transfer state ($V_{IN} = V_{OUT}$) when the p-type and n-type TFTs are simultaneously in the ON-state. The ultralow power consumption demonstrated by these devices, representing the lowest reported value by 3 orders of magnitude for random network SWCNT-based CMOS logic, is enabled by the symmetric and well-separated threshold voltages for the p-type and n-type TFTs.

Figure 3c shows the gain (d$V_{OUT}$/d$V_{IN}$) of the inverter, including a peak gain in excess of 25 at $V_{DD} = 1.25$ V. The peak gain shows a linearly increasing relationship (Figure 3d) with respect to $V_{DD}$ and is likely due to $V_{DD}$ being comparable to the threshold voltages of the TFTs, allowing increasing transconductance with increasing $V_{DD}$.

To demonstrate the next level of CMOS integration, NAND and NOR logic gates were fabricated. A NAND logic gate is
realized by connecting two n-type TFTs in series and two p-type TFTs in parallel, while NOR logic gates employ two n-type TFTs in parallel and two p-type TFTs in series (Figure 4a,b shows the circuit diagrams and associated truth tables for NAND and NOR gates, respectively). Figure 4c,d shows $V_{OUT}$ for the four possible input states of A and B for NAND and NOR gates, respectively. In all cases, $V_{IN}$ (A and B) is set at $V_{DD}$ for the logic state “1”, and $V_{IN}$ is set at 0 V (GND) for the logic state of “0”. For the CMOS NAND logic gate, $V_{OUT}$ becomes logic “0” only when both A and B are in the logic “1” state. Conversely, for the CMOS NOR logic gate, $V_{OUT}$ is the logic “1” level only when both A and B are in the logic “0” state. These tests confirm that in both SWCNT CMOS NAND and NOR devices, the logic gates demonstrate ideal rail-to-rail output voltages for the appropriate two input state. In all static states, the power consumption is on the order of 0.1 nW as shown in Figure 4e for the NAND gate and Figure 4f for the NOR gate. In addition, during the transition between the output states of logic “1” ($V_{OUT} = V_{DD}$) and “0” ($V_{OUT} = GND$), the NAND and NOR gates show a peak power of $\sim$10 nW as expected from the earlier inverter discussion (see Supporting Information Figures S5 and S6 for further details on NAND and NOR operation, respectively). The gain behavior of NAND and NOR gates (see Supporting Information Figure S5 for NAND and Supporting Information Figure S6 for NOR) is also similar to the inverter, showing a linear increase in peak gain with respect to applied voltage, $V_{DD}$. Overall, these CMOS NAND and NOR logic gates are suitable for further integration into complex circuits due to their ideal input and output voltage behavior while concurrently possessing subnanowatt static power consumption.

In conclusion, we have demonstrated SWCNT-based CMOS inverter, NOR, and NAND gates, which constitute the fundamental building blocks of large-scale integrated digital logic circuits with subnanowatt static power consumption, thereby realizing the primary benefit of the CMOS architecture. This enabling advance was accomplished through precise tuning of the p-type and n-type TFT threshold voltages to match the ideal conditions for an integrated CMOS device. The resulting logic gates exhibit symmetric rail-to-rail operation and excellent noise immunity, which will allow for cascaded multiple logic gates in highly integrated circuits. These results coupled with the many other unique attributes of SWCNTs (e.g., solution processability, mechanical flexibility, chemical and thermal stability, and high mobility) provide a direct pathway to large area, ultralow power nanoelectronic systems.

**ASSOCIATED CONTENT**

Supporting Information
Preparation of benzyl viologen solution; dispersion, separation and characterization of SWCNTs; device fabrication procedure; electrical testing setup; dielectric characterization; NAND and NOR logic gate characterization; environmental stability of inverters; hysteresis and key device metrics of the n-type SWCNT TFTs. This material is available free of charge via the Internet at http://pubs.acs.org.

**AUTHOR INFORMATION**

Corresponding Author
*E-mail: m-hersam@northwestern.edu.
Author Contributions
The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes
The authors declare no competing financial interest.

ACKNOWLEDGMENTS
This work was supported by the Office of Naval Research MURI Program (N00014-11-1-0690) and the National Science Foundation (DMR-1006391 and DMR-1121262). A National Science Foundation Graduate Research Fellowship (M.L.G.) and a NASA Space Technology Research Fellowship (J.J.M.) are also acknowledged. The device fabrication was performed at the NUFAF clean room facility at Northwestern University. The AFM and SEM characterization was performed in the NUANCE facility at Northwestern University, which is supported by the NSF-NSEC, NSF-MRSEC, Keck Foundation, and State of Illinois.

REFERENCES