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Aerosol Jet Printed, Low Voltage, Electrolyte Gated Carbon Nanotube Ring Oscillators with Sub-5 μs Stage Delays

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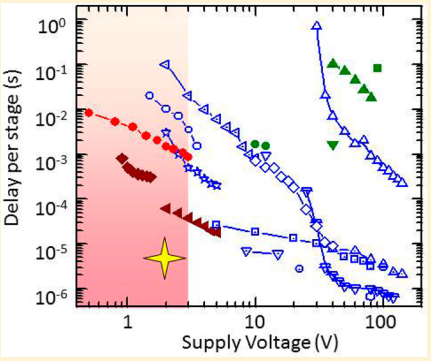
S *Supporting Information*

ABSTRACT: A central challenge for printed electronics is to achieve high operating frequencies (short transistor switching times) at low supply biases compatible with thin film batteries. In this report, we demonstrate partially printed five-stage ring oscillators with >20 kHz operating frequencies and stage delays <5 μs at supply voltages below 3 V. The fastest ring oscillator achieved 1.2 μs delay time at 2 V supply. The inverter stages in these ring oscillators were based on ambipolar thin film transistors (TFTs) employing semiconducting, single-walled carbon nanotube (CNT) networks and a high capacitance (~1 μF/cm^2) ion gel electrolyte as the gate dielectric. All materials except the source and drain electrodes were aerosol jet printed. The TFTs exhibited high electron and hole mobilities (~20 cm^2/(V s)) and ON/OFF current ratios (up to 10^5). Inverter switching times t were systematically characterized as a function of transistor channel length and ionic conductivity of the gel dielectric, demonstrating that both the semiconductor and the ion gel play a role in switching speed. Quantitative scaling analysis suggests that with suitable optimization low voltage, printed ion gel gated CNT inverters could operate at frequencies on the order of 1 MHz.



KEYWORDS: *Printed electronics, carbon nanotubes, ion gel, ring oscillator, delay time, ion conductivity*

Ongoing efforts to develop printed electronics are motivated by a broad spectrum of potential applications including radiation detection, health diagnostics, drug delivery, distributed sensing, information display, food security, and inventory tracking.[1−5] The best opportunities for flexible printed circuits will likely be in applications where large footprints *are required* in addition to mechanical flexibility since conventional semiconductor circuitry is difficult to scale effectively to large areas.

Of the many technical challenges facing printed electronics, one of the most fundamental is the trade-off between supply voltage and operating speed. For any circuit, printed or conventional, operating frequency increases as supply biases are increased. However, many foreseeable printed circuit applications will be powered by relatively low voltage thin film batteries where the maximum supply voltage is typically 3 V or smaller. Organic circuits are good candidates for these applications, yet a survey of the literature reveals that for nonprinted (evaporated, spin-coated, etc.) organic circuits delay times less than 10 μs have been obtained only with 10 V or greater supply biases,[6−14] and the delay times for circuits operating at battery voltages are above 30 μs.[15−19] Printed organic circuits are generally much slower (with milliseconds delay time) and require high supply voltages (tens of volts).[2,20−23] The relatively low switching speeds at low biases are a result of several factors including the comparatively low carrier mobilities of many printed semiconductors and large source-to-drain channel lengths due to limits on printing resolution. Some groups are investigating transfer printing[24−29] or jet printing[2,30−35] of high-mobility semiconductors, e.g., silicon, oxides, nanowires, graphene, and carbon nanotubes (CNTs), and these efforts have the potential to produce low-voltage circuits operating at high speed. However, an additional barrier to low-voltage printed electronics is the low capacitance of many printed gate dielectrics (i.e., the printed gate dielectric layers are too thick and their dielectric constants are too small), which necessitates larger gate voltages to switch the transistors. Therefore, low-voltage, high-speed printed electronics requires

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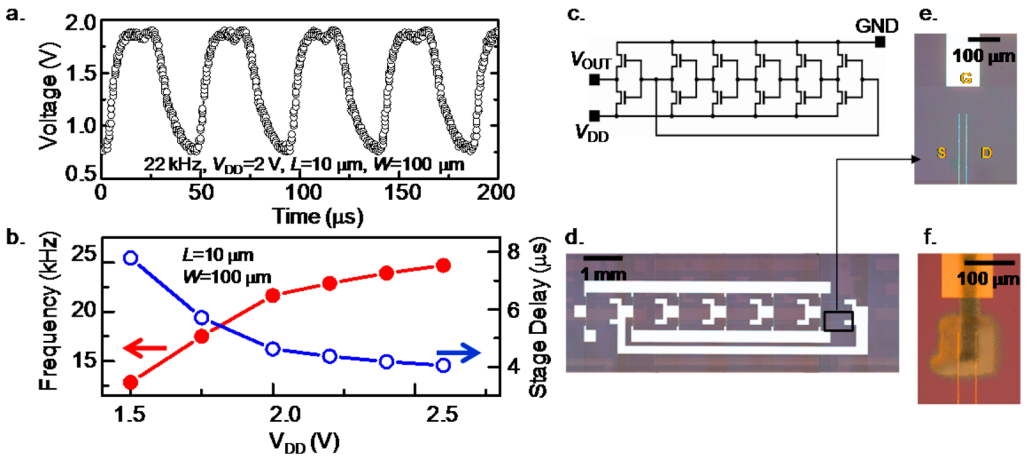

Figure 1. Fast, printed five-stage CNT ring oscillators employing high-capacitance ion gel gate dielectrics. (a) The output signal of a CNT ring oscillator with a frequency of 22 kHz and stage delays of 4.5 μs at V_{DD} = 2 V. The TFTs have channel length of 10 μm, channel width of 100 μm, and ion gel thickness of 1.2 μm. (b) Frequency and stage delay times of the ring oscillator as functions of supply voltage V_{DD}. (c) Circuit diagram of the ring oscillator with a buffer stage. (d) Photograph of the Au contacts in the ring oscillator before printing. (e) Photograph of the Au source, drain, and gate contacts for a single TFT before printing. Source and drain electrodes are 2 μm in width. (f) Picture of a single TFT after all layers were printed, including semiconducting CNT network, ion gel dielectric, and PEDOT:PSS gate electrode.

a comprehensive approach where both the semiconductor and dielectric are carefully chosen and synergistically integrated.

We have recently reported printed thin film transistors (TFTs) and digital circuits that pair a high-mobility semiconductor layer based on semiconducting CNTs with a high-capacitance, printable electrolyte as the gate insulator.[31] The CNT layer, which was deposited from an aqueous ink, has high electron and hole mobilities enabling fast switching, and the high-capacitance gel electrolyte, printed using a solvent-based ink, affords low-voltage operation. Using these materials and an aerosol jet printing process, we demonstrated printed five-stage ring oscillators operating at 2 kHz with a 3 V supply, which corresponded to a delay of 50 μs per stage. At the time, these performance metrics represented a near record value for printed circuits. Following this initial demonstration, Ohno and colleagues subsequently fabricated ring oscillators with 12 μs stage delay at 4 V supply, using dry transfer printing of the CNT semiconductor layer and evaporated dielectric and metal layers,[25] thus suggesting the possibility of further improvements.

Here we report an order of magnitude reduction in switching times for aerosol jet printed, electrolyte gated CNT circuits which has been achieved by employing high-mobility semiconducting CNTs, controlling the thickness of the ion gel gate dielectric, reducing the transistor channel lengths, and minimizing parasitic capacitances and resistances. The fastest circuits operate at 1.2 μs stage delays and 2.2 V (Figure S1). These results are the fastest low-voltage switching speeds in printed electronics reported to date, and the speeds are sufficient for many high value applications including video display backplanes. Additionally, by systematically examining device metrics as a function of TFT architecture, this work provides a clear roadmap for future performance enhancements.

Figure 1a displays the output signal generated by a representative (but not the fastest) five-stage ring oscillator, with transistors having 10 μm channel lengths and 100 μm channel widths. At supply voltage V_{DD} as low as 2 V, the output frequency of the circuit was 22 kHz, which is about 1 order of magnitude faster than our previous report.[31] The output frequency, f, increased from 13 to 25 kHz as V_{DD} increased from 1.5 to 2.6 V, shown in Figure 1b (red solid circles). The stage delay time (blue open circles), t, was estimated from $t = 1/(2Nf)$, where N = 5 is the number of stages in the ring oscillator. At V_{DD} = 2.6 V, the shortest stage delay time for this oscillator was 4 μs.

As illustrated in the circuit diagram of Figure 1c, the printed ring oscillator consisted of five inverter stages and a buffer stage, where each stage employed two identical ion gel-gated ambipolar CNT TFTs. The channel dimensions were defined by 2 μm wide Au source/drain electrodes, which were prepatterned on a Si/SiO_2 substrate by photolithography. The layout of patterned Au electrodes on the Si/SiO_2 substrate is shown in Figure 1d, and an expanded view of one TFT is shown in Figure 1e. On top of the Au electrodes, semiconducting CNTs, ion gel gate dielectric, and poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS) layers were printed sequentially by the aerosol jet technique (see Experimental Section). The ion gel is an ionically conducting, electronically insulating composite based on ionic liquids such as 1-ethyl-3-methylimidazolium tetracyanoborate ([EMI][TCB]) and a structuring triblock copolymer, poly(styrene-*b*-methyl methacrylate-*b*-styrene) (PS−PMMA−PS), as described previously.[36−38] The photomicrograph of a completed ion gel gated CNT TFT is shown in Figure 1f. Importantly, by using narrow source and drain electrodes, the parasitic capacitance between the gate and the source and drain is reduced, and hence the parasitic peaks in the ring oscillator output signals are significantly attenuated compared to our previous results.[31]

With electrolyte gating, CNTs can perform as both p-type and n-type semiconductors, as indicated in the TFT transfer curve shown in Figure 2a. As printed, the CNT network is slightly p-doped. With a negative V_{GS} (gate-to-source voltage), the anions in the ion gel migrate to the ion gel/CNT interface, which enhances the p-doping of the CNTs and increases the hole conductivity. On the other hand, a small positive V_{GS} induces cations at the gel/CNT interface, extracting holes from nanotubes and eliminating the p-type transport. Continuing to apply more positive V_{GS} causes injection of electrons into the

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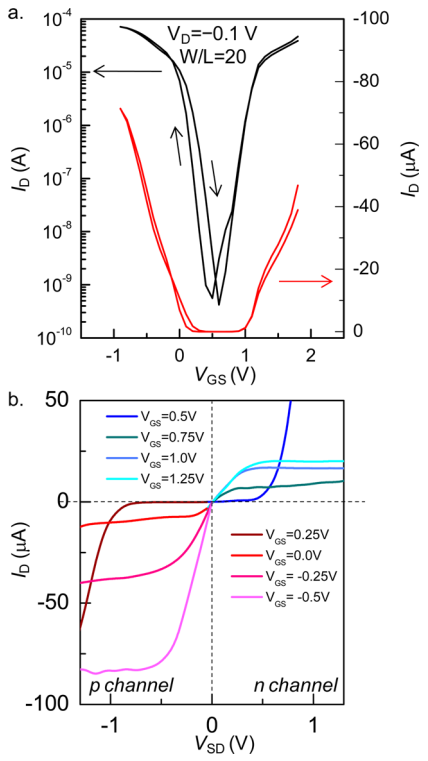

Figure 2. Performance of ion gel gated ambipolar CNT TFTs. (a) Transfer characteristics of a typical CNT TFT shown in linear and semilog scale. Channel dimension is 5 μm × 100 μm, V_D = −0.1 V, and V_G sweep rate is 75 mV/s. The average electron and hole mobilities are 20 cm^2/(V s), and the ON/OFF current ratio is 10^5. (b) Output characteristics of a CNT TFT, where the n-channel (blue curves) and p-channel transport (red curves) are shown separately.

nanotubes and enhances the electron conductivity. The high capacitance ion gel decreases the width of the contact barriers between Au and the conduction and valence bands of the CNTs, making the injection of both electrons and holes easier.[39] Therefore, the ion gel gated CNT TFTs are ambipolar transistors.

In TFTs based on CNT networks, there is always a trade-off between the carrier mobilities and the ON/OFF current ratio. The mobilities generally increase with the network coverage,[25,31] while the ON/OFF current ratio decreases with the CNT network coverage.[40,41] High mobility is the key to achieve fast switching speed, while high ON/OFF current ratio is important for low power consumption and high output voltage swing. In the CNT TFTs reported here, the areal coverage of the printed CNT network is ∼60% of the channel geometric area (see Figure S2), which is well above the percolation limit and thus might be expected to result in high OFF currents. However, we have employed high-purity SWCNTs that contain >99% semiconducting nanotubes in order to reduce shorting and gate-field screening by metallic tubes.[42] Therefore, even with CNT coverage much higher than the percolation limit, the printed gel-gated CNT TFTs are able to achieve high ON/OFF ratios at short channel lengths, i.e., 10^5 with V_D = −0.1 V and L = 10 μm, as shown in Figure 1a. The effective mobilities of the electrons and holes are about 20 cm^2/(V s), estimated from the linear fit of the I_D−V_{GS} transfer curve and average channel capacitance of ∼2 μF/cm^2 (Figure S3). The effective mobility here is estimated based on the channel dimensions, not accounting for the actual CNT network coverage, i.e., the number of nanotubes per area.

Figure 2b displays the typical output characteristics of the ambipolar CNT TFTs. With V_{GS} < 0.5 V, p-type transport dominates (red curves). The source−drain current, I_D, increases with the drain bias, V_{SD}, and shows clear linear and saturation regimes. With V_{GS} = 0.25 V, the TFT is in the OFF state as a typical p-type transistor when a small V_{SD} is applied. Note here the increase of I_D (tail of the curve) at more negative V_{SD} is due to electron injection. The electron injection also contributes to the slight slope of the saturation currents. With V_{GS} > 0.25 V, the TFT shows n-type transport (blue curves) and similar performance as the p side.

With two identical ambipolar TFTs we fabricated inverters, the basic digital logic gate. As shown in the inset of Figure 3a,

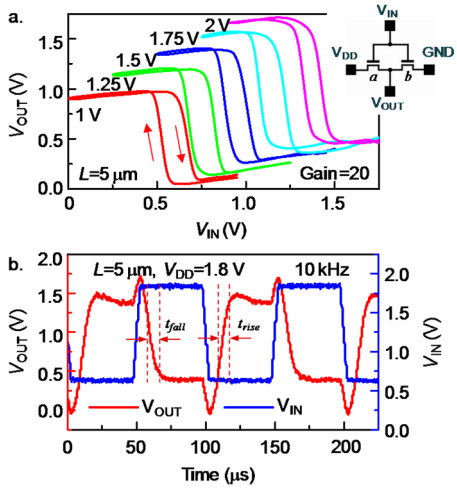

Figure 3. Performance of an ion gel gated CNT inverter. (a) Output characteristics of a CNT inverter with different V_{DD} biases (1−2 V). The inset shows the inverter diagram with two identical ambipolar TFTs. Channel dimensions are 5 μm × 100 μm. The inverter gain at 2 V is 20. (b) Dynamic response of a CNT inverter to a 10 kHz input signal; V_{DD} = 1.8 V and L = 5 μm. The output signal of the inverter (red) follows the input signal (blue). The rising and falling time of the input signal is ramped by 5% of the period.

the gate electrodes of both CNT TFTs were connected to the input. Transistor *a* functions more like a p-type TFT, while transistor *b* more like a n-type device. When input voltage (V_{IN}) is "low", i.e., 0 V, transistor *a* operates in the ON state and transistor *b* in the quasi-OFF state (since there is no real OFF state for ambipolar TFTs), leading to a "high" output voltage (V_{OUT}), i.e., V_{DD} (1 V), and vice versa. The transfer characteristics of a typical ion gel gated CNT inverter are shown in Figure 3a with V_{DD} = 1 V (red curve). V_{OUT} switches between 0 and 1 V, with the trip voltage around 0.5−0.7 V, and an average gain of 20. The hysteresis between the forward and backward sweeps is likely related to hysteresis in the TFT transfer curve (Figure 2a).

As we and others have pointed out,[7,31,43−45] for inverters based on ambipolar TFTs the channel may not be turned OFF completely, which effectively results in a static current. Hence, V_{OUT} may not be pulled all the way to V_{DD} or ground. With V_{DD} = 1 V, the output swing is about 95% V_{DD}, which indicates the presence of a small static current. As V_{DD} increases (transfer curves shown in color in Figure 3a), the transistor OFF current increases due to the higher drain bias (see Figure S4); hence,

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the output swing decreases, e.g., about 65% V_{DD} at V_{DD} = 2 V. The inverter trip voltage shifts with V_{DD}, which is due to the transistor OFF voltage changing with V_D, as shown in Figure S4.

A consequence of having a static inverter current is higher power consumption, which is characteristic of digital circuits based on ambipolar TFTs. In our previous work,[31] we discussed both the static and dynamic power consumption in ambipolar ring oscillators. In this work, the static power consumption for a single inverter stage was $P_{static} = IV_{DD} \approx 100\ \mu A \times 2\ V = 0.2$ mW, where I is the average current under operation. While this is rather high, a larger band gap ambipolar semiconductor, e.g., CNTs with smaller diameter, may mitigate the problem because it should have a broader "OFF" regime in the transfer characteristic.

The dynamic response of a printed inverter with channel length of 5 μm was measured at 10 kHz and V_{DD} = 1.8 V. As shown in Figure 3b, V_{OUT} (red) followed V_{IN} (blue). To better represent the circumstances in ring oscillators, the inverter was tested with an identical load inverter, and a square-wave signal with ramping time of 5% of the period was used as input voltage. The fall and rise time (t_{fall} and t_{rise}) of V_{OUT} indicates how fast the inverter can switch, which directly affects the stage delay in a ring oscillator. The spikes in the output signal likely result from parasitic capacitance at the ion gel/Au electrode interfaces, and the abrupt change of the input voltage, as discussed previously.[31] Here, t_{fall} and t_{rise} are estimated excluding the spikes. For example, t_{fall} is estimated from the duration of V_{OUT} switching from high to low at the falling edge, as shown in Figure 3b. We have used the switching time, $t = (t_{fall} + t_{rise})/2$, to characterize the speed of the inverters in order to qualitatively understand the limits of delay time in a ring oscillator. It is noteworthy that the inverter switching time does not equal the ring oscillator stage delay time. In fact, in a ring oscillator, the first inverter only has to switch its output to the trip voltage to trigger the second inverter switching. Therefore, t_{fall} and t_{rise} may be longer than the stage delay time in ring oscillators.

In a classic MOSFET, i.e., $I_D \sim \mu C_i(W/L)(V_G - V_{TH})^2$, where W and L are the channel width and length, μ is the CNT mobility, C_i is the sheet capacitance of the dielectric, and V_G and V_{TH} are gate and threshold voltages, respectively. Assuming $V_G - V_{TH} \approx V_{DD}$, the RC time constant can be estimated as $t \sim (V_{DD}/I_D)(C_iWL) \sim L^2/(\mu V_{DD})$. This indicates that, in an inverter in which channel resistance dominates, the switching time increases as L^2. However, as shown in Figure 4a, there are other factors in the system that affect the switching time.

The left panel of Figure 4a exhibits two inverters in series, representing two consecutive stages in a ring oscillator. The switching time of the inverter is the time required for V_B (the voltage at point B) to flip, after V_A (the voltage at point A) flips. The simplified equivalent RC circuit is illustrated in the right panel, where $R_{channel}$ is the channel resistance, R_{gate} is resistance of the gate electrode, R_{gel} is the bulk resistance of the ion gel dielectric, and C_{gel} is the ion gel capacitance. Importantly, the charging and discharging time of each stage is controlled by the total RC time constant. We discuss the contributions to the RC time constant below.

The gate resistance, R_{gate}, may not be ignored when estimating the RC time (for more details, see Figure S3) because the gate electrode material, PEDOT:PSS, has orders of magnitude lower conductivity than a typical metal. In this work, the gate electrodes were scaled to match the channel width but

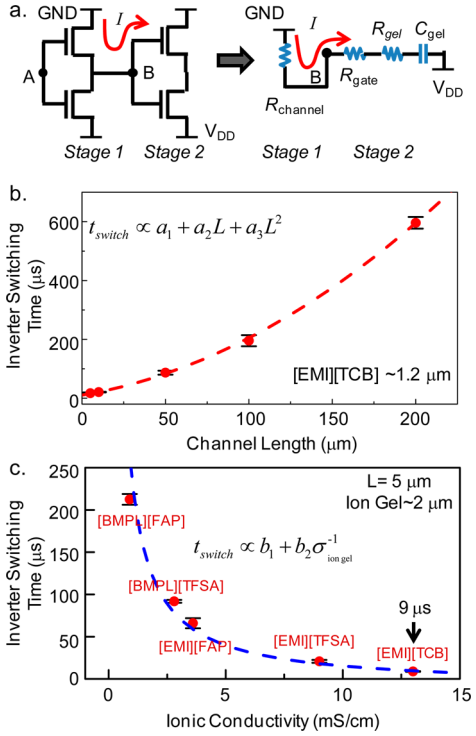

Figure 4. Parameters affecting the frequency and switching time of the CNT inverters. (a) Circuit diagram and equivalent circuit of two consecutive inverter stages. (b) Inverter delay time as a function of TFT channel length (W = 100 μm). The thickness of [EMI][TCB] ion gel is 1.2 μm, with ionic conductivity of 13 mS/cm. Fitting curve (red dashed line) shows $t_{delay} \sim L + L^2$. (c) Inverter delay time as a function of ion conductivities in ion gels. L = 5 μm, and ion gel thickness is 2.3 ± 0.3 μm. Fitting curve (dashed line) shows $t_{delay} \sim \sigma^{-1}$.

were fixed in length (50 μm) and thickness (1 μm). Consequently, the gate resistance of the inverters was independent of channel length and scaled with channel width as $R_{gate} \propto \rho W$, where ρ is the resistivity of PEDOT:PSS. Likewise, the bulk ion gel resistance R_{gel} may not be discounted. The printed gel area scaled with both channel dimensions, such that $R_{gel} = H/(\sigma WL)$, where σ is the ionic conductivity and H is the ion gel thickness. With thickness fixed, $R_{gel} \propto (WL)^{-1}$. Considering all three contributions, the total RC time of the inverter scales with length as $t_{switch} \sim (R_{channel} + R_{gate} + R_{gel})C_{gel} \propto (LW^{-1} + W + (WL)^{-1})(WL) \sim L^2 + W^2L^1 + L^0$. Figure 4b displays the measured inverter switching times as a function of TFT channel length, keeping the channel width constant (100 μm). [EMI][TCB] ion gel with a thickness of 1.2 μm was printed as the dielectric layer. Each data point represents the average and standard deviation of switching times measured from five inverters, at V_{DD} = 1.8 V. As expected, the switching time increases with channel length, and the data are well fit by $t_{switch} = a_1 + a_2L + a_3L^2$, a polynomial which follows from the discussion above. The a_2L term represents the contribution of the gate electrode, and a_3L^2 represents the channel dependence. Interestingly, the contribution of $R_{gel}C_{gel}$ to the total RC time constant (a_3) has no L dependence, as can be seen from the scaling relationships above.

However, R_{gel}, and thus the switching time, does depend on the ionic conductivity of the gel and on the printed gel layer thickness. The dependence of t on ionic conductivity is shown in Figure 4c. Five different ion gels each containing 10 wt %

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polymer and 90 wt % ionic liquid (see Experimental Section) were employed. The low weight percentage of polymer content ensured the ion conductivity is close to the pure ionic liquid.[37,46] The ionic liquids 1-ethyl-3-methylimidazolium tetracyanoborate ([EMI][TCB]), 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)amide ([EMI][TFSA]), 1-ethyl-3-methylimidazolium tris(pentafluoroethyl)trifluorophosphate ([EMI][FAP]), 1-butyl-3-methylimidazolium tris-(pentafluoroethyl)trifluorophosphate ([BMPL][FAP]), and 1-butyl-3-methylimidazolium bis(trifluoromethylsulfonyl)amide ([BMPL][TFSA]) have ionic conductivities varying from 0.9 to 13 mS/cm. As shown in Figure 4c, as the ionic conductivity increases, the inverter switching time decreases from 210 to 9 μs; the times were measured with devices having ~2 μm ion gel thickness and 5 μm source−drain channel lengths. Each data point shows the average and standard deviation of three inverters. As expected, the switching time scales as σ^{-1}, and $t_{switch} = b_1 + b_2\sigma^{-1}$ (blue dashed line) fits the data well. This indicates that in ion gel-gated TFTs higher ionic conductivity, i.e., faster ion motion, can lead to faster switching of the transistors.

Figure 4b,c demonstrates the contributions of the TFT channel and ion gel bulk resistance to the inverter switching time. Of course, the quantitative scaling relationships may vary if other circuit parameters change. For example, with ultrathin, high conductivity ion gels (i.e., small R_{gel}) or very conductive gate electrodes (i.e., small R_{gate}), the channel resistance alone will dominate the total *RC* time. Then the switching time will simply scale as L^2, rather than the polynomial relation we observe.

We anticipate that further decreases in the transistor dimensions, reducing the ion gel thickness,[47] and enhancing the ion gel ionic conductivity should improve the switching speed. It is instructive to consider quantitatively what delay times can be achieved. We estimate the resistance of each series element of the 10 μm channel length TFTs to be (see Figure 4a) $R_{channel} = V_D/I_D \approx 0.1$ V/100 μA = 1 kΩ; $R_{gel} = H/(\sigma WL) \approx 1\ \mu$m/(10 mS/cm × 10 μm × 100 μm) = 1 kΩ; and $R_{gate} \approx 1$ kΩ.[48] That is, for the shorter 10 μm channels we have investigated in this study, the resistances of the three elements are comparable. In order to achieve 1 MHz frequency operation, a factor of ~5 reduction in overall RC time constant is necessary, as we have shown here that 5 μs switching times are readily achievable with 10 μm long channels. The gate resistance can be reduced by using high-conductivity, printable material, such as metallic CNTs, or by scaling down the channel width (length of the gate electrode). Lower gel resistance requires electrolyte with higher ionic conductivity or a thinner gel layer. A 5-fold reduction implies a gel thickness of 200 nm, which is clearly feasible. There are several strategies that can lead to lower channel resistance. One is to increase the CNT network coverage, which will increase the effective mobility. Alternatively, scaling down the channel length will also lead to lower channel resistance and to decreased channel capacitance. An $L = 4$ μm channel will have ~5 times smaller RC constant than the sub-5 μs value we have achieved here, for example. Thus, making all of the changes described here should allow 1 μs delay times, or 1 MHz operating frequencies, to be obtained.

Finally, in considering switching speed, it is important to bear in mind that other "parasitic" parameters may exist in printed circuits that can increase signal propagation delays. One important example is parasitic capacitance, e.g., capacitance between the gate and the source/drain electrodes. Parasitic capacitance may be a particularly challenging problem in printed electronics where precision patterning is challenging and electrode roughnesses may be high. These factors will add to the overall *RC* time constants.

In conclusion, five-stage ion gel gated CNT ring oscillators can achieve fast frequencies >20 kHz, corresponding to stage delay times <5 μs at supply voltages below 3 V. These are the fastest printed circuits reported to date operating at low voltages. The switching times of the inverter stages are affected by the resistances of the semiconductor channel, gate electrode, and ion gel layer as well as the gate capacitance, and they increase with channel length and decrease with ion gel conductivity, following straightforward scaling arguments. Thus, the results suggest that even faster printed circuits can be achieved with shorter channel lengths, higher conductivity ion gels, thinner ion gel layers, and more highly conductive printed electrodes.

Experimental Section. *Materials.* High-purity semiconducting CNT inks dispersed in aqueous medium were synthesized by two-step density gradient ultracentrifugation (DGU)[49] using electric arc discharge grown (P2, Carbon Solutions Inc.) or raw HiPco (Nanointegris) SWCNTs. After ultracentrifugation, the centrifuge tubes were fractionated in 0.5 mm steps using a piston gradient fractionator (Biocomp Instruments Inc.), and the SWCNT electronic type purity of individual fractions was determined by optical absorbance spectroscopy (Varian Cary 5000 spectrophotometer). The fractions corresponding to semiconducting purity of >99% were combined to make the resulting CNT ink solution. The CNT ink was then dialyzed into 0.2% w/v sodium cholate aqueous solution in order to remove the density gradient medium (iodixanol) and to lower the surfactant concentration in the ink.

The ion gel inks were prepared by dissolving 9 wt % of ionic liquid and 1 wt % of poly(styrene-*b*-methyl methacrylate-*b*-styrene) (PS−PMMA−PS) in 90 wt % of ethyl acetate. The ionic liquids include 1-ethyl-3-methylimidazolium tetracyanoborate ([EMI][TCB]), 1-ethyl-3-methylimidazolium bis-(trifluoromethylsulfonyl)amide ([EMI][TFSA]), 1-ethyl-3-methylimidazolium tris(pentafluoroethyl)trifluorophosphate ([EMI][FAP]), 1-butyl-3-methylimidazolium tris-(pentafluoroethyl)trifluorophosphate ([BMPL][FAP]), and 1-butyl-3-methylimidazoliumbis(trifluoromethylsulfonyl)amide ([BMPL][TFSA]). The triblock copolymer was synthesized in-house with M_n = 13K−65K−13K and PDI = 1.3. 10 wt % of ethylene glycol was added into the PEDOT:PSS ink (1−1.4 wt % polymer in water, PH 500 from H.C. Stark) as a cosolvent in order to enhance the electronic conductivity.

Device Fabrication. The Cr (2 nm)/Au (28 nm) metal contacts and interconnections of CNT TFTs and circuits were evaporated on Si/SiO_2 substrates with electron-beam evaporation and patterned by photolithography. The transistor channel width was 100 μm, length varied from 5 to 200 μm, and the width of source/drain electrodes was 2 μm. By using a commercially available Aerosol-Jet printing system (Optomec, Inc.), functional materials were printed on substrate in ambient. Substrates were heated at 60 °C during printing to allow the solvent to dry. The nanotubes were first printed, and the substrate was rinsed with deionized water to remove residual surfactant. The nanotubes film was heated at 105 °C for 30 min to remove water before printing of the ion gel layer. A PEDOT:PSS gate electrode was printed on top of the ion gel and aligned with the channel. The completed TFTs were then

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heated at 105 °C in a glovebox for 1 h to remove residual solvent and water before electrical characterization. The ion gel layer thickness was measured by a confocal microscope.

Electrical Measurements. All devices were measured under 10^{-6} Torr at room temperature in a Lakeshore vacuum probe station. The electrical performance of TFTs and inverters were characterized by connecting two source meters (Keithley 236, 237) to source/drain electrodes and an electrometer (Keithley 6517A) to gate electrode. The input signal of inverters was generated by Agilent 33220 arbitrary-waveform generators. The dynamic responses of inverters and ring oscillators were acquired by a Tektronix TDS1002B digital oscilloscope.

■ ASSOCIATED CONTENT

Supporting Information

Fast, printed ion gel gated CNTs ring oscillator, parasitic resistance of gate electrode, transistor performance with various V_D. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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