An Array-Based Circuit for Characterizing Latent Plasma-Induced Damage

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Purpose

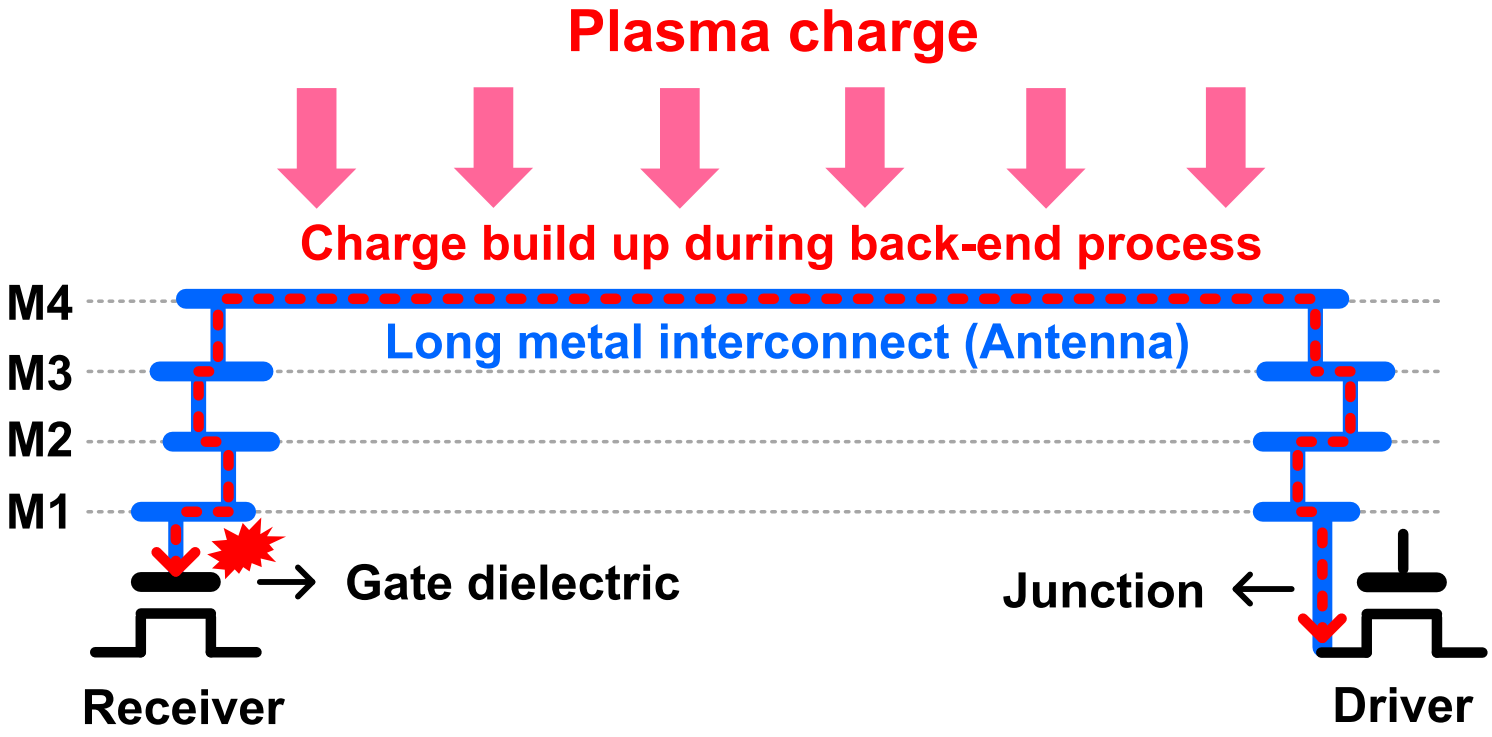
- **Design a dedicated on-chip array-based circuit for efficiently characterizing latent plasma-induced damage.**

- **Collect massive time-to-breakdown data from devices with various antenna topologies in a short test time.**

Outline

- **Plasma-Induced Damage (PID)**
- **Array-Based PID Characterization Circuit**
- **Antenna Design**
- **Stress Experiment Results**
- **Conclusions**

Plasma-Induced Damage (PID)



Z. Wang, *et al*., ICICDT 2005

- **Plasma charge generated during the fabrication process leads to damage in the gate dielectric manifesting as latent BTI and TDDB reliability issues.**
- **The contiguous metal structure referred to as “antenna”**

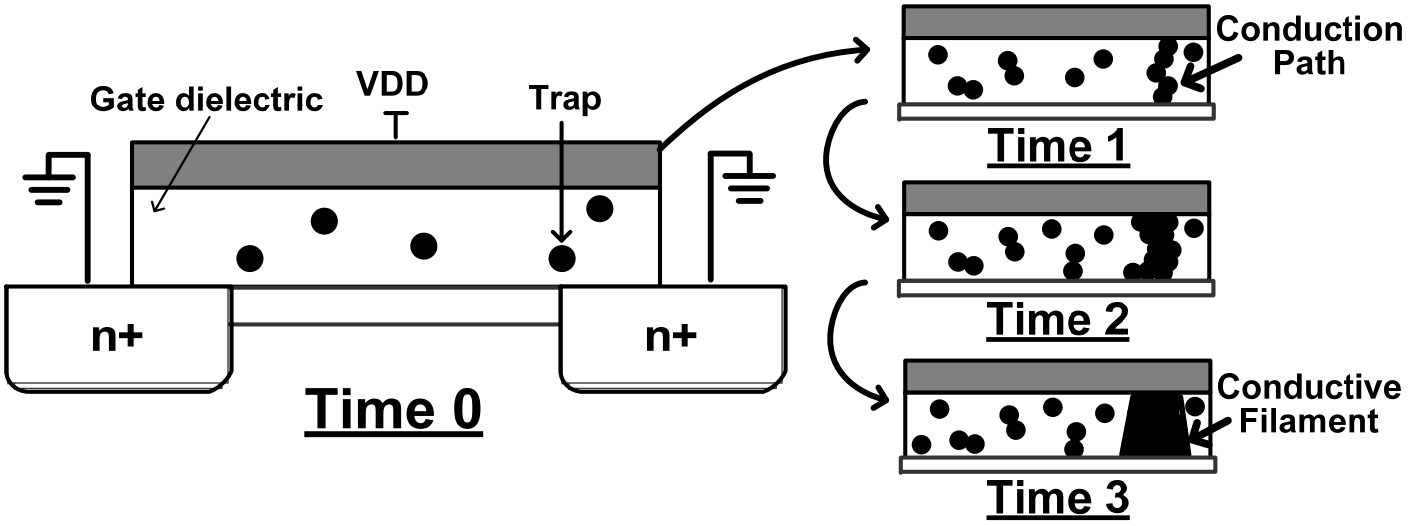
Characterizing "Latent" PID: BTI vs. TDDB

"Bias Temperature Instability"
"Time Dependent Dielectric Breakdown"

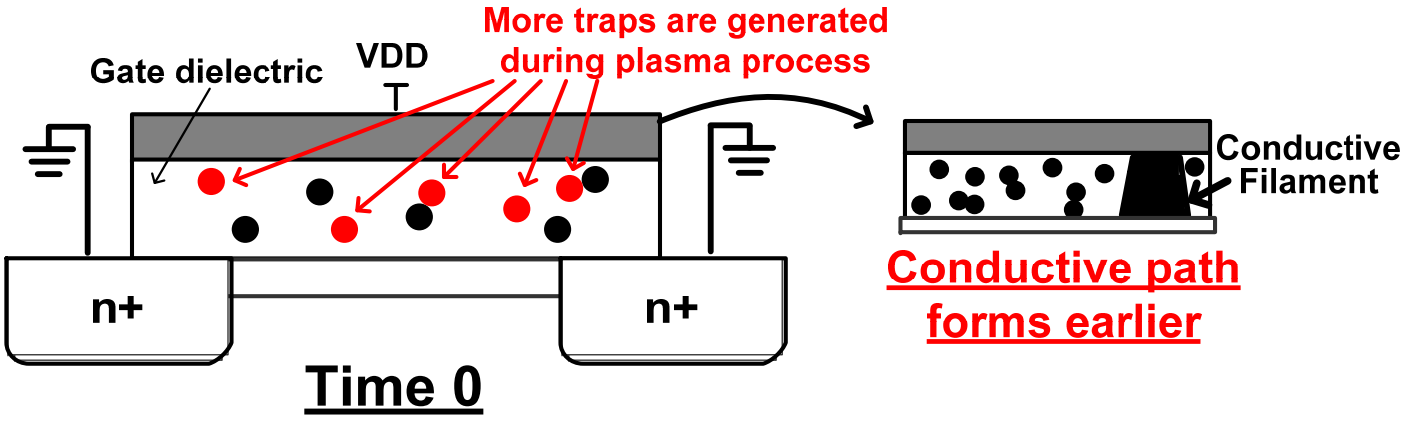
	BTI Test	TDDB Test
Impact of latent PID	Increased ΔVth	Shorter time-to-breakdown
Pros	Higher sensitivity Short test time	Suitable for array based test structures
Cons	Difficult to collect high quality data (fast BTI, unwanted recovery)	Lower sensitivity Longer test time

- **BTI & TDDB methods have to be considered together in order to fully understand the impact of latent PID on device and circuit reliability**

TDDB Aggravated by PID

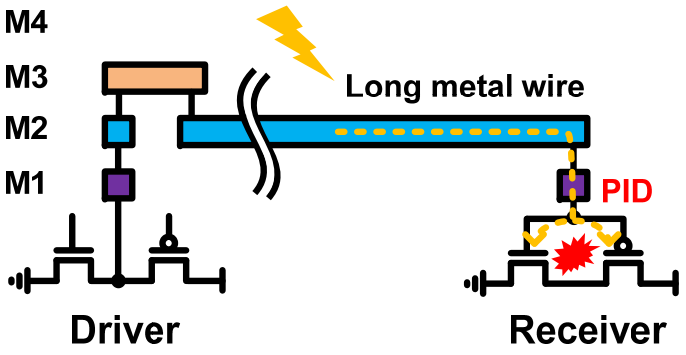
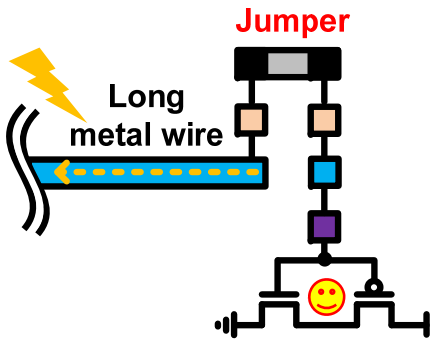
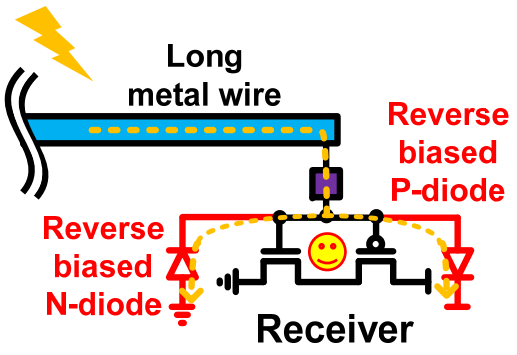


(a) TDDB mechanism



(b) TDDB in the presence of PID

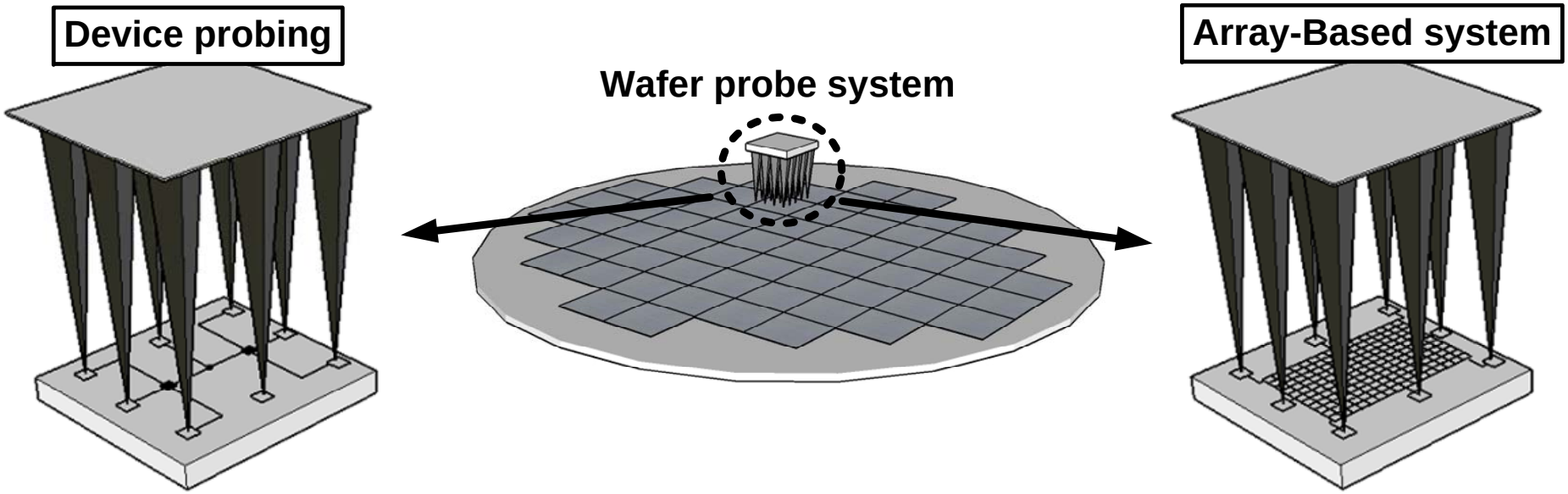
Circuit Impact and Mitigation Techniques

(a) PID in Inverter Chain	(b) PID Solution: Jumper Insertion	(c) PID Solution: Protection Diode
		
(1) Increased Vth shift *>> Delay↑* (2) Aggravated TDDB *>> Lifetime↓*	Inserting vias *>> R↑, Delay↑* *>> EDA tool support* *>> Time to market ↑*	Inserting diodes *>> C↑, Delay↑* *>> Leakage current↑* *>> EDA tool support* *>> Time to market ↑*

P. H. Chen, IEEE Circuits & Devices Magazine 2004

- **Mitigation techniques incur speed, power, cost, and time-to-market overhead**
- **PID impact on circuits need to be accurately assessed**

PID Characterization Method
Device Probing vs. Array-Based System

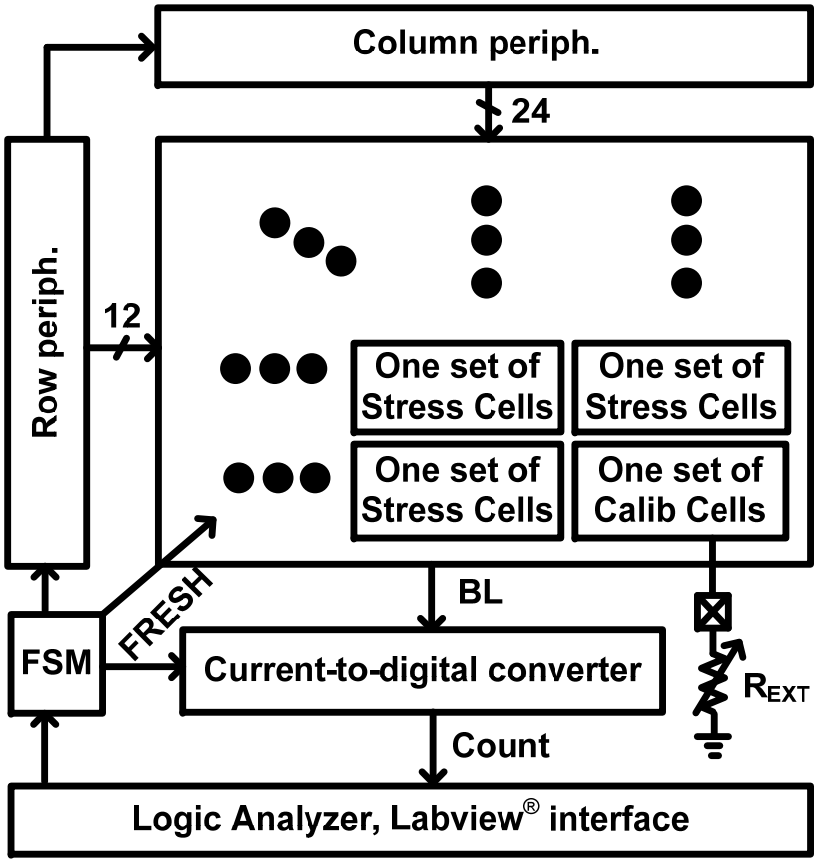


	Meas. time	Wafer area	Measurement	Scalability
Device Probing	1	1	Off-chip tester	No
Array-based	*1/n^2	*1/n^2	On-chip current to digital	Yes

***nxn array, parallel stress**

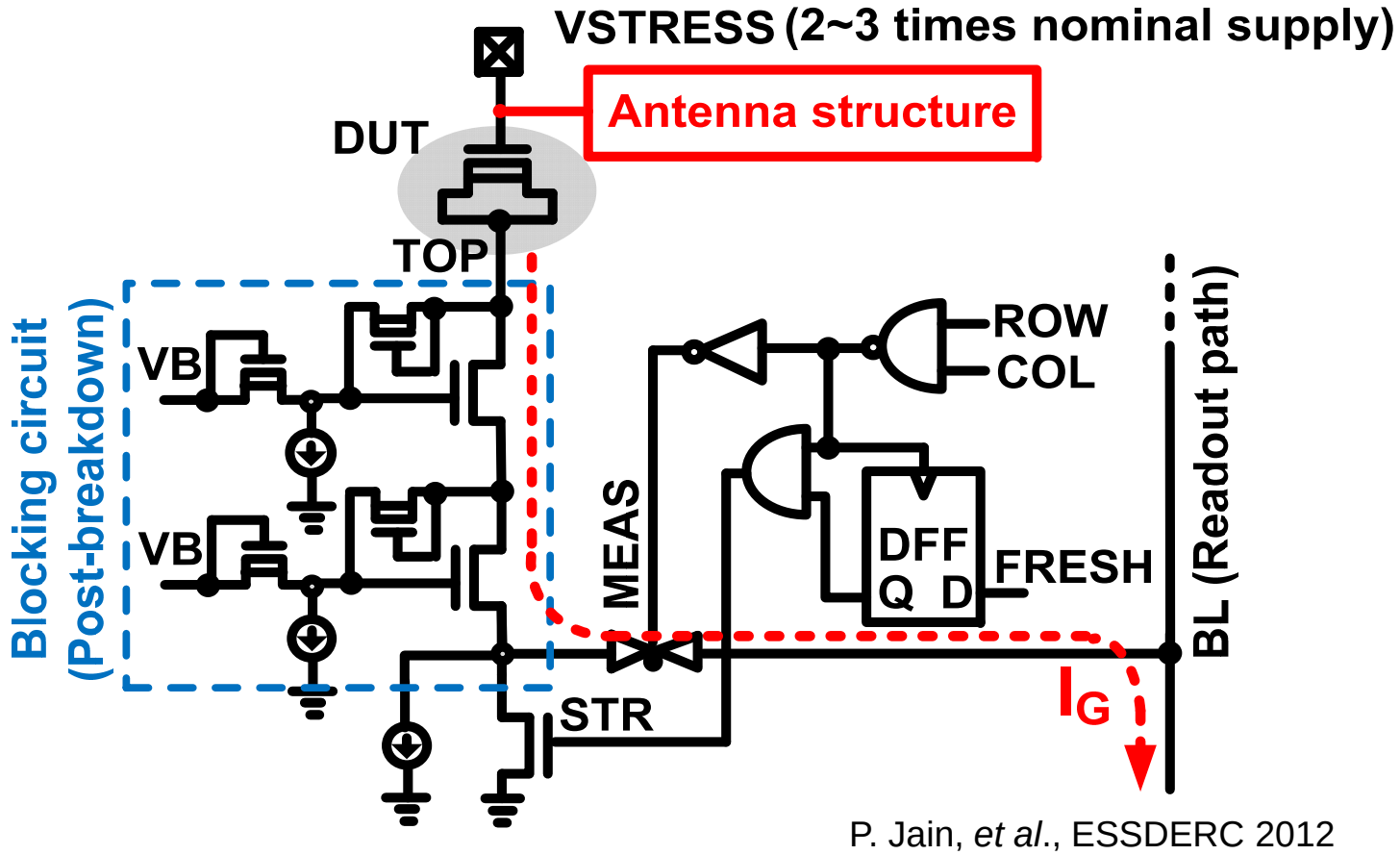
P. Jain, *et al*., ESSDERC 2012

Proposed PID Characterization Array



- **12x24 stress cells array allows parallel stress/serial measurement capability**
- **Three types of antenna implemented: plate-type antenna, fork-type antenna, no antenna**

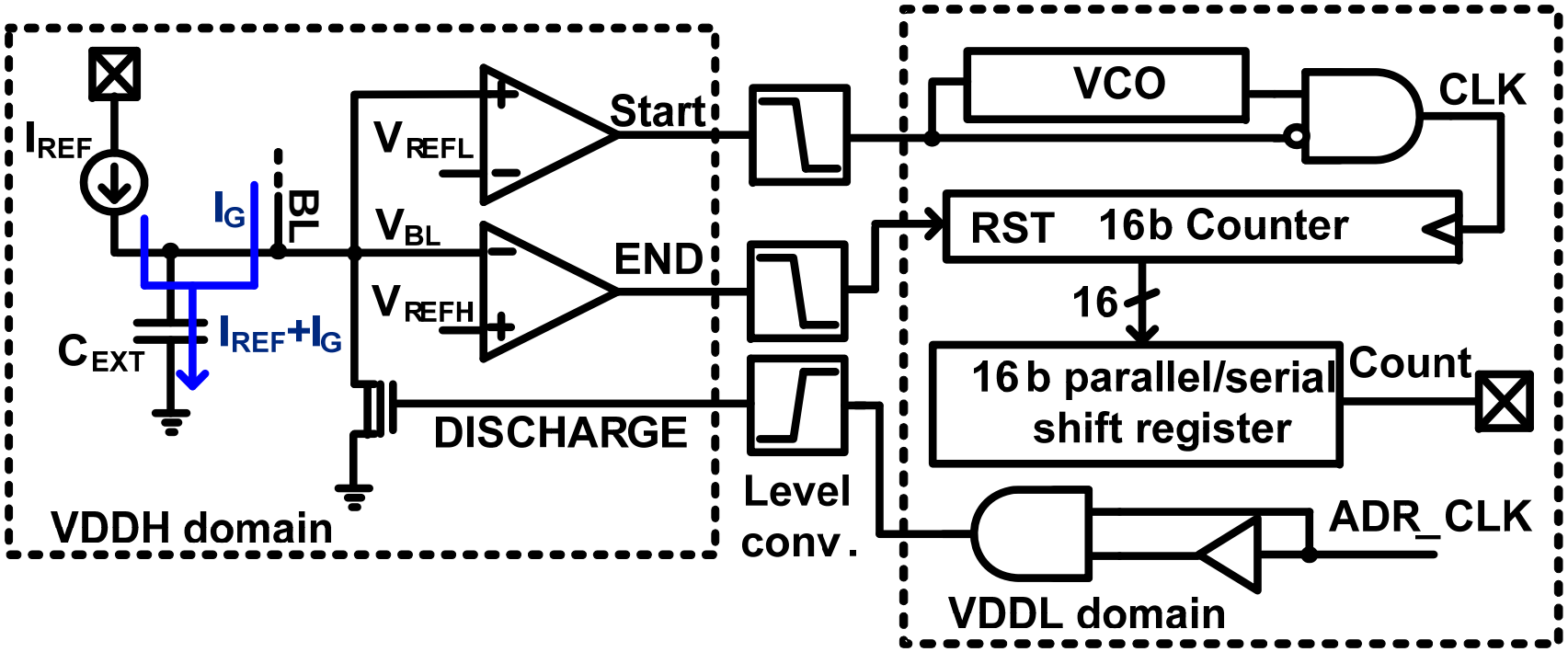
Unit Stress Cell with Antenna Structure



P. Jain, *et al*., ESSDERC 2012

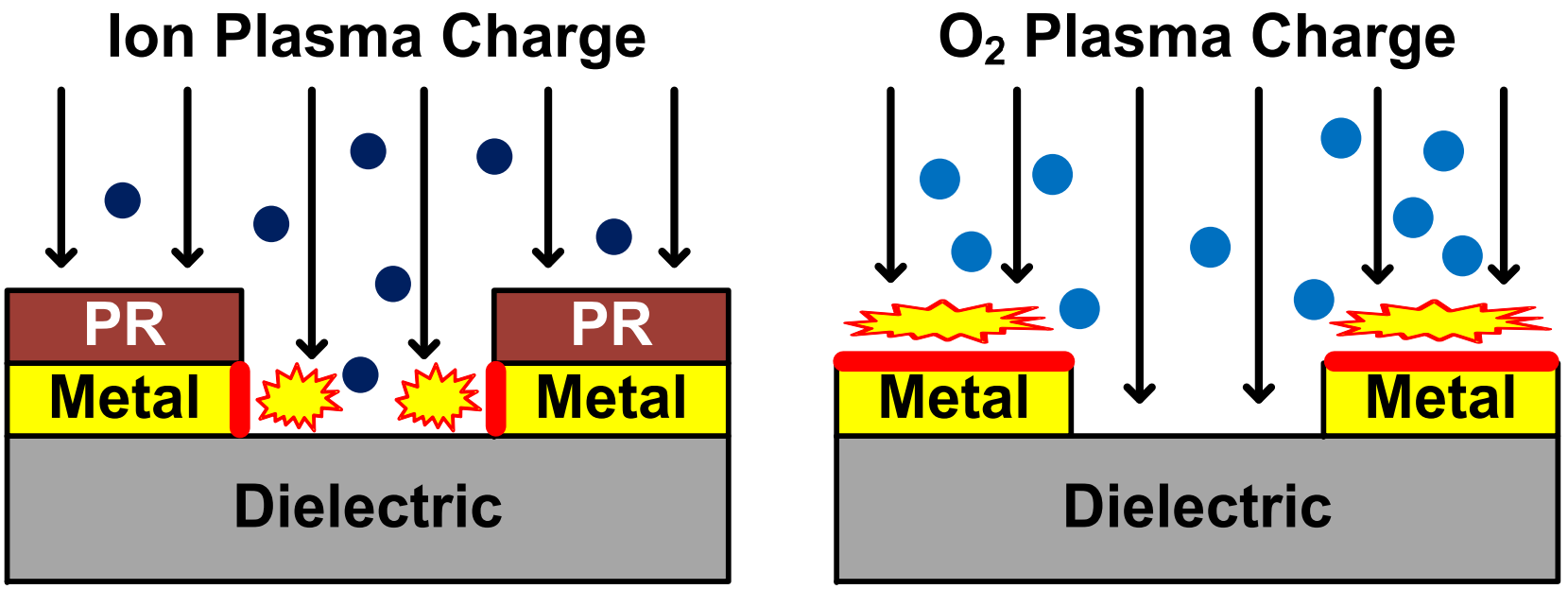
- **A NMOS with 5.0nm tox (2.5V) is used as a DUT**
- **Pre-breakdown: Full VSTRESS appears across DUT**
- **Post-breakdown: $2V_{GS}+2V_T$ drop blocks VSTRESS**

On-Chip Current-to-Digital Converter



- Fast evaluation of progressive TDDB behavior in the DUT cell
- I_G of each DUT measured sequentially and converted to a digital count and read off-chip

PID during Plasma Etching / Ashing

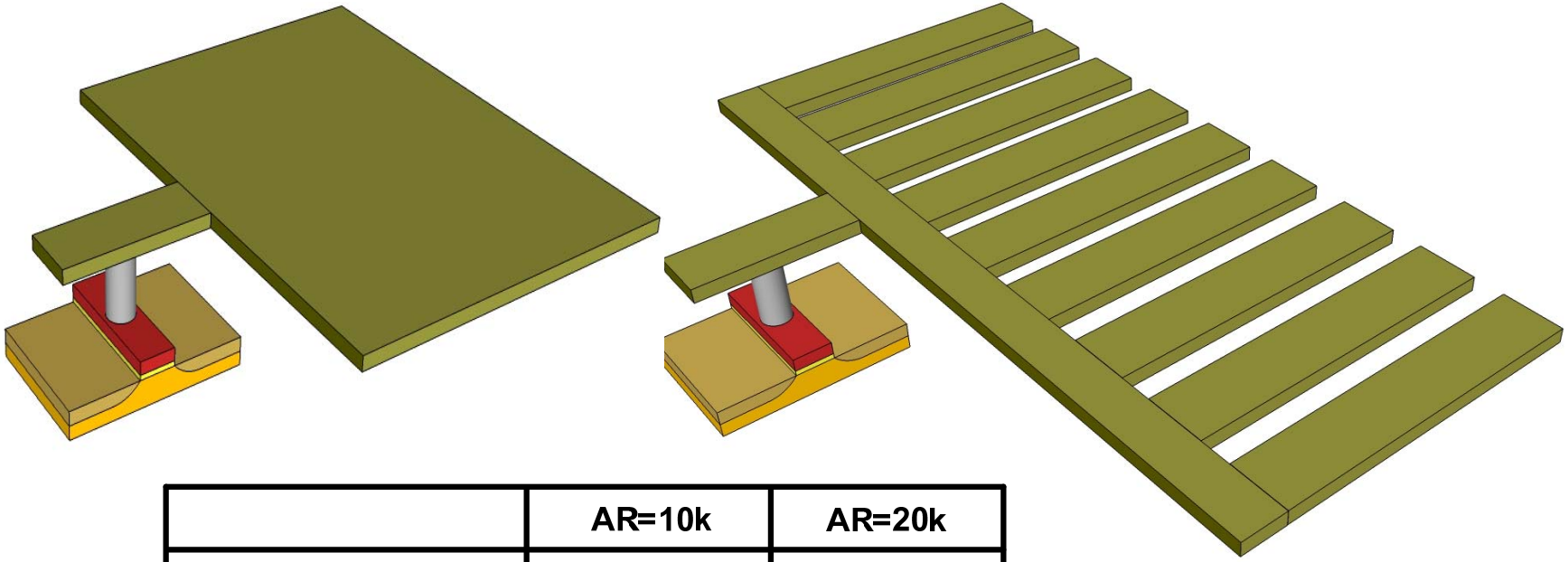


Plasma Etching **Plasma Ashing**

H. Shin, *et al*., IRPS 1992

- **Etching: plasma charging current is proportional to metal perimeter area**
- **Ashing : plasma charging current is proportional to metal top surface area**

Plate and Fork Type Antenna



	AR=10k	AR=20k
DUT with plate type antenna	64ea	32ea
DUT with fork type antenna	64ea	32ea

Reference DUT without antenna : 96ea

- **Fork type antenna consists of numerous metal fingers and hence occupies a larger silicon area than the plate type antenna for the same antenna ratio (AR)**

Metal Layer Usage and Antenna Ratio

Metal layer	Signal routing	Antenna	Jumper
M7			O
M5 ~ M6		O	
M2 ~ M4	O	O	
M1	O		

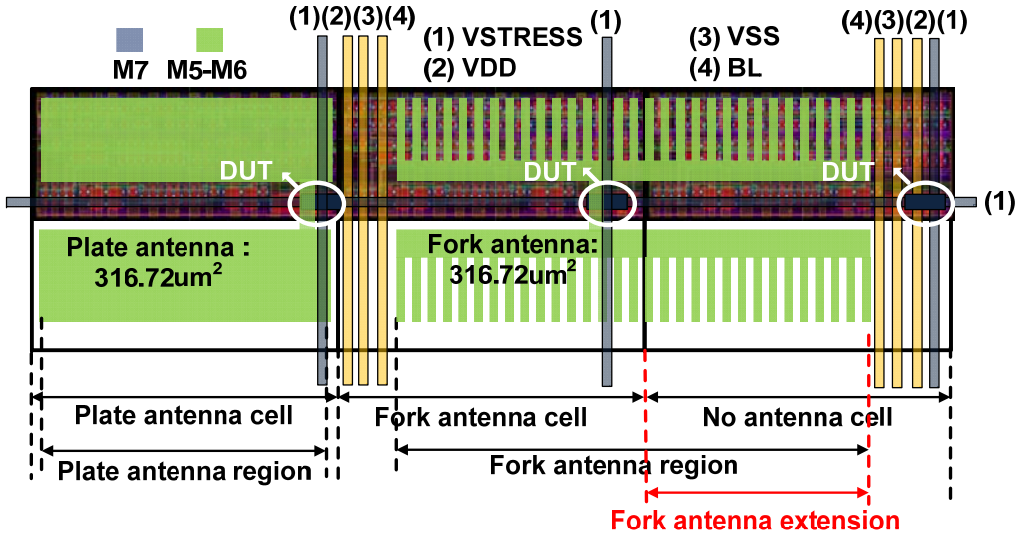
	AR=10k	AR=20k
M5, M6	316.72μm^2	607.76μm^2
M2, M3, M4	171.2μm^2	462.24μm^2
Total antenna area of each DUT	1147.04μm^2	2602.24μm^2
AR (Antenna Ratio)	10241	23234

$$AR = \frac{\text{total surface area of antenna structure}}{\text{gate area}}$$

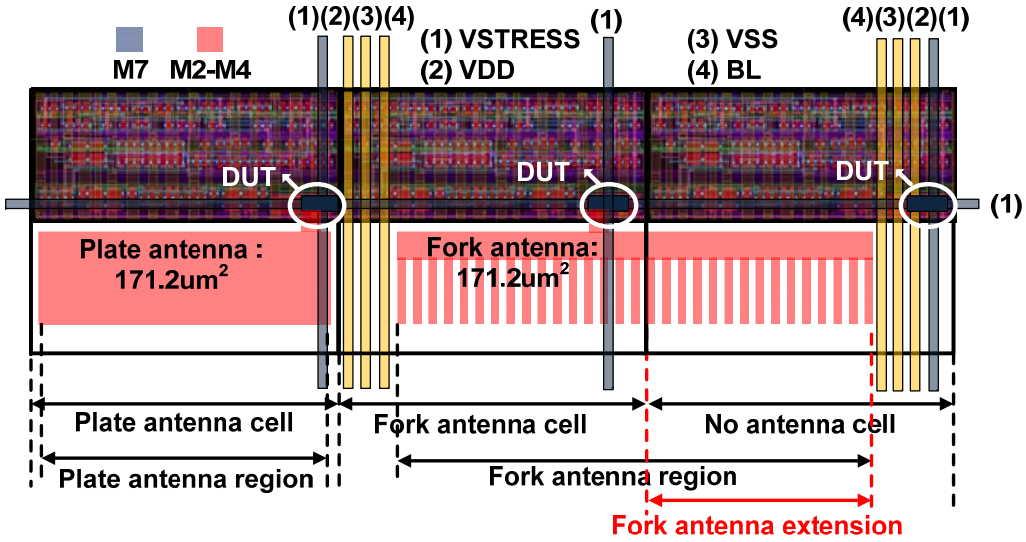
- Each antenna consists of 5 metal layers (M2-M6)
- AR values of 10k and 20k were implemented

Layout View of Three Stress Cells

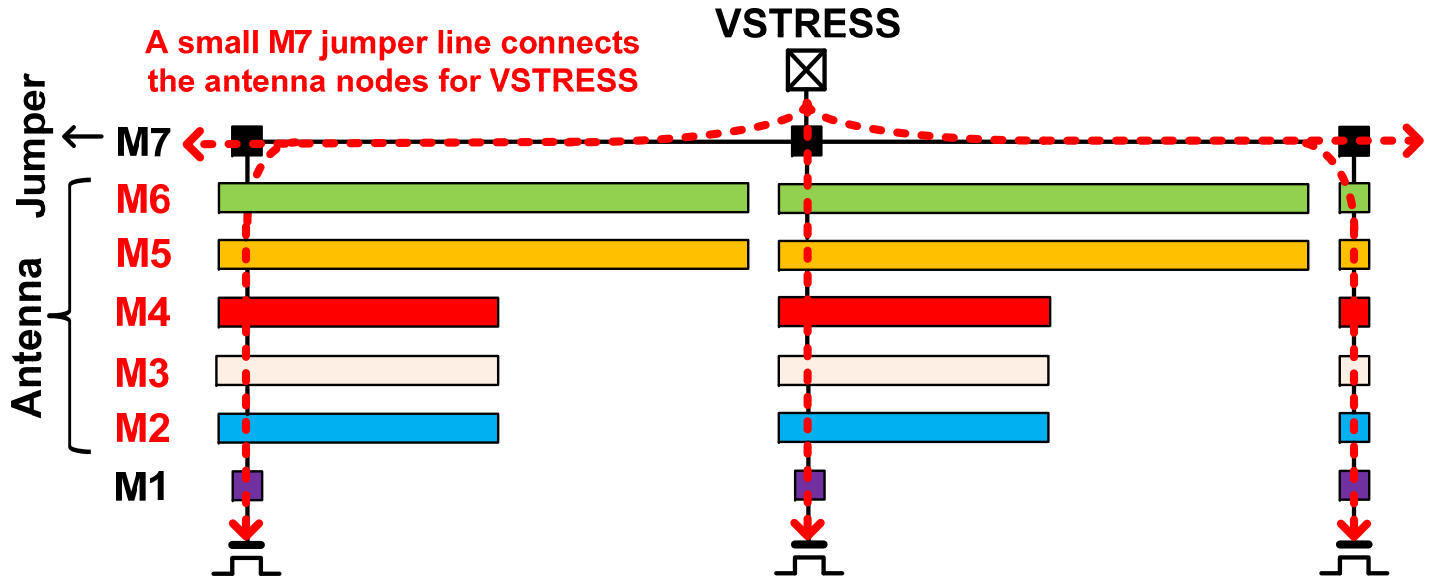
(a) Upper layers
[M5-M6]



(b) Lower layers
[M2-M4]



Cross-sectional View of Antenna Structure

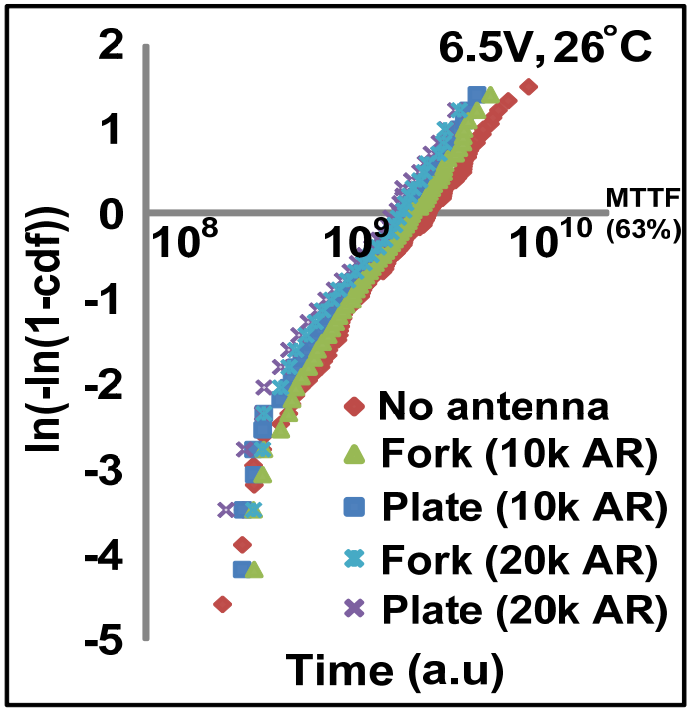


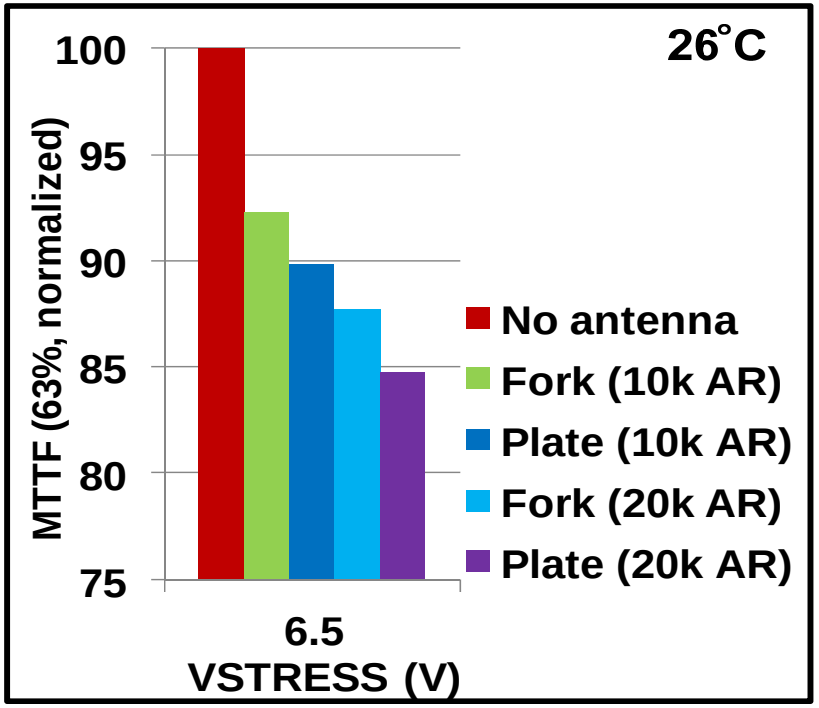
$$AR(\text{Plate, Fork}) \approx \frac{\sum \text{Area(M2-M6)}}{\text{Area(Gate)}} + \frac{\text{Area(M7)}}{\text{Area(Gate)} \times (12 \times 24)}$$

$$AR(\text{No antenna}) \approx \frac{\text{Area(M7)}}{\text{Area(Gate)} \times (12 \times 24)}$$

- **A small M7 jumper line was used to maximize the PID damage occurring while forming layers M2-M6**

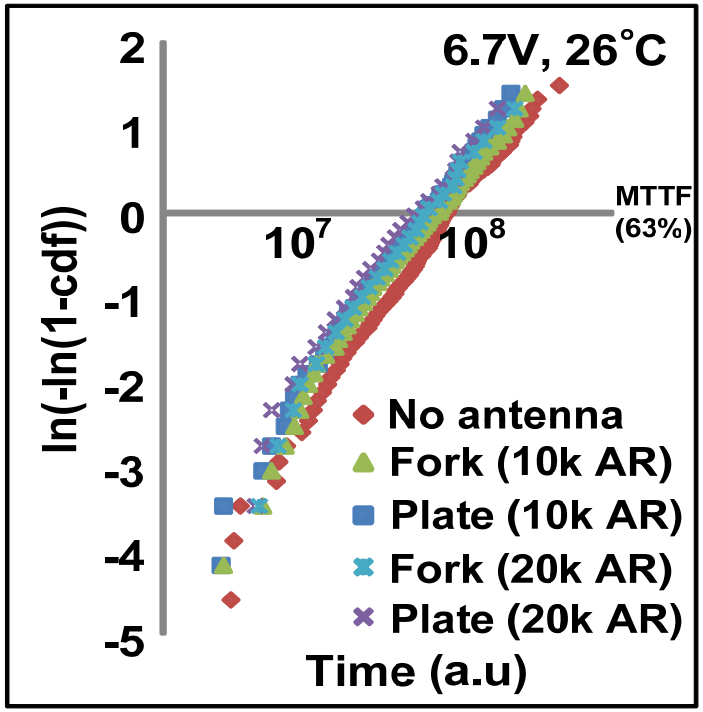
Measured Breakdown Data @ 6.5V

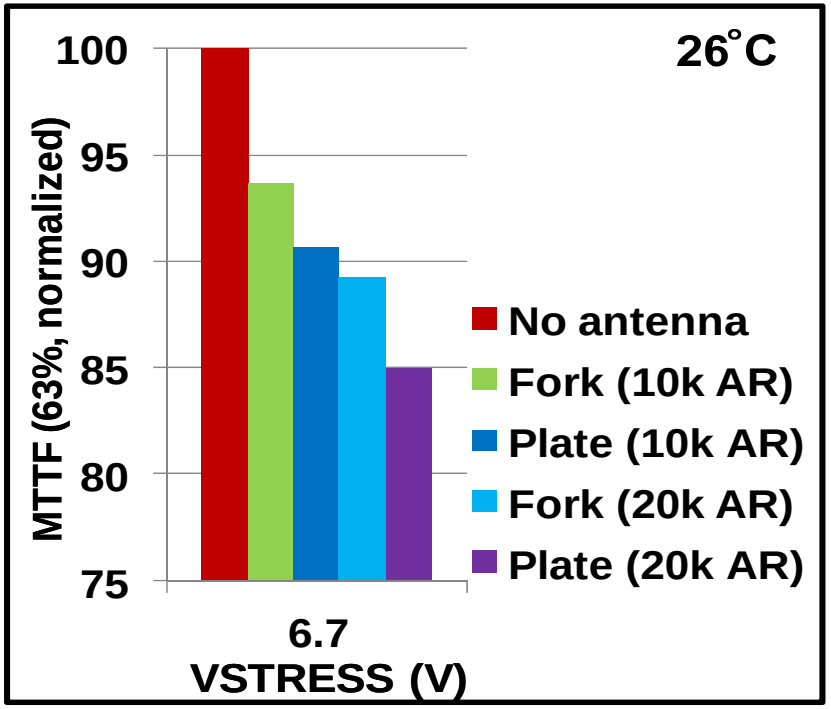




- **The cumulative time-to-breakdown curve shifts to the left for DUT array with larger antennas**
- **DUT array with plate antenna shows a consistently shorter lifetime compared to its fork type counterpart**
  - **Lifetime degradation of the fork (or plate) antenna with 10k AR: 7.7% (or 10.2%) for a 6.5V stress voltage**

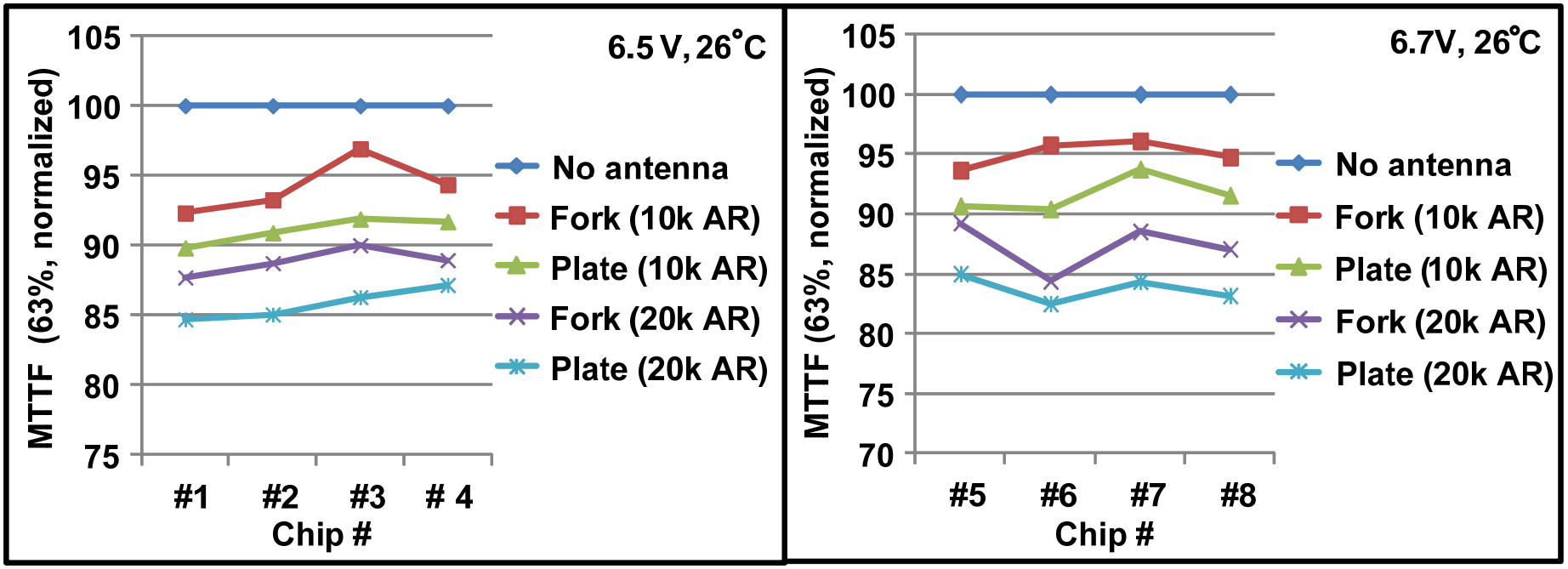
Measured Breakdown Data @ 6.7V





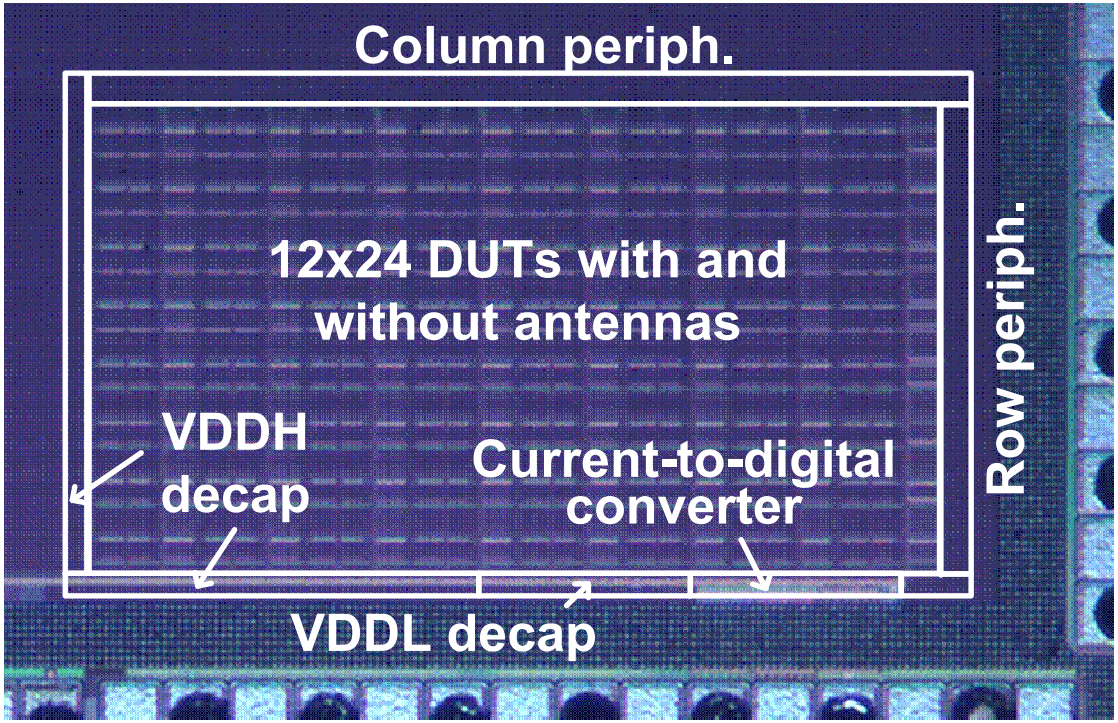
- Similar trends for a higher stress voltage of 6.7V
  - Larger antenna shows worse PID
  - Plate type antenna has worse PID than fork type

Chip-to-Chip Variation



- **Time-to-breakdown trend consistent across different chips**
- **Measured data suggests that PID during the etching is relatively small compared to that during the ashing**

65nm Die Photo and Chip Features



Process	65nm LP CMOS
VDD (core/IO)	1.2V / 2.5V
Stress Condition	6.5V, 6.7V @ 26ºC
Circuit Area	0.65x0.36mm^2

Conclusions

- **Array-based PID characterization circuit with various antenna structures fabricated in a 65nm process**
  - **Reduces the stress time and silicon area by a factor proportional to the number of DUTs to be tested**
  - **An effective research tool for understanding PID effects**
- **Time-to-breakdown curve shifts to the left for DUT array with larger antennas**
- **DUT with plate antenna has a consistently shorter lifetime compared to its fork type counterpart**
  - **Suggests that PID during the etching step is relatively small compared to that during the ashing step**