An Array-Based Circuit for Characterizing Latent Plasma-Induced Damage

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Purpose

• Design a dedicated on-chip array-based circuit for efficiently characterizing latent plasma-induced damage.

• Collect massive time-to-breakdown data from devices with various antenna topologies in a short test time.
Outline

• Plasma-Induced Damage (PID)
• Array-Based PID Characterization Circuit
• Antenna Design
• Stress Experiment Results
• Conclusions
Plasma-Induced Damage (PID)

- Plasma charge generated during the fabrication process leads to damage in the gate dielectric manifesting as latent BTI and TDDB reliability issues.
- The contiguous metal structure referred to as “antenna”

Z. Wang, et al., ICICDT 2005
Characterizing “Latent” PID: **BTI** vs. **TDDB**

“**Bias Temperature Instability**”
“**Time Dependent Dielectric Breakdown**”

<table>
<thead>
<tr>
<th>Impact of latent PID</th>
<th>BTI Test</th>
<th>TDDB Test</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Increased $\Delta V_{th}$</td>
<td>Shorter time-to-breakdown</td>
</tr>
<tr>
<td><strong>Pros</strong></td>
<td>Higher sensitivity</td>
<td>Suitable for array based test structures</td>
</tr>
<tr>
<td></td>
<td>Short test time</td>
<td></td>
</tr>
<tr>
<td><strong>Cons</strong></td>
<td>Difficult to collect high quality data (fast BTI, unwanted recovery)</td>
<td>Lower sensitivity</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Longer test time</td>
</tr>
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</table>

- BTI & TDDB methods have to be considered together in order to fully understand the impact of latent PID on device and circuit reliability.
TDDB Aggravated by PID

(a) TDDB mechanism

More traps are generated during plasma process

(b) TDDB in the presence of PID

Conductive path forms earlier
## Circuit Impact and Mitigation Techniques

### (a) PID in Inverter Chain
- **Driver**
- Long metal wire
- **Receiver**
- PID

### (b) PID Solution: Jumper Insertion
- **Receiver**
- Jumper
- Long metal wire

### (c) PID Solution: Protection Diode
- **Receiver**
- Reverse biased P-diode
- Reverse biased N-diode

<table>
<thead>
<tr>
<th>Impact</th>
<th>Mitigation</th>
<th>Speed</th>
<th>Power</th>
<th>Cost</th>
<th>Time-to-Market</th>
</tr>
</thead>
</table>
| (1) Increased Vth shift  
   >> Delay↑  
| (2) Aggravated TDDB  
| >> Lifetime↓  | Inserting vias  
| >> R↑, Delay↑  
| >> EDA tool support  
| >> Time to market ↑  | Inserting diodes  
| >> C↑, Delay↑  
| >> Leakage current↑  
| >> EDA tool support  
| >> Time to market ↑  |


- Mitigation techniques incur speed, power, cost, and time-to-market overhead
- PID impact on circuits need to be accurately assessed
## PID Characterization Method
### Device Probing vs. Array-Based System

<table>
<thead>
<tr>
<th></th>
<th>Meas. time</th>
<th>Wafer area</th>
<th>Measurement</th>
<th>Scalability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device Probing</td>
<td>1</td>
<td>1</td>
<td>Off-chip tester</td>
<td>No</td>
</tr>
<tr>
<td>Array-based</td>
<td>*1/n²</td>
<td>*1/n²</td>
<td>On-chip current to digital</td>
<td>Yes</td>
</tr>
</tbody>
</table>

*nxn array, parallel stress

P. Jain, et al., ESSDERC 2012
Proposed PID Characterization Array

- 12x24 stress cells array allows parallel stress/serial measurement capability
- Three types of antenna implemented: plate-type antenna, fork-type antenna, no antenna
Unit Stress Cell with Antenna Structure

- A NMOS with 5.0nm tox (2.5V) is used as a DUT
- Pre-breakdown: Full VSTRESS appears across DUT
- Post-breakdown: $2V_{GS} + 2V_T$ drop blocks VSTRESS

P. Jain, et al., ESSDERC 2012
On-Chip Current-to-Digital Converter

- Fast evaluation of progressive TDDB behavior in the DUT cell
- $I_G$ of each DUT measured sequentially and converted to a digital count and read off-chip
PID during Plasma Etching / Ashing

• **Etching**: plasma charging current is proportional to metal perimeter area

• **Ashing**: plasma charging current is proportional to metal top surface area

H. Shin, et al., IRPS 1992
Plate and Fork Type Antenna

- Fork type antenna consists of numerous metal fingers and hence occupies a larger silicon area than the plate type antenna for the same antenna ratio (AR)

<table>
<thead>
<tr>
<th></th>
<th>AR=10k</th>
<th>AR=20k</th>
</tr>
</thead>
<tbody>
<tr>
<td>DUT with plate type</td>
<td>64ea</td>
<td>32ea</td>
</tr>
<tr>
<td>antenna</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DUT with fork type</td>
<td>64ea</td>
<td>32ea</td>
</tr>
<tr>
<td>antenna</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Reference DUT without antenna : 96ea
Metal Layer Usage and Antenna Ratio

<table>
<thead>
<tr>
<th>Metal layer</th>
<th>Signal routing</th>
<th>Antenna</th>
<th>Jumper</th>
</tr>
</thead>
<tbody>
<tr>
<td>M7</td>
<td></td>
<td></td>
<td>O</td>
</tr>
<tr>
<td>M5 ~ M6</td>
<td></td>
<td></td>
<td>O</td>
</tr>
<tr>
<td>M2 ~ M4</td>
<td>O</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>M1</td>
<td>O</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>AR=10k</th>
<th>AR=20k</th>
</tr>
</thead>
<tbody>
<tr>
<td>M5, M6</td>
<td>316.72μm²</td>
<td>607.76μm²</td>
</tr>
<tr>
<td>M2, M3, M4</td>
<td>171.2μm²</td>
<td>462.24μm²</td>
</tr>
<tr>
<td>Total antenna area of each DUT</td>
<td>1147.04μm²</td>
<td>2602.24μm²</td>
</tr>
<tr>
<td>AR (Antenna Ratio)</td>
<td>10241</td>
<td>23234</td>
</tr>
</tbody>
</table>

- Each antenna consists of 5 metal layers (M2-M6)
- AR values of 10k and 20k were implemented
Layout View of Three Stress Cells

(a) Upper layers [M5-M6]

(b) Lower layers [M2-M4]
Cross-sectional View of Antenna Structure

A small M7 jumper line was used to maximize the PID damage occurring while forming layers M2-M6

\[ \text{AR(Plate, Fork)} \approx \frac{\sum \text{Area(M2-M6)}}{\text{Area/Gate}} + \frac{\text{Area(M7)}}{\text{Area/Gate} \times (12 \times 24)} \]

\[ \text{AR(No antenna)} \approx \frac{\text{Area(M7)}}{\text{Area/Gate} \times (12 \times 24)} \]

- A small M7 jumper line was used to maximize the PID damage occurring while forming layers M2-M6
The cumulative time-to-breakdown curve shifts to the left for DUT array with larger antennas.

DUT array with plate antenna shows a consistently shorter lifetime compared to its fork type counterpart.

- Lifetime degradation of the fork (or plate) antenna with 10k AR: 7.7% (or 10.2%) for a 6.5V stress voltage.
• Similar trends for a higher stress voltage of 6.7V
  • Larger antenna shows worse PID
  • Plate type antenna has worse PID than fork type
Chip-to-Chip Variation

- Time-to-breakdown trend consistent across different chips
- Measured data suggests that PID during the etching is relatively small compared to that during the ashing
65nm Die Photo and Chip Features

<table>
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<tr>
<th>Process</th>
<th>65nm LP CMOS</th>
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<tbody>
<tr>
<td>VDD (core/IO)</td>
<td>1.2V / 2.5V</td>
</tr>
<tr>
<td>Stress Condition</td>
<td>6.5V, 6.7V @ 26°C</td>
</tr>
<tr>
<td>Circuit Area</td>
<td>0.65x0.36mm²</td>
</tr>
</tbody>
</table>
Conclusions

• Array-based PID characterization circuit with various antenna structures fabricated in a 65nm process
  – Reduces the stress time and silicon area by a factor proportional to the number of DUTs to be tested
  – An effective research tool for understanding PID effects

• Time-to-breakdown curve shifts to the left for DUT array with larger antennas

• DUT with plate antenna has a consistently shorter lifetime compared to its fork type counterpart
  – Suggests that PID during the etching step is relatively small compared to that during the ashing step