An Array-Based Circuit for Characterizing Latent Plasma-Induced Damage

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Abstract— **An array-based Plasma-Induced Damage (PID) characterization circuit with various antenna structures is proposed for efficient collection of massive PID breakdown statistics. The proposed circuit reduces the stress time and test area by a factor proportional to the number of Devices Under Test (DUTs). Measured Weibull statistics from a 12x24 array implemented in 65nm show that DUTs with plate type antennas have a shorter lifetime compared to their fork type counterparts suggesting greater PID effect during the plasma ashing process.**

Keywords - Plasma-induced damage; Aging; Time dependent dielectric breakdown; degradation

I. INTRODUCTION

Plasma etching and ashing are extensively used in silicon chip manufacturing. It is well known that the charge build-up in the metal lines during plasma processing can lead to high voltage stress conditions in the transistor gate dielectric thereby degrading the gate dielectric and device reliability. Experimental data shows that the time-to-breakdown worsens for transistors whose gates are connected to large metal structures [1]. Fig. 1 illustrates the PID phenomenon occurring in a gate dielectric during the formation of various metal layers [2]. The contiguous metal structure where the charge build up occurs is commonly referred to as an "antenna". Circuit designers rely on two methods to prevent the plasma process from inflicting noticeable lifetime degradation: (1) ensure that the Antenna Ratio (AR, defined as the area ratio between the antenna and the gate dielectric) does not exceed a given specification or (2) insert antenna diodes to provide a discharge path. Several studies show that the degree to which PID affects device reliability is a function of not only the AR, but also the topology of the antenna structure [2-6].
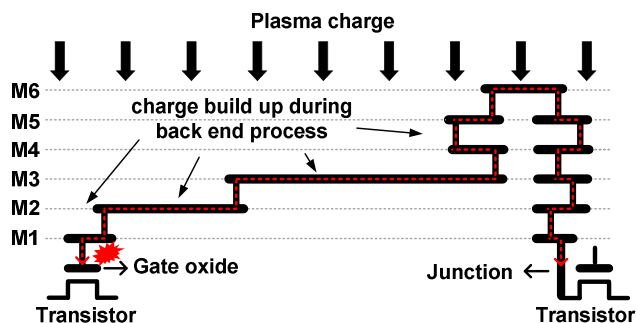

Figure 1. Plasma-Induced Damage (PID) during the back end processing steps results in gate oxide reliability issues [2].

Existing approaches for characterizing PID effects can be classified into four categories: (1) Gate-leakage test on fresh devices is a simple and fast method, but suffers from low sensitivity [1, 3]. (2) Constant-voltage Time Dependent Dielectric Breakdown (TDDB) test is accurate and provides higher sensitivity, but requires a long test time of over 1000 seconds per sample [1, 3]. (3) Ramped-voltage TDDB test was introduced in [1] to reduce the TDDB test time to 2 seconds per sample, but the main drawback is that the results do not match the standard TDDB results very well. (4) NBTI lifetime test has been generally accepted as the most sensitive method to detect PID (i.e. previous studies have shown noticeable difference in NBTI induced V_t shift for different AR ratios), but only limited data has been presented due to the difficulty in collecting high quality NBTI data [6]. A combination of the methods described above may have to be considered in order to fully understand the impact of latent PID on device and circuit reliability.

The foremost challenge to an effective PID mitigation strategy is in the collection of massive TDDB or NBTI data within a short test time from devices with various antenna topologies. Unfortunately, traditional device probing quickly becomes cumbersome and time consuming for this purpose due to the serial stress nature [7]. In this work, we demonstrate for the first time an array-based PID characterization circuit that can enable efficient collection of massive TDDB statistics. DUTs can be stressed in parallel while taking fast serial measurements administered through a convenient scan based interface. This feature reduces the test time and silicon area by a factor proportional to the number of DUTs. Another key benefit is that no special test equipment or elaborated test setups are required.

II. TEST ARRAY DESIGN

The proposed array-based PID characterization system shown in Fig. 2 consists of 12x24 stress cells, an on-chip current-to-digital converter, a Finite State Machine (FSM) control logic, column/row select circuits, and a scan interface. Although both thin oxide and thick oxide devices can be considered for the DUT, we chose to use the latter option as experimental data indicate that devices with oxides thinner than 2nm are more tolerant to PID effects [6]. Each stress cell contains an NMOS DUT with an oxide thickness of 5.0nm. Each DUT has a dimension of W=0.4µm, L=0.24µm. No protection diodes are connected to the gate of the NMOS transistors. The higher stress voltage (typically 3-4 times the IO
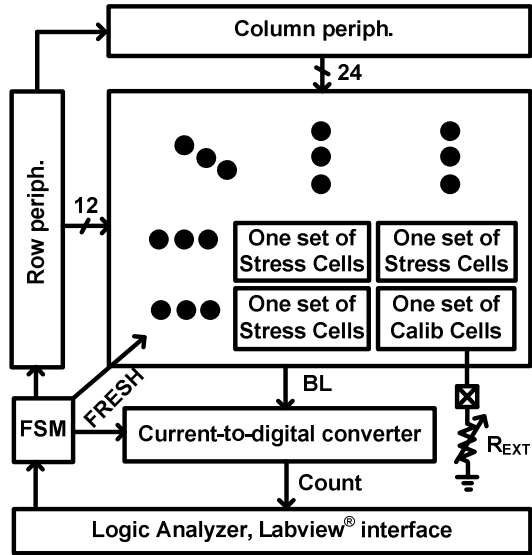
Figure 2. Diagram of the proposed array-based PID characterization circuit. One set of stress cells have three stress cells (i.e. two cells with antennas (plate and fork type) and one reference stress cell without an antenna).
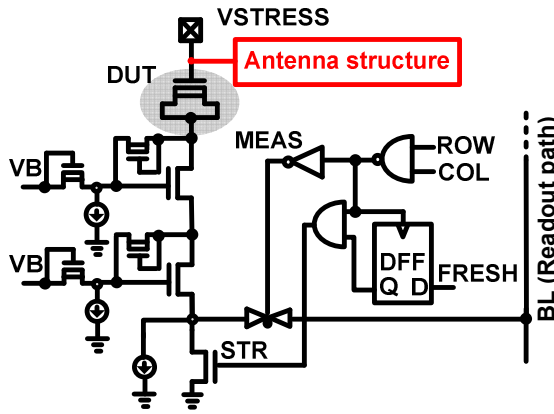

Figure 3. Single stress cell including DUT, antenna, and control circuits.

supply) and lack of an even thicker oxide device complicate the design of the stress cell implemented with IO devices only [8]. A stack of two blocking circuits with dynamic biasing shown in Fig. 3 was employed to protect stress cell circuits from the high stress voltage (VSTRESS). It was sufficient for the ~6.5V stress voltage that was to keep the measurement time small. An off-chip VSTRESS voltage was applied through a dedicated pad. The gate of DUT is connected to various antenna structures. Reference DUTs with no antennas are also implemented for comparison purposes. Gate current (I_G) of each DUT is measured sequentially through a global BitLine (BL) while the entire array is being stressed in parallel. The BL voltage is first pre-discharged and then pulled up by I_G. Any progressive TDDB behavior in the form of I_G is converted to a digital count by an on-chip current-to-digital converter shown in Fig.4. An optional I_{REF} is used to set the minimum count output. The dual reference comparator senses the 'START' and 'END' times for the counting operation. The count value is loaded into a shift register and serially read out through a convenient scan interface. A Labview® program compares the
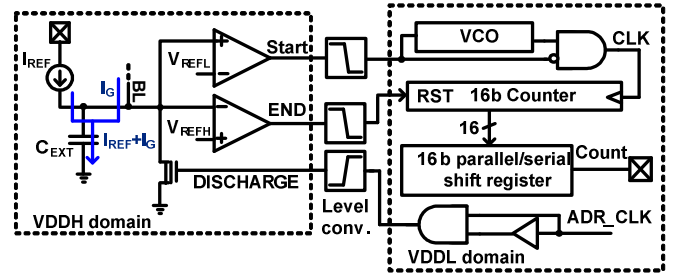

Figure 4. On-chip current-to-digital converter for monitoring soft and hard breakdown events in the DUT cell.

count with a user defined threshold and asserts a FRESH signal which prevents further stressing in case the cell is broken. A calibration cell and an external resistor (R_{EXT}) are used to translate the measured count to an absolute resistance value.

III. ANTENNA DESIGN

Plate and fork type antenna structures with AR values of 10k and 20k were implemented (Fig. 5). Among various candidates, we selected these two antenna topologies to compare the PID effect in an area-extensive antenna (plate type) versus a perimeter-extensive antenna (fork type). The number of DUTs for each antenna topology is given in Fig. 6. Although we were only able to include 64 or 32 DUTs for each antenna type due to the limited silicon area and the large antenna footprint, the proposed array design can be easily scaled up to collect. The layout view of the three stress cells (i.e. plate antenna, fork antenna, no antenna) is shown in Fig. 7. M5-M6 layers were dedicated to the antenna structures while portions of M2-M4 were used for antennas due to the areas reserved for the signal and power routing tracks. For the same AR, the fork antenna requires a larger silicon area than the plate antenna due to the metal fingers. Rather than increasing the stress cell area which will result in an unnecessarily large test chip, we utilize the empty space in the adjacent no antenna DUT cell for the
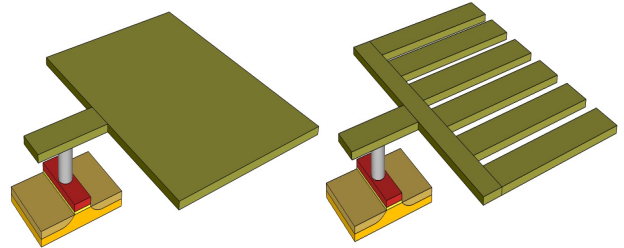

Figure 5. Conceptual view of the plate (left) and fork (right) type antenna structures implemented in the test array. Each antenna consists of 5 metal layers (M2-M6). Only one metal layer is shown here for simplicity. The fork type antenna consists of metal fingers and hence occupies a larger silicon area than the plate type antenna with the same AR.

	AR=10k	AR=20k
DUT with plate type antenna	64ea	32ea
DUT with fork type antenna	64ea	32ea

Reference DUT without antenna : 96ea

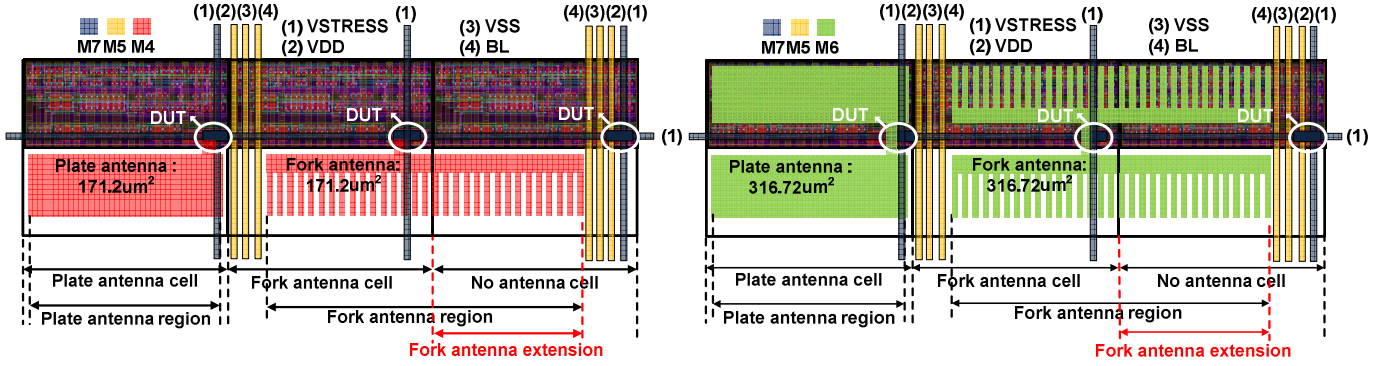Figure 6. The number of DUTs for each antenna type.

Figure 7. Layout view of three stress cells (i.e. two cells with antennas and one reference stress cell without an antenna). M4 layer (left) and M6 layer (right) views shown. Empty back end areas were filled with antenna structures for a compact array design.

Metal layer	Signal routing	Antenna	Jumper
M7			O
M5 ~ M6		O	
M2 ~ M4	O	O	
M1	O		

Figure 8. Metal layer usage in the 65nm PID characterization test chip.

	AR=10k	AR=20k
M5, M6	316.72μm²	607.76μm²
M2, M3, M4	171.2μm²	462.24μm²
Total antenna area of each DUT	1147.04μm²	2602.24μm²
AR (Antenna Ratio)	10241	23234

$$AR = \frac{\text{total surface area of antenna structure}}{\text{gate area}}$$

Figure 9. Antenna area of each metal layer and total Antenna Ratio (AR). Thick oxide NMOS devices used for the DUT have a dimension of W=0.4μm and L=0.28μm.
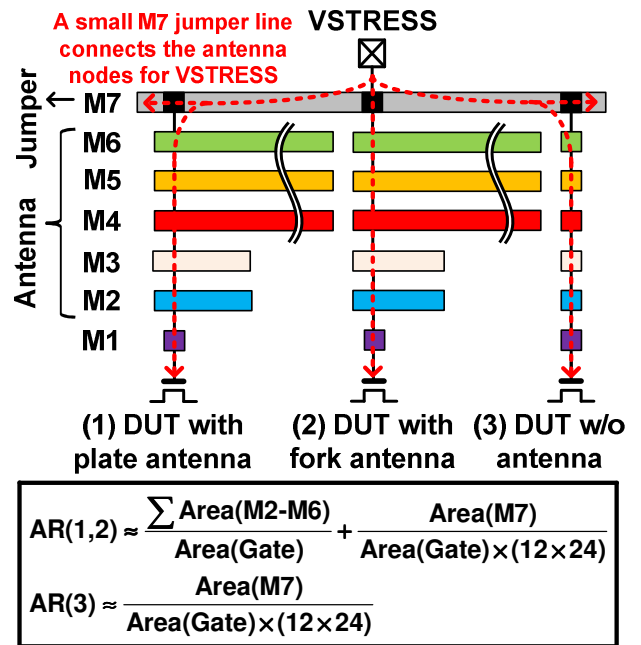

Figure 10. Cross-sectional view of antenna structure including a small M7 jumper connection for the common VSTRESS signal (top). Antenna ratio calculation (bottom).

large fork antenna. Usage of each metal layers in the test chip are listed in Fig. 8. To maximize the utilization of the metal layers and to achieve a dense chip implementation, we fill the empty areas of M2-M6 with antenna structures. Note that M1 to M4 layers were used for the signal and power routing tracks. The top surface areas for each metal layer along with the total antenna area are given in Fig. 9. Since we want each DUT to be affected by the plasma charge acting on its own antenna in M2-M6, a small jumper line on M7 was used as the global VSTRESS node as shown in Fig. 10. This well-known method prevents the global node from connecting to the DUTs prior to the M7 metal formation resulting in a realistic PID damage scenario. The cumulative ARs of the DUTs are given in bottom of Fig. 10. The AR due to the vias and contacts were negligible and therefore were omitted in the calculation. Note that each DUT has the same number of vias and contacts. Due to the small metal area of the M7 jumper and the large number of DUTs, PID due to the M7 layer itself can be ignored.

IV. STRESS EXPERIMENT RESULTS

Fig. 11 shows the measured time-to-breakdown data in Weibull scale for DUTs with different antenna structures stressed at 6.5V and 6.7V. The cumulative time-to-breakdown curves shift to the left for DUTs with larger antennas indicating an increased PID for gate dielectrics connected to larger antennas. The normalized Mean Time to Failure (MTTF, 63 percentile point) data under a 6.5V stress voltage in Fig. 12 shows that the fork (or plate) antenna with AR=10k has a 7.7% (or 10.2%) shorter lifetime compared to a reference device with no antennas attached. A DUT with a plate type antenna shows a consistently shorter lifetime compared to its fork type counterpart. Fork antennas have a larger perimeter surface area compared to plate antennas and hence become more susceptible to plasma damage during the etching process. However, our measured data shows the opposite trend with
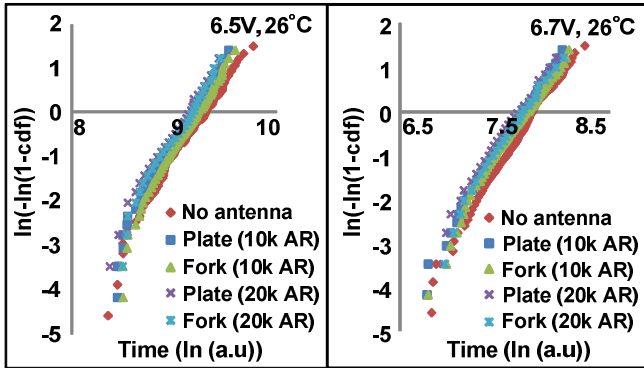
Figure 11. Measured breakdown data in Weibull scale for devices with different antenna topologies. Results are shown for two stress voltages; 6.5V (left) and 6.7V (right).
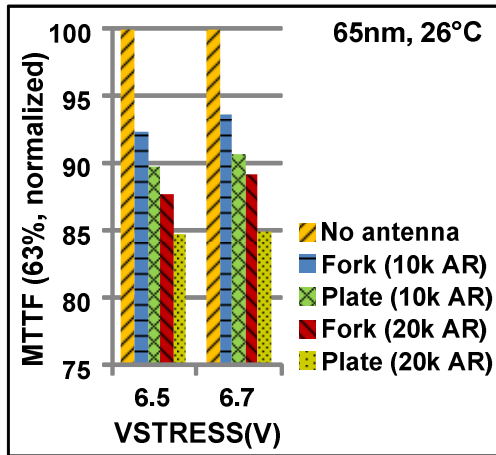

Figure 12. Normalized MTTF for devices with different antenna topologies stressed at 6.5V and 6.7V.

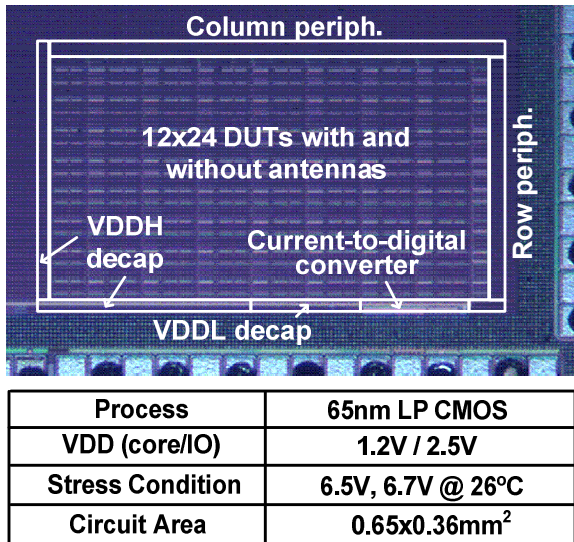| Process	65nm LP CMOS
VDD (core/IO)	1.2V / 2.5V
Stress Condition	6.5V, 6.7V @ 26°C
Circuit Area	0.65x0.36mm^2

Figure 13. Die photo and summary of the array-based PID characterization chip.

plate antennas having shorter lifetimes. This suggests that PID during the etching process is relatively small compared to that during the ashing process. Note that the charge build up during

ashing is facilitated when the resistance from the charge collecting surface to the gate dielectric is smaller as in the case of plate antennas. The die photograph of the 65nm test chip is shown in Fig. 13.

V.   CONCLUSIONS

Latent Plasma-Induced Damage (PID) affects device reliability and is a function of the AR as well as the specific topology of the antenna. The main challenge in characterizing PID effects using the TDDB lifetime method is in the collection of massive time-to-breakdown data from devices with various antenna topologies in a reasonable test time. In this work, we propose an array-based PID characterization circuit that can reduce the TDDB stress time and silicon area by a factor proportional to the number of DUTs to be tested. Two types of antennas, namely the area-extensive plate type antenna and the perimeter-extensive fork type antenna, were integrated in the test chip to understand PID effects according to the topology of the antenna. Experimental results show a clear shift in the Weibull curve for DUTs with larger ARs. In addition, DUTs with a plate type antenna have a consistently shorter TDDB lifetime compared to their fork type counterparts. This suggests that PID during the etching process is relatively small compared to that during the ashing process.

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