Duty-Cycle Shift under Asymmetric BTI Aging: A Simple Characterization Method and its Application to SRAM Timing

[1]Xiaofei Wang, [2]John Keane, [2]Pulkit Jain, [3]Vijay Reddy and [1]Chris H. Kim

[1]University of Minnesota, Minneapolis, MN

[2]Now at Intel Corporation, Hillsboro, OR

[3]Texas Instruments, Dallas, TX

xfwang@umn.edu

www.umn.edu/~chriskim/

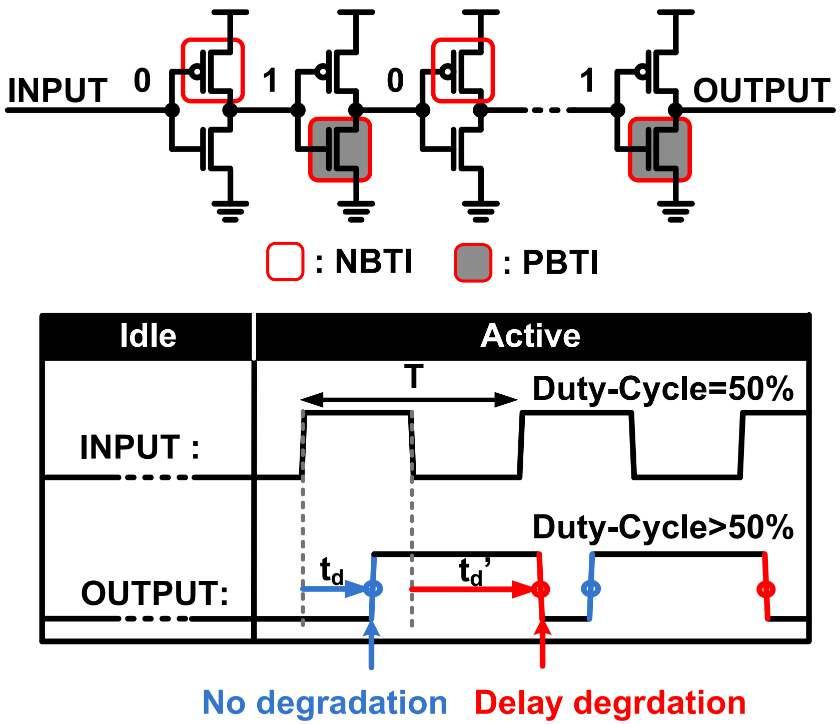
Purpose

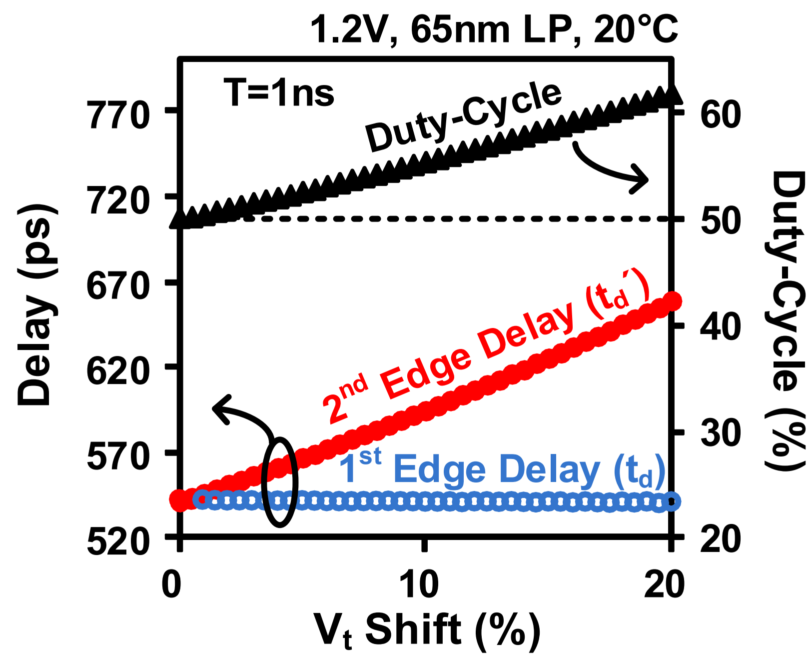
- Explore the impact of asymmetric BTI aging on circuit performance
- Measure the duty-cycle degradation using the silicon odometer framework
- Study duty-cycle degradation impact on SRAM timing

Outline

- Introduction to asymmetric BTI aging and its impact on different circuits
- Measurement method and test chip results
- Asymmetric aging impact on SRAM timing
- Summary

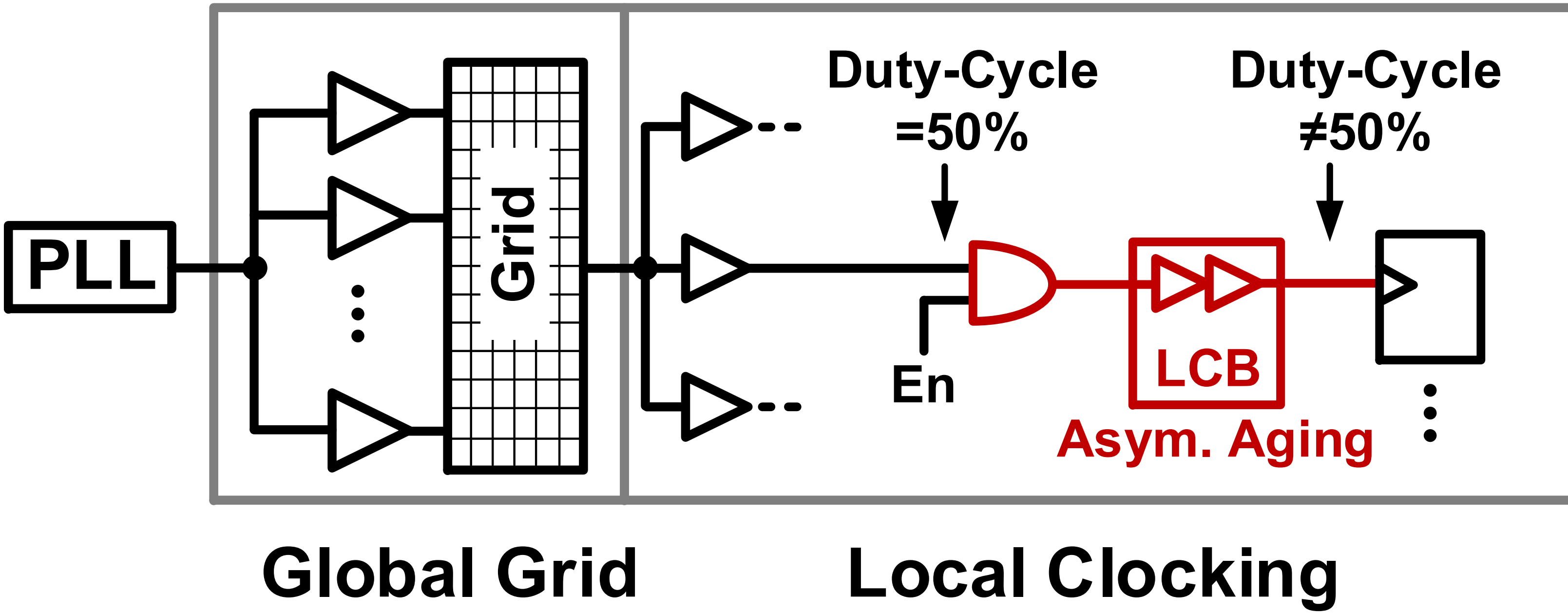
Asymmetric BTI Aging Effects





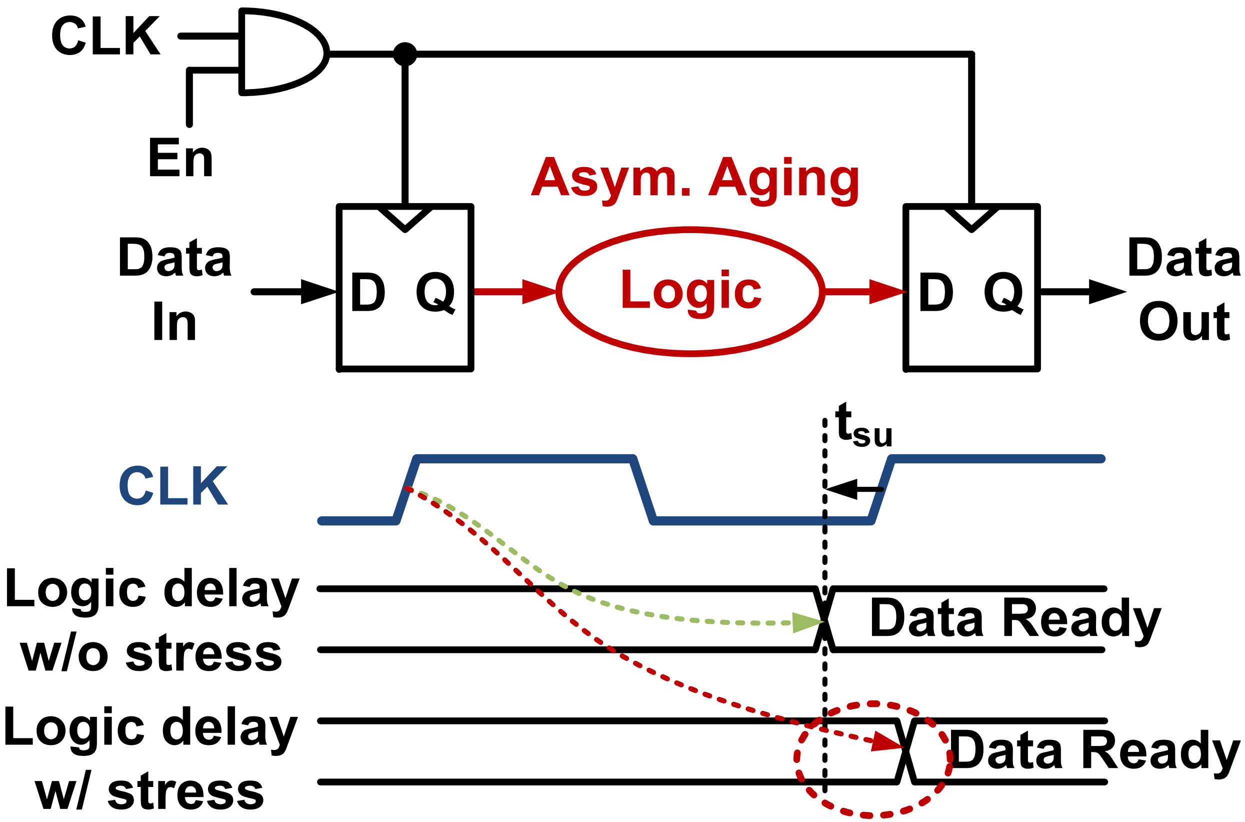
- When input is static, PMOS and NMOS in a signal path are alternately stressed
- In active mode, the 1st edge propagates through unstressed devices only
- 2nd edge propagates through stressed devices only

Case 1: Local Clock Buffer Aging



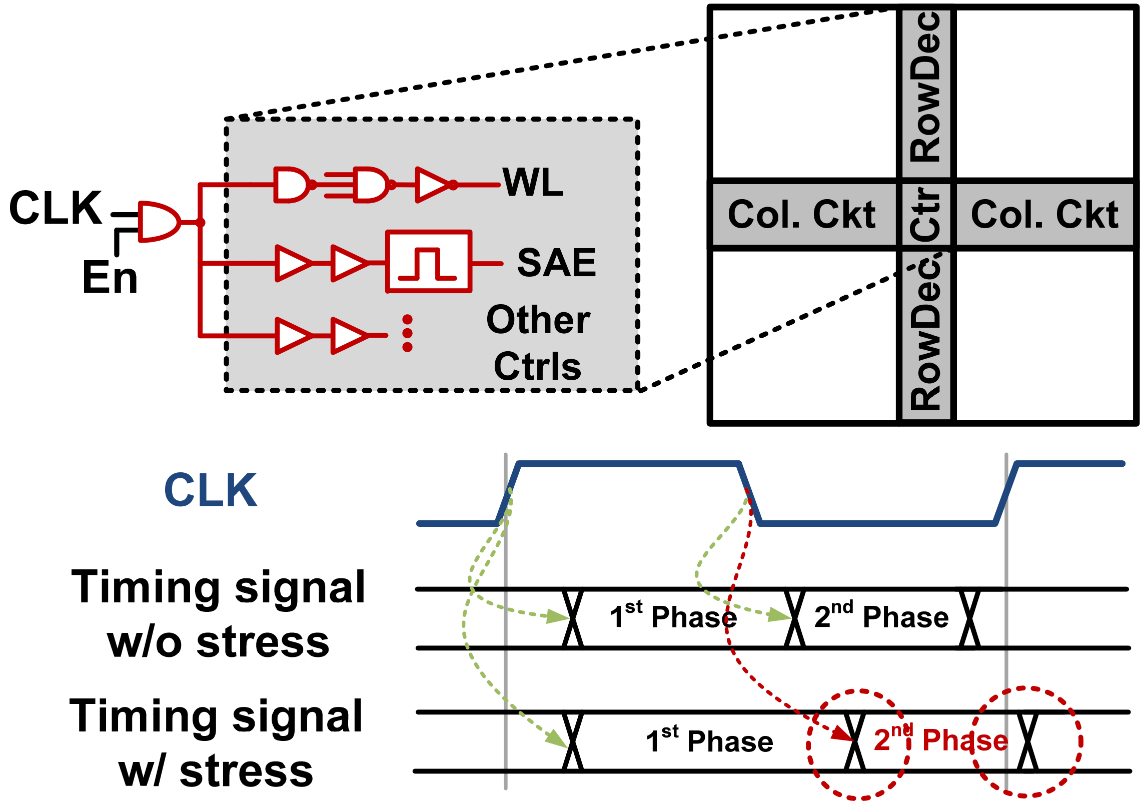
- The local clock buffer (LCB) is stressed when global clock signal is gated off → clock duty-cycle change
- Impact on duty-cycle can be small especially if leaf-level gating logic is implemented

Case 2: Logic Path Aging



- While clock is gated, the logic path undergoes DC BTI stress
- Increased logic delay lowers the operating frequency

Case 3: SRAM Timing Path Aging



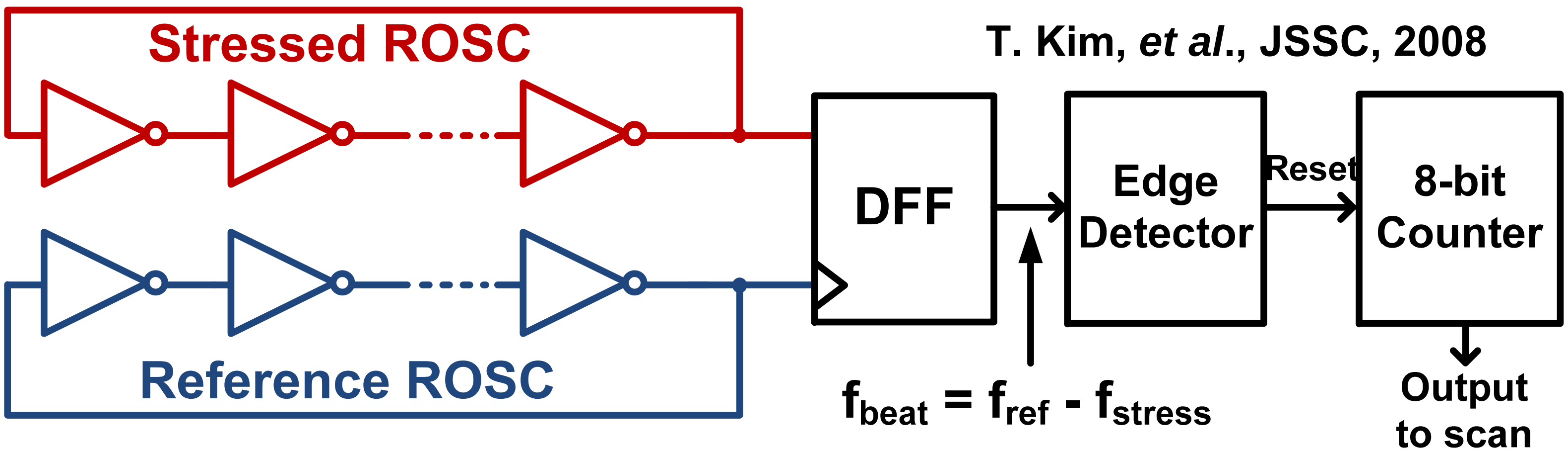
- Internal timing signal paths for SRAM operation are DC stressed when clock is gated off
- Affects the duty-cycle of critical signals such as WL, SAE, precharge, etc. → lower operating frequency

Prior Work on Asymmetric BTI Aging

- **Product drift from NBTI: Guardbanding, circuit and statistical effects (*A. Krishnan, et al., IEDM 2010*)**
  - **Experimentally shows the half-cycle paths under clock gating are more sensitive to transistor degradation**
  - **Derive formulas to calculate the additional guardband required for the asymmetric aging**
- **A TDC-based test platform for dynamic circuit aging characterization (*M. Chen, et al., IRPS 2011*)**
  - **Proposed an on-chip TDC-based technique to measure delay degradation**
- **Failure analysis of asymmetric aging under NBTI (*J. Velamala, et al., TDMR 2012*)**
  - **Proposed a failure diagnosis method for predicting timing violations**

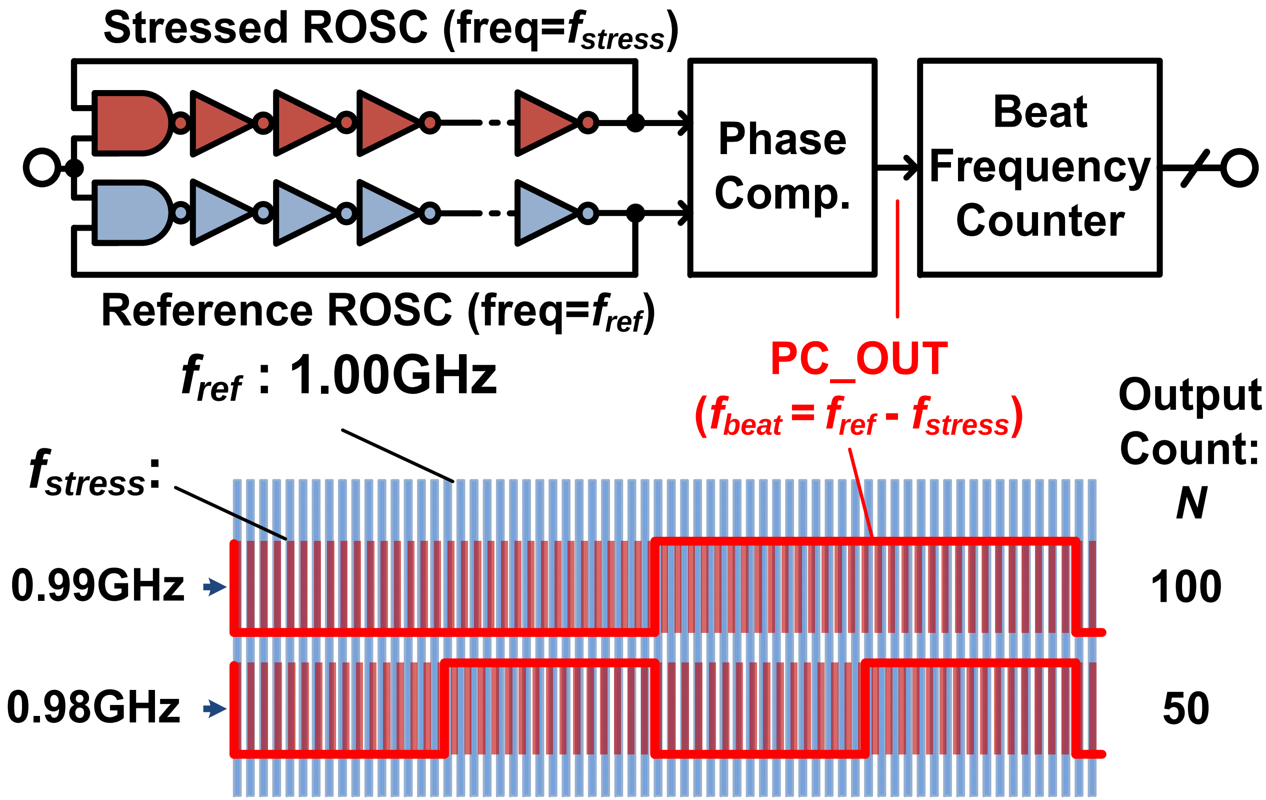
None of the previous work reported duty-cycle shift data

Silicon Odometer Beat Frequency Scheme



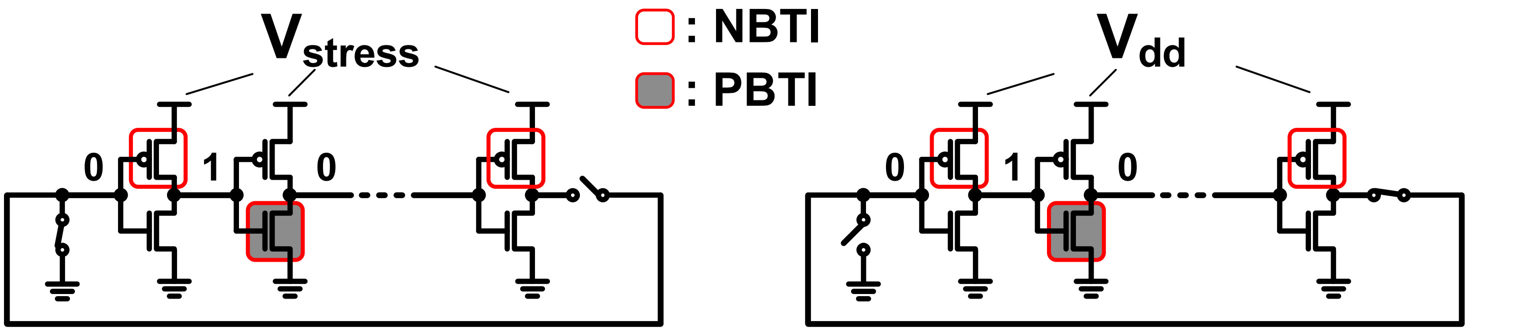
- **Beat frequency of two free running ROSCs measured by DFF and edge detector**
- **Benefits of beat frequency detection system**
  - **Achieve ps resolution with µs measurement interrupt**
  - **Insensitive to common mode noise such as temperature drifts**
  - **Fully digital, scan based interface, easy implementation**

Silicon Odometer Beat Frequency Scheme

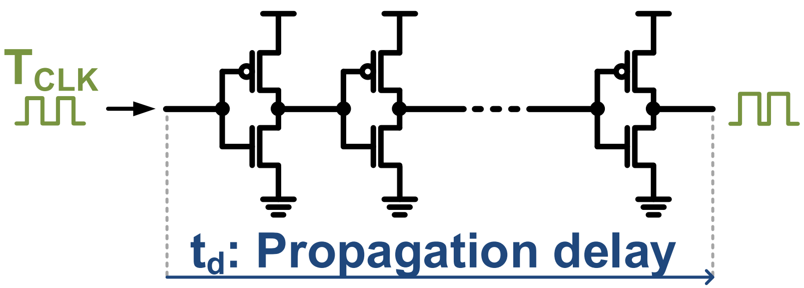


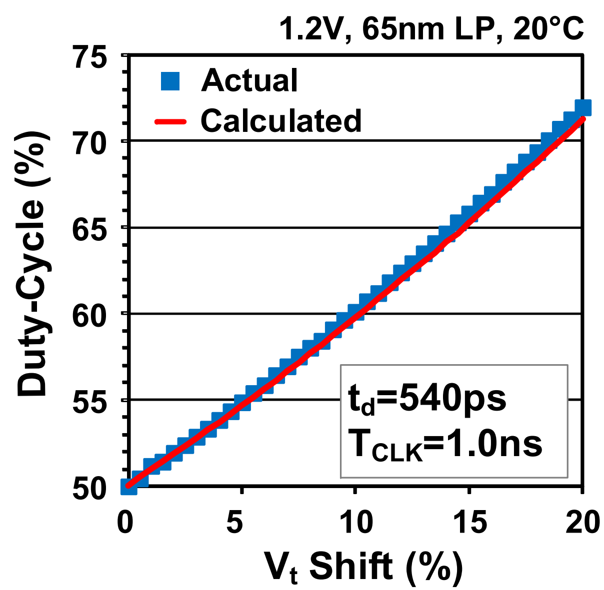
- Sample stressed ROSC output with reference ROSC
  - 1% frequency difference before stress → N=100
  - 2% frequency difference after stress → N=50
  - Δf or ΔT sensing resolution is 0.01%

Using Frequency Data to Calculate Duty-Cycle



Stress Mode **Measurement Mode**





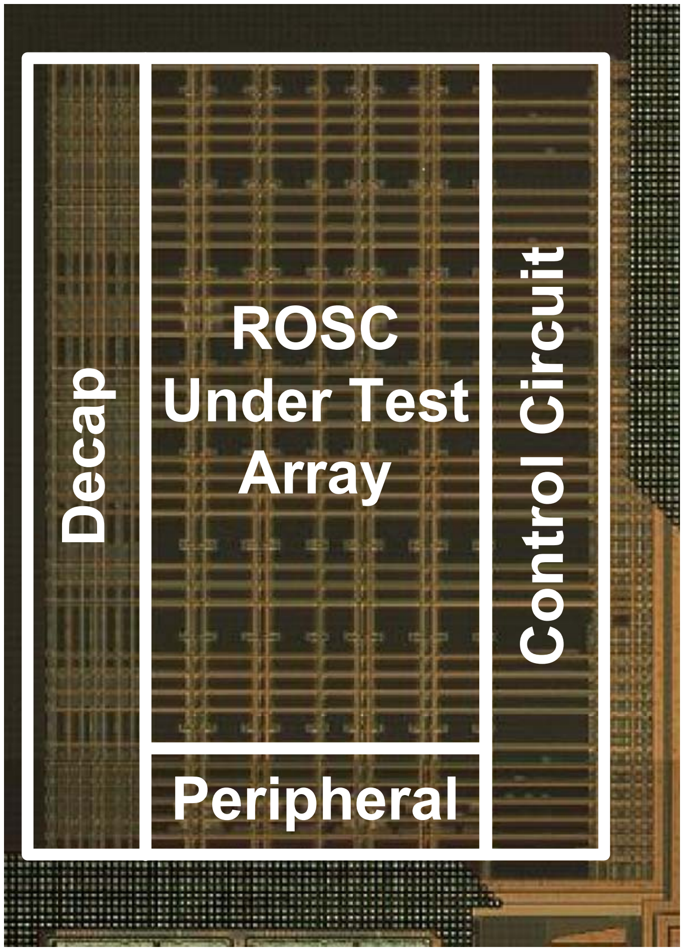
Duty-Cycle Shift (%):

$$\frac{\Delta t_d}{T_{CLK}} = \left(2\cdot\boxed{\frac{\Delta T_{ROSC}}{T_{ROSC}}}\right)\cdot\frac{t_d}{T_{CLK}}\cdot 100$$

Measured period shift

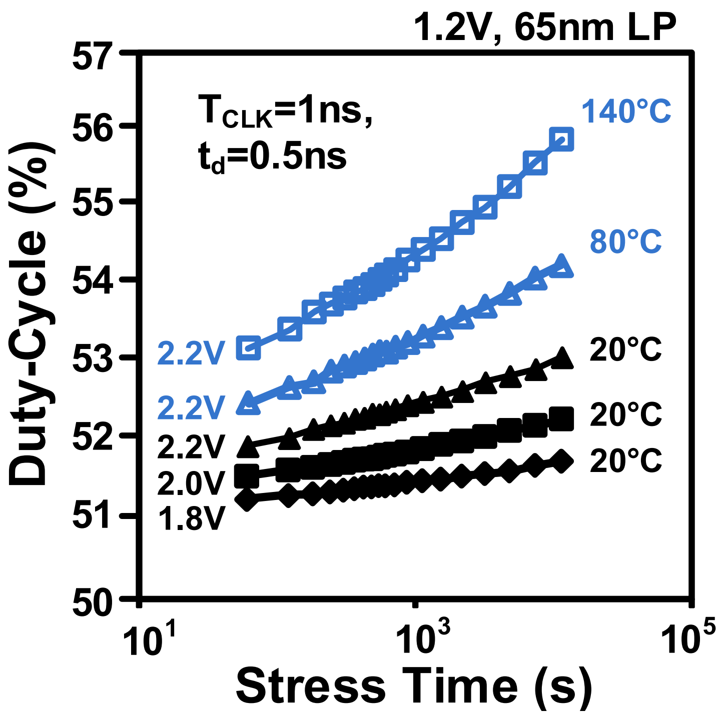
- **Use ROSC period degradation to calculate duty-cycle shift under the same amount of stress**

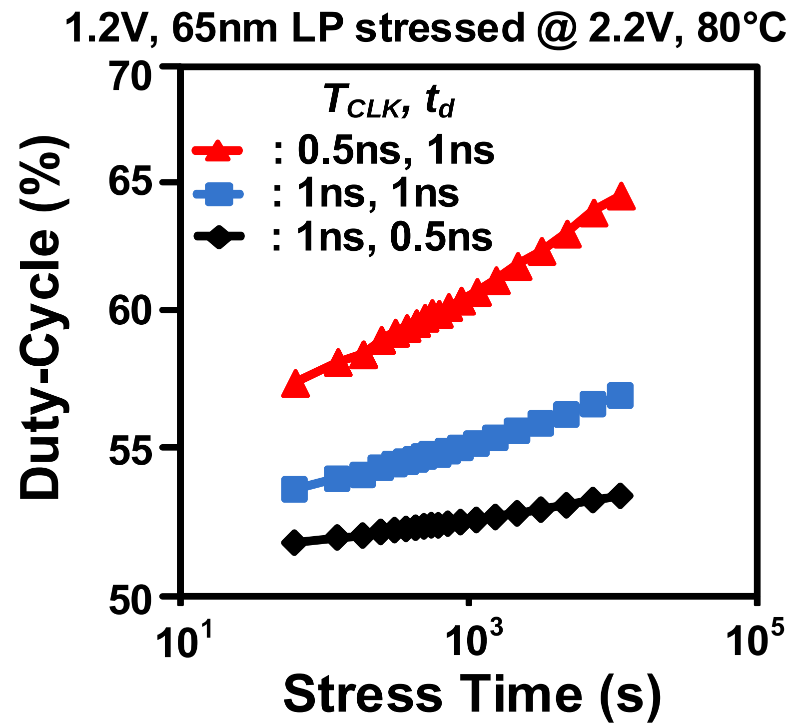
65nm Test Chip Die Photo and Features



Process	65nm LP CMOS
Core / IO Supplies	1.2V / 2.5V
Stress Voltage	1.8V, 2.0V, 2.2V
Active Area	257x475μm^2
Δf Resolution	0.07%
Meas. Interrupt	>1μs
DUT Dimensions	P: 300/60nm N: 200/60nm
Array Size	8x10

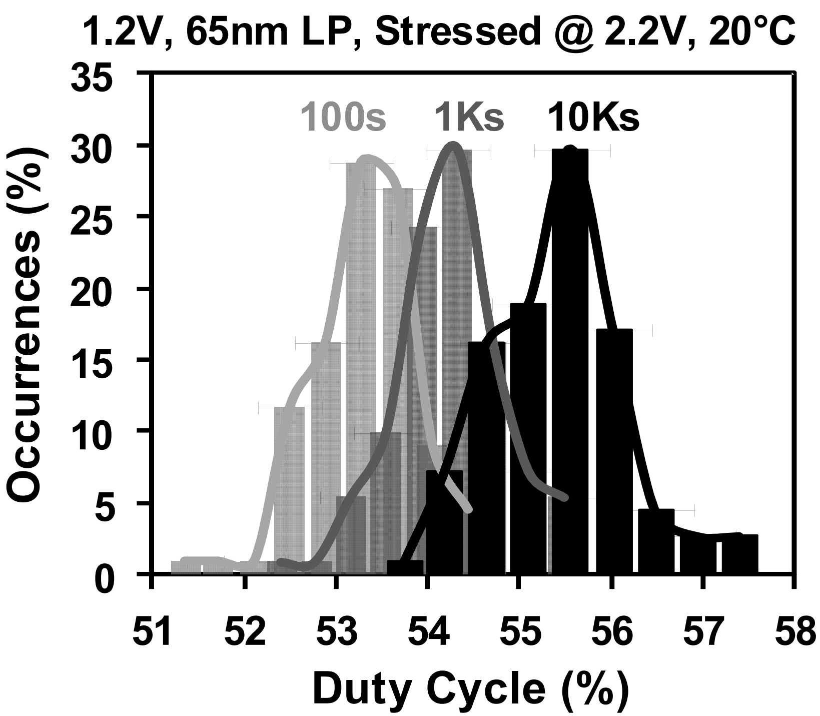
Hardware Results from Test Chips

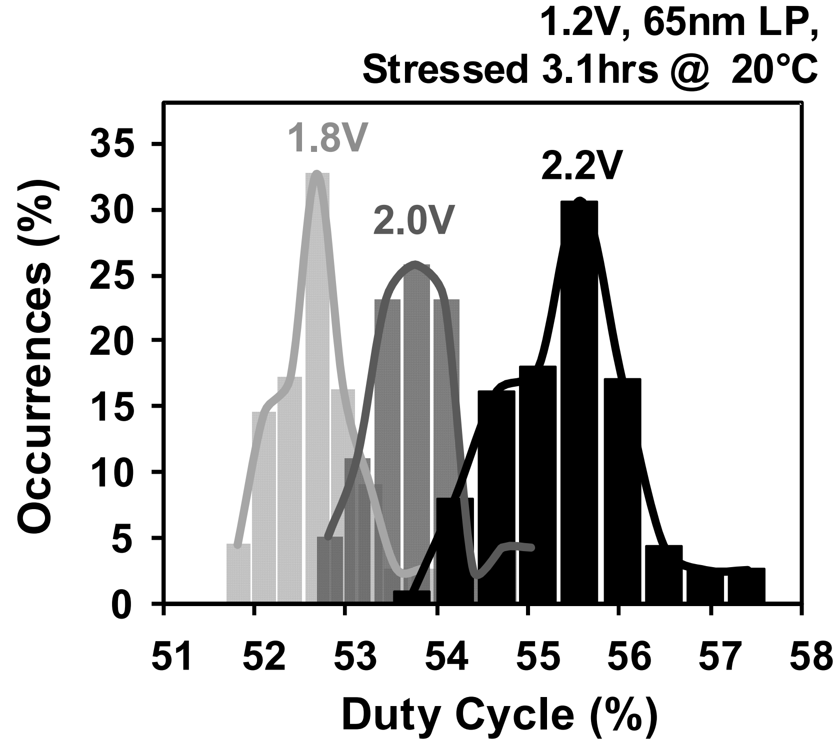




- Duty-cycle increases with higher stress voltage and temperature
- Duty-cycle shift is inversely proportional to T_{clk}, and linear with t_d

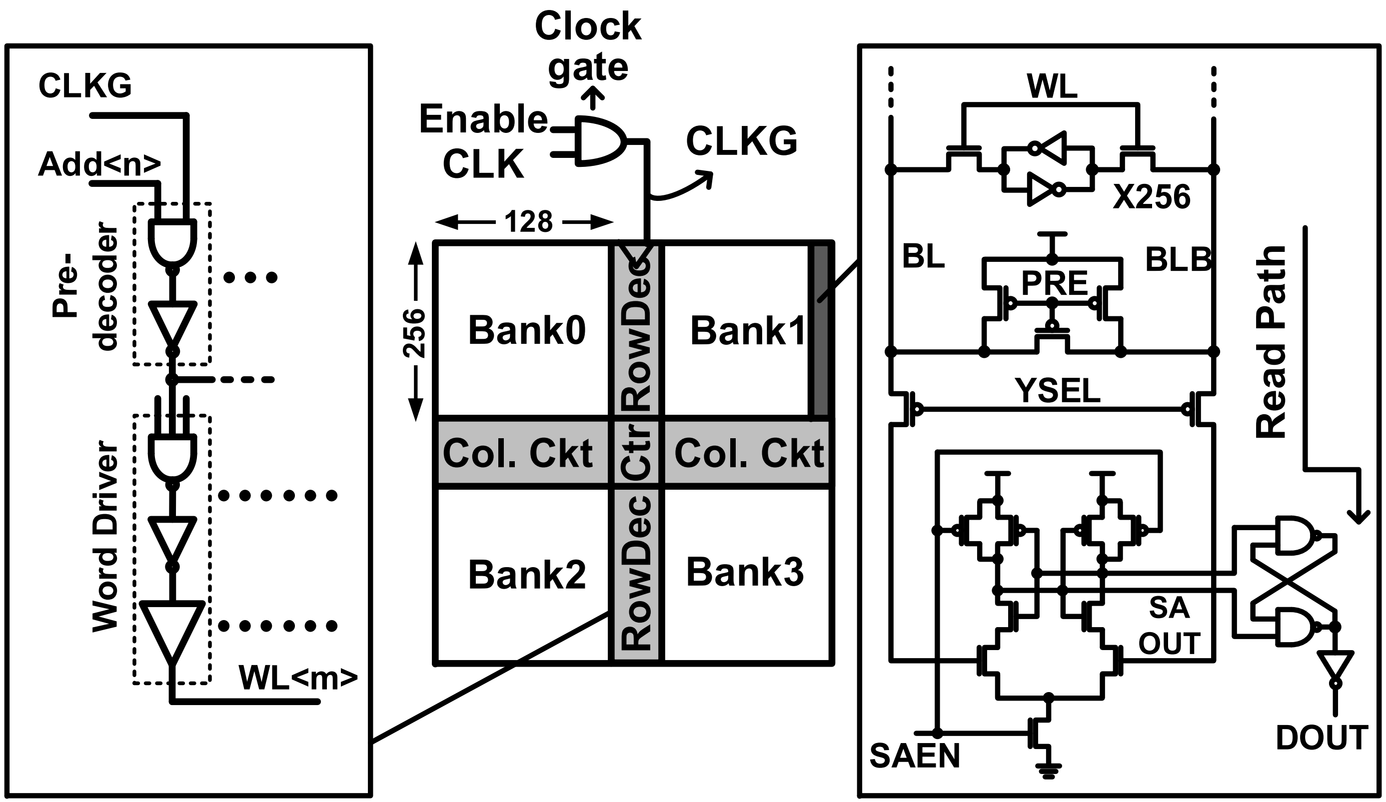
Statistical Data from Test Chips





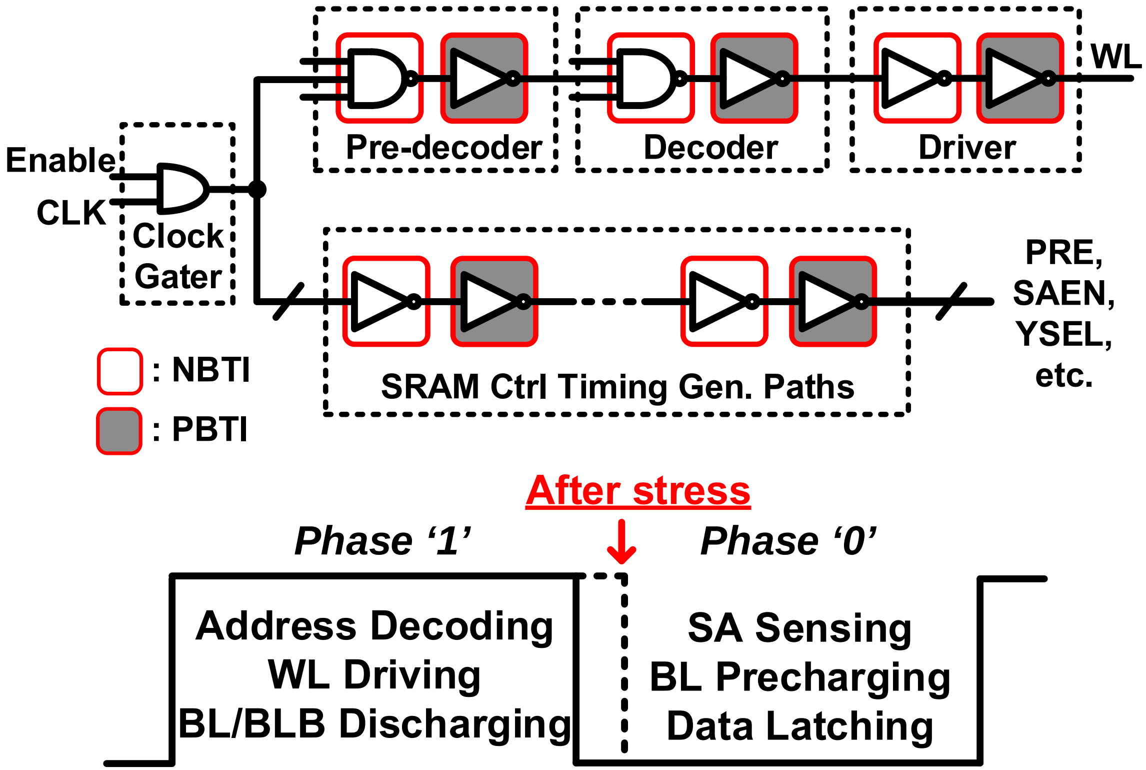
- **Duty-cycle distribution with the sample size of 80 are measured**
- **Duty-cycle distribution spreads out as the mean value increases with a higher stress voltage and longer stress time**

SRAM Array Configuration



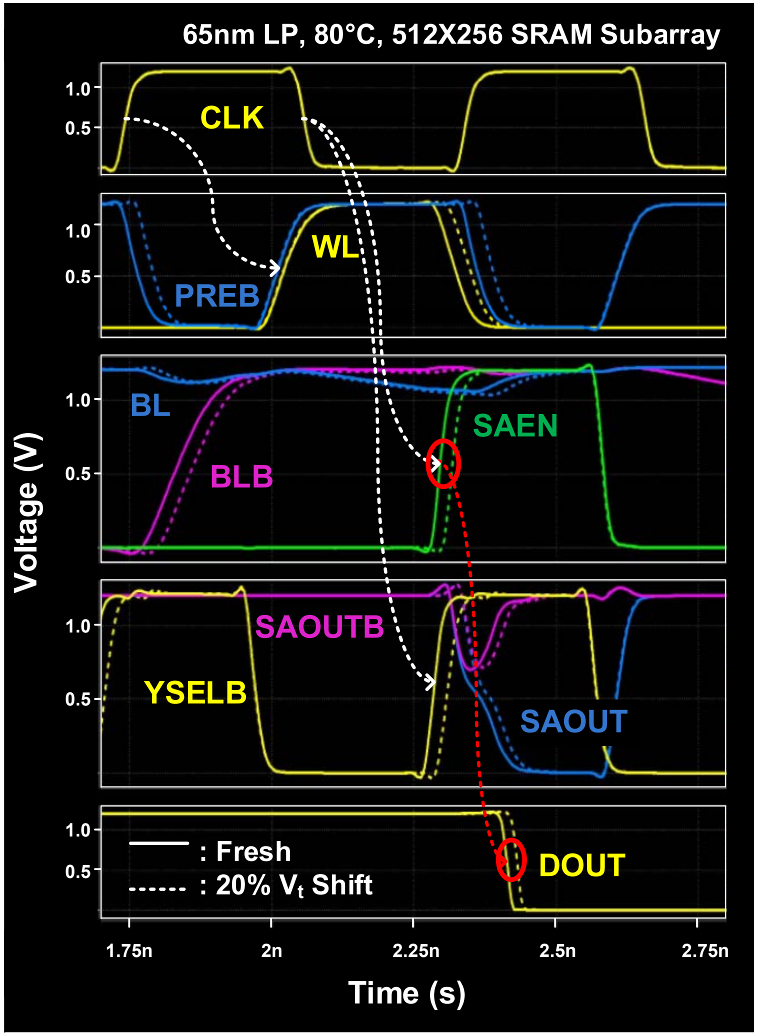
- Clock cycle = random cycle
- Clock gating technique is used to turn off the clock when set in idle
- Four banks, 256X128 for each bank, f=2.0GHz

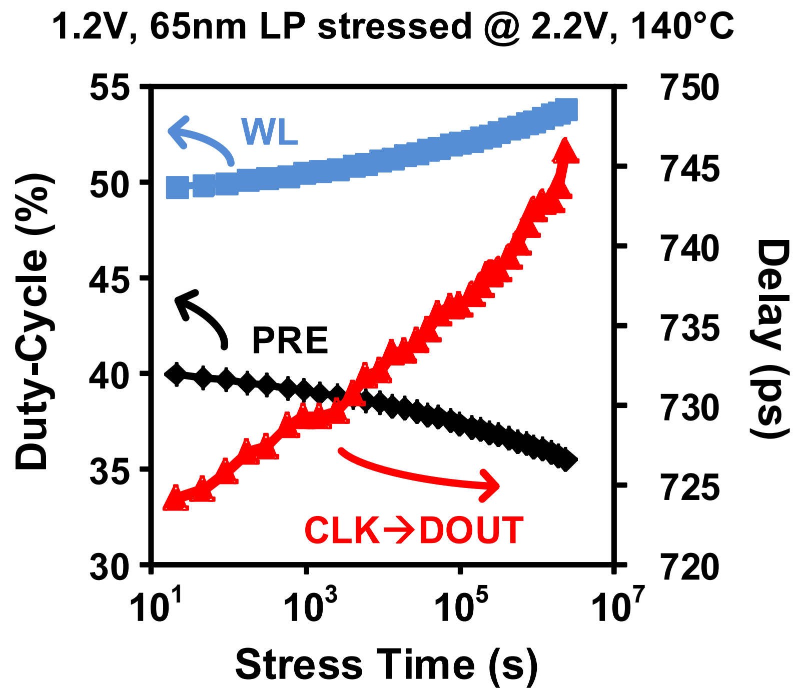
SRAM Timing Duty-Cycle Shift



- **Asymmetric BTI aging during idle mode affects the internal control cycles in the next active mode**
- **Operation cycle of phase '1' is extended, but phase '0' is shorter**

Impact on SRAM Read-after-Write Operation





- Narrower *precharge* phase
- Sense amplifier enable is delayed
- Clock-to-data delay worsens

Summary

- The odometer framework is utilized to measure the duty-cycle shift due to DC BTI aging
  - Beat-frequency detection system is adopted for high measurement precision and short measurement time
  - Simple calculation translates ROSC period shifts to duty-cycle shift
  - Experimental results are shown under different stress conditions
- The impact of the DC BTI aging on SRAM timing is studied for the first time
  - SRAM read speed degrades due to the extended WL enable phase