A Bit-by-Bit Re-Writable Eflash in a Generic Logic Process for Moderate-Density Embedded Non-Volatile Memory Applications

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Outline

• Introduction of Single-Poly Embedded Flash
• Proposed Bit-by-Bit Re-Writable Eflash
  – 6T Eflash Memory Cell
  – Negative High Voltage Switch and Charge Pump
• 65nm Eflash Test Chip Measurement Result
• Conclusions
## Embedded Non-Volatile Memories

<table>
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<tr>
<th>eNVM Technology</th>
<th>High Density eNVM (&gt;Mb)</th>
<th>Moderate Density eNVM (~kb)</th>
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<tr>
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<td>High Density Eflash, FeRAM, STT-MRAM, RRAM</td>
<td>E-Fuse, Anti-Fuse, Single-Poly Eflash</td>
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<td>Applications</td>
<td>Code Storage, Data Storage, Nonvolatile Programmable Logic</td>
<td>Redundancy Scheme, Circuit Trimming, Digital Calibration, Secure ID Storage</td>
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</table>

- A wide range of eNVM applications exists
- Moderate density eNVMs could play a key role in mitigating variability and reliability issues
Embedded NVM Examples

- **High Density eNVM (ex: Dual-Poly Eflash)**
  - **Erase**
    - 0V
    - **FG**
    - VPP
    - Low $V_{TH}$
  - **Program**
    - Re-writable
    - VPP
    - **FG**
    - 0V
    - High $V_{TH}$

- **Moderate Density eNVM (ex: Anti-Fuse)**
  - **Fresh**
    - **FG**
    - High $V_{TH}$
    - Hi-Z
  - **Program**
    - Irreversible
    - VPP
    - 0V
    - Lo-Z

- Dual-poly eflash: dense, multiple P/E operation, requires floating gate device (process overhead)
- Anti-fuse: one-time program through gate oxide breakdown, logic compatible
Single-Poly Embedded Flash

- Floating gate formed by back-to-back gates
- No process overhead beyond logic CMOS
- Higher coupling ratio reduces write voltages
- Suitable for moderate density eNVM applications
Single-Poly Eflash Basic Operation

- **Erase Operation**
  - PWL (0V) → FG (~0V) → WWL (10V) → 0V

- **Program Operation**
  - PWL (10V) → FG (~10V) → WWL (10V) → 0V

- FG node voltage follows PWL because of the high coupling capacitance between PWL and FG
- FN tunneling mechanism used for erase and program
WL-by-WL Erase vs. Bit-by-Bit Erase

- WL-by-WL erase: Cells are unnecessarily erased, no disturbance issue in unselected WL’s
- Bit-by-bit erase: Only selected cells are erased, boosted BL voltage required for erase inhibit → disturbance issues in unselected WL’s
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Proposed Selective Floating Gate Boosting Scheme

- Prior 5T eflash boosts FG irrespective of BL level
- Proposed scheme selectively boosts FG bit-by-bit
Proposed 6T Cell Write Operation

- FG is boosted higher for ‘0’ BL than ‘1’ BL
- Write ‘0’ phase: PWL driven to a small (+) voltage
- Write ‘1’ phase: PWL driven to a large (-) voltage
Read Operation

- ‘1’ cells provide larger BL current than ‘0’ cells

- BL voltages are compared to VREF using conventional voltage sense amplifiers
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Multi-Story Negative High Voltage Switch

- Stacked latch stage + driver stage
- 2.5V IO devices
- No gate overstress
- VPP4 level limited by junction breakdown voltage
On-Chip Negative Charge Pump

- Cascaded voltage doubler using metal-metal cap.

P. Favrat et al., JSSC Mar. 1998
R. Pelliconi et al., JSSC Jun. 2003
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- 2.5V I/O devices with 5nm Tox used in flash cells and high voltage switch
Waveforms of CP and HVS

- CP generates four boosted (-) levels (VPP1-4)
- Multi-story HVS generates WWL/PWL pulses
Bit-by-Bit Update Sequence

- Bit-by-bit update sequence from (0101) to (1100)
- Initial read
Bit-by-Bit Update Sequence

- Bit-by-bit update sequence from (0101) to (1100)
- Initial read $\rightarrow$ write ‘0’ phase
Bit-by-Bit Update Sequence

- Bit-by-bit update sequence from (0101) to (1100)
- Initial read → write ‘0’ phase → write ‘1’ phase
Bit-by-Bit Re-Write Measurements

- Disturbance in ‘1’ BL cells during write ‘0’ phase
- Write ‘0’ speed depends on the data pattern
Retention and Endurance

- Median cells with 1k pre-cycles meet 1 year reten.
- Overall endurance improved by 8x using bit-by-bit write
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### Comparison with Prior eNVMs

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<tbody>
<tr>
<td>Process</td>
<td>32nm Logic</td>
<td>65nm Logic</td>
<td>0.18μm Logic</td>
<td>65nm Logic</td>
<td>65nm Logic</td>
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<tr>
<td>Access or Cell Transistor</td>
<td>1.8V I/O TR</td>
<td>3.3V I/O TR</td>
<td>3.3V I/O TR</td>
<td>2.5V I/O TR</td>
<td>2.5V I/O TR</td>
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<tr>
<td>Writing Method</td>
<td>Gate Oxide Breakdown</td>
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<td>FN Tunneling</td>
<td>FN Tunneling</td>
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<tr>
<td>Bit-by-Bit Rewrite</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
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<tr>
<td>Unsel. WL Disturb</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
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<tr>
<td>Unit Cell Area</td>
<td>1.01μm$^2$</td>
<td>15.3μm$^2$</td>
<td>220μm$^2$</td>
<td>8.62μm$^2$</td>
<td>15.3μm$^2$</td>
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<tr>
<td>Capacity</td>
<td>1kb</td>
<td>8kb</td>
<td>192b</td>
<td>2kb</td>
<td>4kb</td>
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</tbody>
</table>


- **Bit-by-bit access with minimum disturbance**
Summary

• Single-poly embedded flash memory
  – Suitable for moderate density eNVM applications
  – No process overhead beyond logic CMOS
  – Previous bit-by-bit erase scheme suffers from high voltage disturbance issues in unselected WLs

• Proposed bit-by-bit re-writable 6T eflash
  – Selective FG boosting technique prevents disturbance in unselected WLs
  – On-chip negative high voltage switch and charge pump generate WL pulses
  – 4kb eflash test chip demonstrated in a generic 65nm logic process